PEX Bus Specification

Issue 3

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Trademarks

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Chapter 1 - PEX Bus Specification

Introduction

The PEX Bus (**P**rocessor **EX**tension **Bus**) is a standard interface used to allow the connection of extra facilities to the Radstone range of VME processor boards. The PEX interface permits communication between a host processor and a selection of plug-in boards each of which provides some extra function such as, for example, a SCSI Interface.

While designed to be moderately flexible, the majority of the signals used are specifically defined regarding timing, drive levels and functions. There are also signals which do not have pre-defined functions and are present to allow for user defined functions.

The PEX Bus itself comprises a 40-pin connector organised as two rows of 20 pins. Also defined by the PEX Bus are the maximum PEX board size, component heights on both the PEX board and the host pcb (where the PEX board is located), areas used for connectors (PEX and connections to the outside world via the front panel of the host board) and where the PEX board is physically attached to the host board.

A PEX board is addressed in much the same way as VLSI devices by providing a Chip Select type signal because the PEX interface uses the lowest eight address lines and the highest eight data lines (non multiplexed). Most signals are defined in an asynchronous manner with respect to the system or processor clocks. Signalling conventions used on the PEX board will allow easy integration into the 68000 family environment since the pre-defined signals are optimised to this specification and need little or no conditioning of the interface signals.

The remainder of this specification is organised as follows:

Chapter 2 - PEX Signal Definitions

Chapter 3 - PEX Signal Timings

Chapter 4 - Signal Drive Levels and Loading Specifications

Chapter 5 - PEX Bus Mechanical Details

Note: Since arbitration is not needed on the PEX Bus, the use of Read-Modify-Write cycles is not normally used in the standard implementation of the PEX interface. Consequently, while not ruling out the use of Read-Modify-Write cycles, this specification does not define such a cycle as applied to the PEX Bus. It is therefore advised that if possible, Read-Modify-Write cycles should not be used. PEX Bus boards do not have to incorporate the facility for Read-Modify-Write.

PEX Module Identification

Each PEX module must provide a unique identification number when a read takes place from location base address +FF hex.

PEX identification numbers will be allocated, upon request, by the Marketing Department at Radstone Technology.

PEX/APEX ID HEX		
-	PEX-1 SCSI I/F	PEX Modules
02		
03	PEX-3 FDC I/F	
04	PEX-4 Parallel I/O	
05	PEX-5 IEEE 488 I/F	
06		
etc		
80	APEX-100 (Ethernet)	APEX Modules
81		
82		
etc		
FF	Reserved	

Chapter 2 - Signal Definitions

Input Signals

Address Lines (PA7 - PA0)

The PEX Bus interface uses 8 address lines. On processors with address line A0, these will be A7 - A0, otherwise they are to be A8 - A1 inclusive. They are active high and are validated by the address-strobe (AS*) signal. Address lines are not allowed to change their state after address-strobe until that cycle is completed, signalled by AS* becoming non-valid. The most significant address line is PA7 and the least significant PA0.

PEX SELect (PEXSEL*)

This active low signal indicates to the PEX board whether or not the board has been selected for that cycle. When in the high (inactive) state, this is used to prevent all the outputs from the PEX board from driving the bus, with the exception of RESET*, PEXINT* and PEXPRES*. The PEXOUT* signal may or may not be affected by PEXSEL* depending on its implementation. PEXSEL* may be used to latch the address bus and/or other inputs.

When inactive, no input on either input-only or bi-directional lines will be recognised with the exception of RESET* and PEXIN* (if defined to respond without the presence of PEXSEL*, otherwise it will not be affected).

In the low (active) state, this input upon becoming valid must remain so until the cycle ends.

Address Strobe (AS*)

The Address Strobe signal is active low. AS* must not become valid until the address lines have become valid (as defined by the timing relationships). On a PEX Bus cycle, this input must stay valid until the cycle ends or is terminated. When the PEX board is not selected, AS* may change state as appropriate without affecting the PEX board.

Read/Write (R/W*)

This signal shows the data direction for a cycle. When high, this line indicates the host processor is in Read mode and expects data to be output from the PEX board. When low, data is to be transferred to the PEX board. R/W* must be qualified by PEXSEL* in order to be recognised by the PEX board and must remain at either the high or low state throughout the cycle.

Data Strobe (DS*)

An active low signal asserted when valid data is available during a Write cycle and is low throughout the Read cycle. DS* must be qualified by PEXSEL* to be accepted.

PEXIN

This is a spare input used to transfer extra information of an application specific nature across the PEX Bus to a PEX board. Functionality and timing are thus defined by system and application needs only. PEXIN may be qualified by PEXSEL* but this is not an essential requirement of the PEX Bus definition. Leave unconnected on the host board or PEX board if not needed.

Output Signals

DSACK0*

This is like the signal DTACK* for 68000/010 range of processors. It is used to signal data transfer has been completed over all 8 bits of the data bus. DSACK0* is driven low by the PEX board only after data has been transferred correctly; it must not be driven if the PEX board recognises that an error of some description has occurred. DSACK0* must be tri-stated when the PEX board is not being accessed.

BERR*

When an error occurs, the cycle is terminated with the bus error signal BERR*, an active low tri-state logic signal. BERR* must be qualified by the presence of PEXSEL* before it can be used. If BERR* becomes valid, the current cycle will be terminated. DSACK0* must not be asserted to show data transfer in any cycle when BERR* becomes valid.

PEXINT*

Used by the PEX Bus to signal an interrupt request from a PEX board to the host processor. This active low signal does not need qualifying by any other signal, it may become valid at any time. It is not an Open Collector signal and will require buffering on the host board.

PEXPRES*

PEXPRES* is used to show the presence of a PEX Bus board allowing the processor to poll this line to determine the presence of a PEX board. On the PEX board this is tied to 0 volts at all times; on the host board PEXPRES* will normally be connected to +5 volts via a pull-up resistor.

PEXOUT*

An active low signal output from the PEX board. The function and timing specification are defined by the circuit requirements, only the loading parameters are defined for this output.

Use of this output is complementary to the PEXIN* input signal.

Bi-directional Signals

Data Lines (PD7 - PD0)

These data lines are used by the PEX interface as the primary means of data transfer. PD7 is the most significant data line and PD0 the least significant. All data lines are non-inverted. Direction of data transfer is given by the input signal R/W* and successful data transfer is acknowledged by assertion of DSACK0* by the PEX board. These data lines must be tri-stated when PEXSEL* is not valid. As outputs, tri-state logic must be used and no pull-up or pull-down resistors are to be used on these lines directly. During a Write cycle to the PEX board, valid data is shown by the host boards assertion of the DS* signal. During a Read from the PEX board, DSACK0* is used to qualify the data on PD7-0. The data lines are active high.

RESET*

This signal may be used at any time, either by the host board to reset the PEX board or by the PEX board to reset the rest of the system. In applications where the PEX board is allowed to drive the RESET* line, the output type can be either tri-state or open-collector/open-drain but the latter is preferable since the RESET* line must have a pull-up resistor positioned on the main board and not on the PEX board. Resetting the PEX board needs this line to be driven low for more than 25μs. For the PEX board to reset the host processor, this line must be low for more than 50μs.

Clock Signals

PROCLK

Generated on the host, this signal must be of the same frequency as the host processor clock and be synchronised with it. It must be present at all times that the system is up and it must have a Mark/Space ratio of between 40:60 and 50:50.

SYSCLK

Also generated on the host, this signal is to be 16MHz and in phase with the system clock. It must be present at all times when the system is up and have a Mark/Space ratio of between 40:60 and 50:50.

Power Lines

Vcc rail

There are three +5 Volt power lines, all of which must be connected together on both the PEX board and the host board. This must remain within tolerance as long as the system is powered up.

0V rail

There are four 0 Volt lines which must be connected together at all times on both the PEX board and the host board.

+12volts

This line is to be connected to +12 Volts while the system is powered up and must remain within tolerance at all times.

- 12volts

This line is to be connected to -12 Volts while the system is powered up and must remain within tolerance at all times.

VALWAYS

This line may be connected to the +5VSTDBY on the VMEbus or some other source on the host board. This may be done directly or indirectly thus allowing for a circuit to reduce the rail voltage under power-down conditions.

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Chapter 3 - Timing Diagrams

Introduction

Since many of the signals of the PEX Bus have either no specific timing relationships or are completely asynchronous in that they may occur any time, the timing relationships only show read and write cycles, with and without bus error situations. Not all of the PEX signals are shown on the timing diagrams. Those that are not shown explicitly are implied by their nature or will have no significance in a cycle should they change state. PEXIN and PEXOUT are situation defined. The signal timings are therefore defined by the designer and are only specified in terms of loading and drive information by the PEX Bus.

Cycles without BERR*

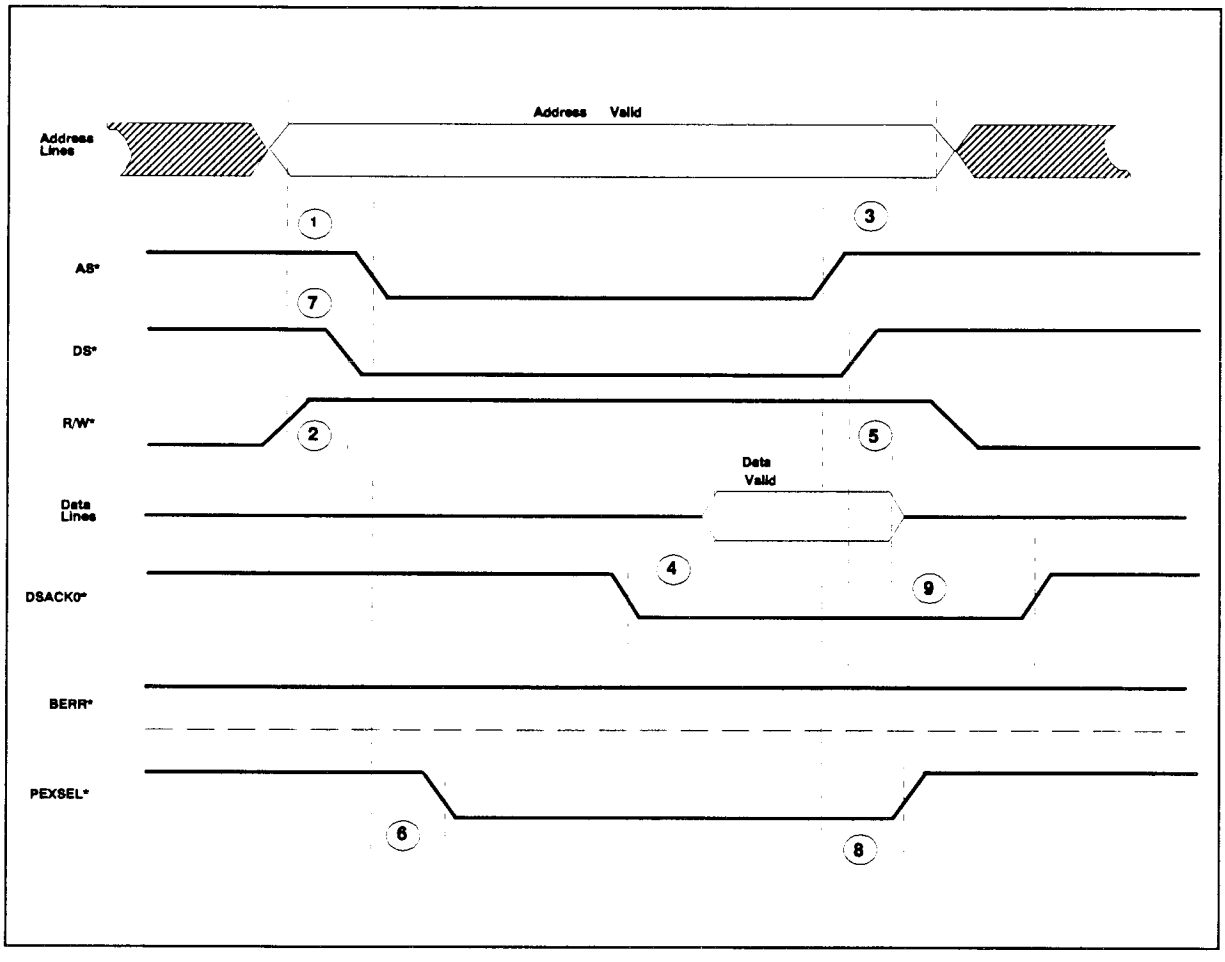
Read Cycle

This is shown in Figure 1, all important timings shown on the diagram are given in Table 1. Note that the timings are independent of processor or system clocks as far as PEX boards are concerned.

Table 1 - Timing Parameters for Read Without Bus Error

Number	Parameter	Min (nsec)	Max (nsec)
1	Address valid to AS* valid	5	--
2	R/W* valid to AS* valid	5	--
3	Address hold time	5	--
4	DSACK0* valid to Data valid	--	0
5	Data hold time	0	35
6	AS* valid to PEXSEL* valid	0	--
7	AS* to DS* skew	-20	+20
8	AS* not-valid to PEXSEL* not valid	0	40
9	DS* not-valid to DSACK0* or BERR* not valid	0	25

Figure 1 - Read Cycle Without Bus Error



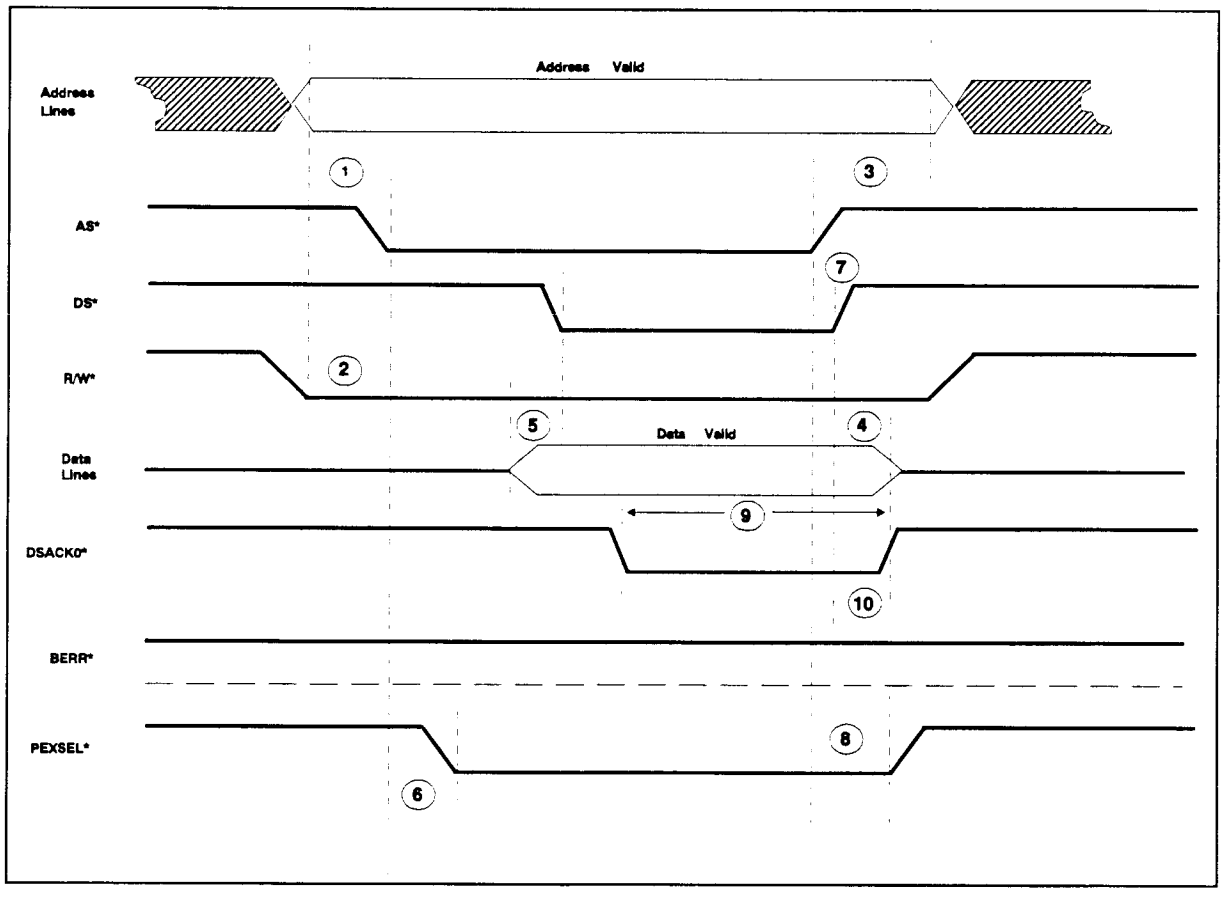
Write Cycle Timing

The important timing relationships are shown in Figure 2, the key to the diagram is shown in Table 2. DSACK0* may occur at any time after the Data has become valid.

Table 2 - Write Timing Parameters Without Bus Error

Number	Parameter	min (nsec)	max (nsec)
1	Address valid to AS* valid	5	--
2	R/W* to AS* valid	5	--
3	Address hold time	5	--
4	DS* not-valid to Data not-valid	5	--
5	Data set-up time	0	--
6	AS* valid to PEXSEL* valid	0	--
7	AS* to DS* skew	-20	+20
8	AS* not-valid to PEXSEL* not-valid	0	40
9	DSACK* TO DATA not valid	20	--
10	DS* not valid to DSACK0* or BERR* not valid	0	25

Figure 2 - Write Cycle Without Bus Error

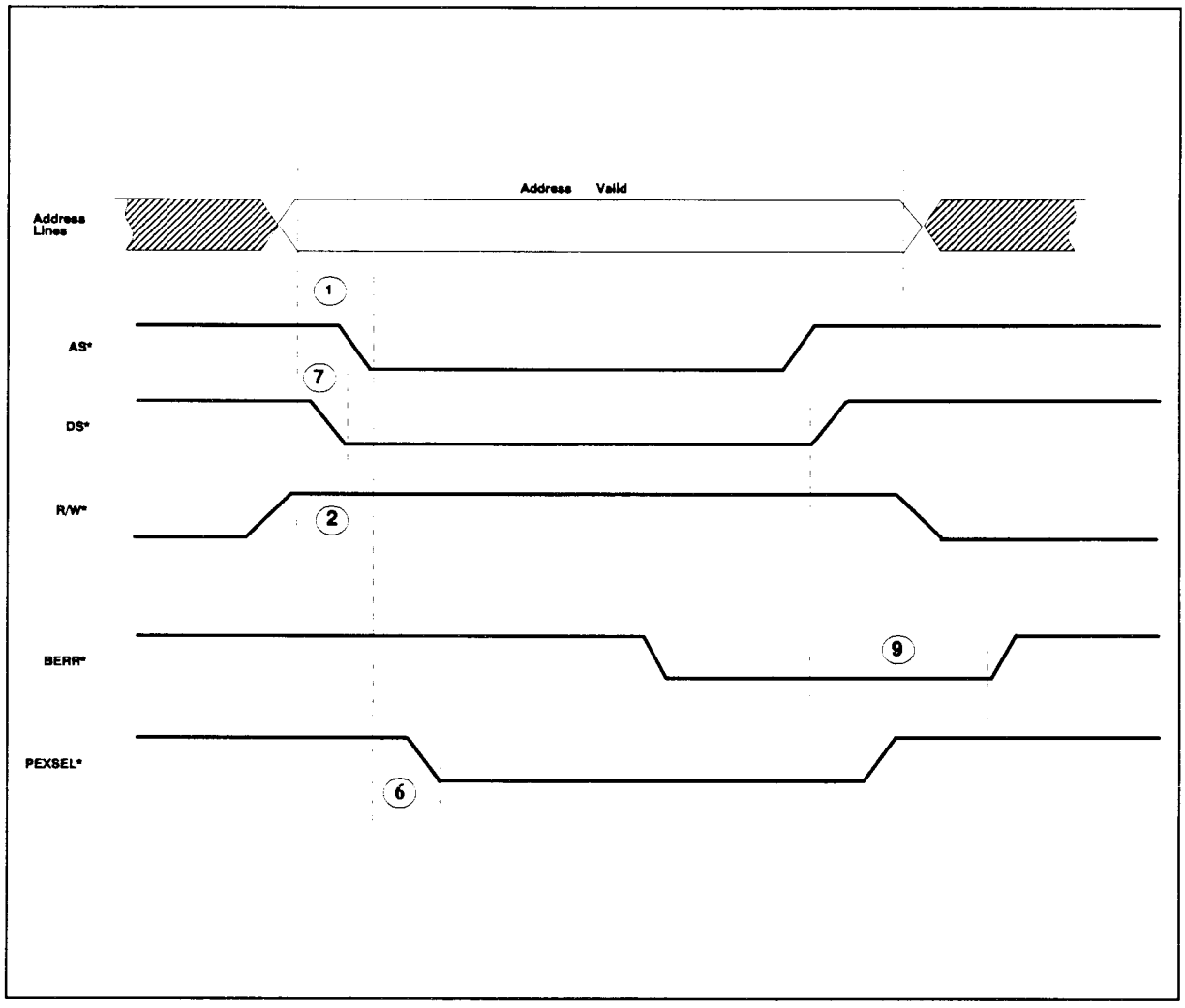


Cycles with BERR*

Read Cycle with BERR*

In this cycle, DSACK0* must not be asserted. The timings for a read with BERR* are shown in Figure 3. The values of the timing parameters indicated on the diagram are the same as shown in Table 1 for a Read cycle without BERR*.

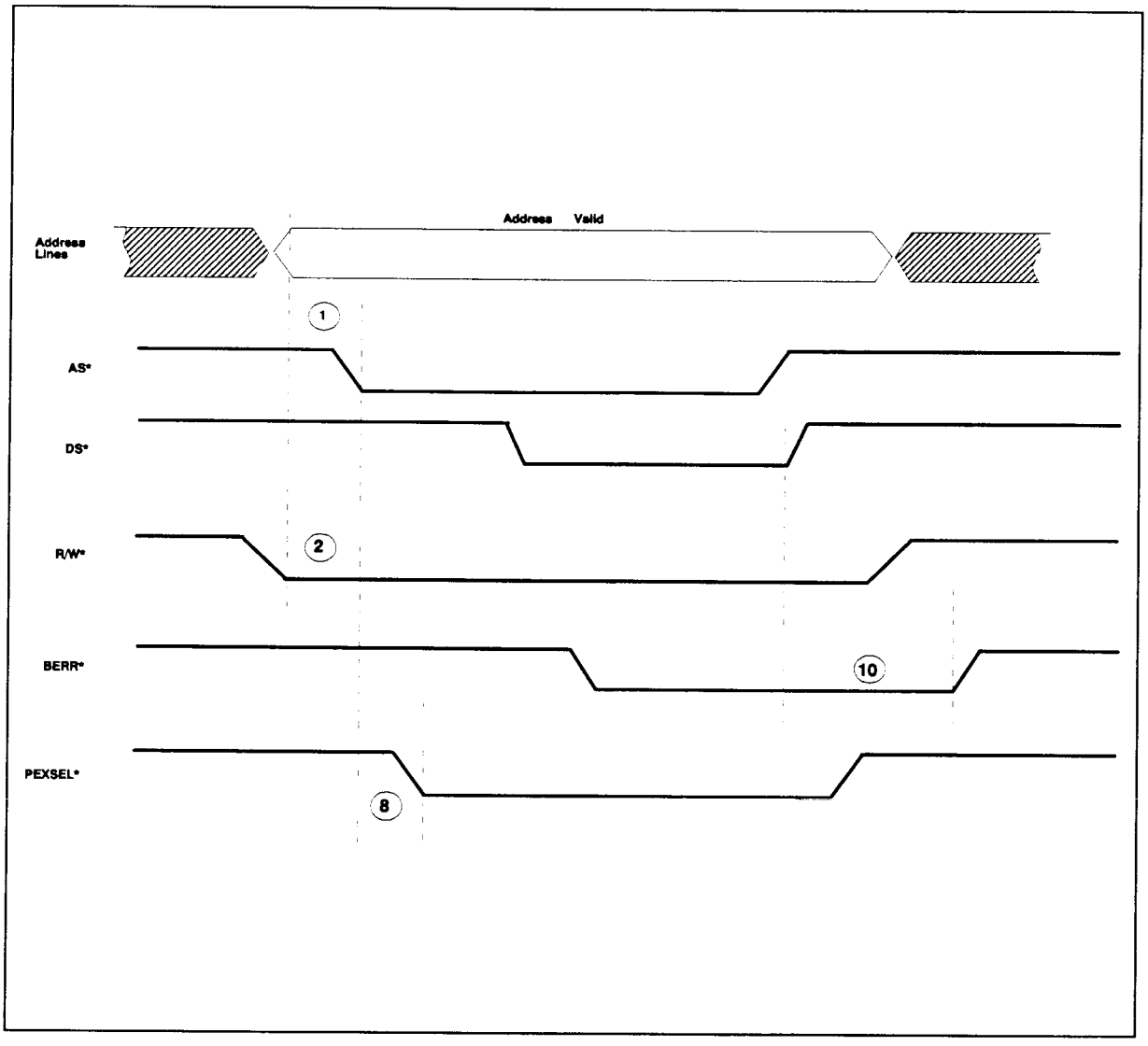
Figure 3 - Read Cycle With Bus Error



Write Cycle with BERR*

DSACK0* must not be asserted during this cycle. The timing relationships between the signals are shown in Figure 4 where the parameters marked are given in the table corresponding to a write cycle without BERR* (Table 2).

Figure 4 - Write Cycle With Bus Error



Clock Signals

Both clock signals PROCLK and SYSCLK are to have mark space ratios of between 40:60 and 50:50 and rise and fall times of no more than 10nsec. each. SYSCLK is to have a frequency of 16MHz to within 200 ppm. The frequency of PROCLK is to be the same as the processor clock and is to be in phase with the processor clock.

Chapter 4 - Loading Characteristics

Input Loading Characteristics

All Inputs

These characteristics relate to both input only signals and to bi-directional signals when being used as inputs. This does not apply to power rails.

Input current (logic 1)	<40μA	for all V_{in} such that 2.0V <=V_{in} <=Vcc
Input current (logic 0)	<800μA	for all V_{in} such that Vss <=V_{in} <=0.8V
Input voltage (logic 1)	>2.0v	for all I_{in} such that 0μA <=I_{in} <=40μA
Input voltage (logic 0)	<0.8v	for all I_{in} such that 0μA <=I_{in} <=800μA
Capacitive loading	30 pF	

Output Loading

All Output

This applies to all output only lines and bi-directional signals when configured as outputs but not to power rails.

Output current (logic 1)	>1μA	for all V_{out} such that 2.0V <=V_{out} <=V_{cc}
Output current (logic 0)	>20μA	for all V_{out} such that Vss <=V_{out} <=0.8V
Output voltage (logic 1)	>2.0v	for all I_{out} such that 0μA <=I_{out} <=1μA
Output voltage (logic 0)	<0.6v	for all I_{out} such that 0μA <=I_{out} <=8μA
Capacitive loading	2pF	

Note that I_{in} and I_{out} refer to the currents passing through the inputs or outputs of the PEX Bus, they convey information as to the magnitude of these currents but do not specify the direction of current flow.

Power Rails

V_{cc} Rail

The three pins on the connector must not carry more than 1A each, the supply tolerance for this rail is:

$+4.75V < V_{cc} < +5.25V$

This applies at all currents up to the rated maximum. There must to be no more than 50mV supply rail ripple on these lines. V_{cc} pins on both the main PCB and the PEX board must be connected to each other on their own side of the interface.

V_{ss} Rail

This supply rail comprises four pins of the PEX connector. All four lines must be connected to each other on both sides of the interface. This rail is used for reference purposes for voltages on either side of the PEX interface. No more than 1A is to flow through any single pin.

$V_{ss} = 0V$

+12V Rail

No more than 1A is to flow through this pin on the connector. The permissible voltage range for this rail is:

+11.5V < +12V rail < +12.5V

The ripple in this rail must not exceed 120mV

- 12V Rail

No more than 1A is to flow through this connector pin. Supply variation must not deviate from the range:

-12.5V < -12V Rail < -11.5V

The ripple must not exceed 120mV.

VALWAYS (optional)

No more than 1A is to flow through this pin on the connector. When power on V_{cc} is available, this supply rail voltage must be within the range:

+4.75V <VALWAYS < +5.25V

when power is not available on V_{cc}, this voltage must be within the range:

+2.5V <VALWAYS < +5.25V

Ripple on this rail must not exceed 50mV in either case. During transition periods between V_{cc} available to V_{cc} not available, the supply rail must rise or fall smoothly. On power down, rate of change of this rail must not exceed -0.5V/μs. between working and backup voltage levels. On power up, rate of change of this rail must be between +0.5V/μs. during the transition from backup to working levels. Ripple during the transition must not exceed 50mV superimposed on the rising or falling rail voltage.

Chapter 5 - Mechanical Details.

Introduction

The PEX Bus specifies the following mechanical parameters:

1. Maximum size of PEX board
2. Positioning of PEX board on main board
3. Connectors used
4. Component maximum height

It is intended that only one PEX board (if any) be mounted on the PEX interface at any given time, although this does not imply that a particular host board is only permitted to use one of the PEX board range. PEX boards may vary in both size and shape where only the maximum dimensions are specified. It is not permitted to move the location of the PEX connector towards or away from the front panel, nor rotate the connector. The PEX board is to be mounted on the host board such that the component sides of the two boards are adjacent.

As the host and PEX board combination are to occupy a single width slot on the backplane, it will not be possible to use double stacking techniques on the PEX board or the host board (in the region of the PEX interface). Thus the use of IC sockets is not possible either. The output from the PEX board to the outside world (eg. SCSI connector, etc.) will necessitate an area of the host PCB to be left un-used to allow sufficient space for the connector itself. More space will also have to be left to provide mounting holes to secure the PEX board to the host.

Positioning of the PEX board is only specified in terms of orientation and position from the front panel. Precisely where on the front panel the PEX interface will appear can change from host to host provided that the PEX Bus specifications for the area of the main board to be used are adhered to.

Size of PEX Boards

Figure 5 shows the maximum dimension of a PEX board, these may be reduced slightly. The limit of any such reduction is to the point where the mounting holes become 5mm away from the edge of the PEX board. Such size reduction may be used only in the design of PEX boards - not their hosts.

Positioning of PEX Board on the Host

This is dependant on the component layout of the host PCB and is defined in Figures 6 and 7 regarding only the height above the host board and where along the front panel of the host the PEX board may be placed. This will therefore determine where the host PCB will be height limited and where space for the front panel connector and PEX board mounting holes will need to be left. Actual installation of a PEX board (fittings, screws etc.) is detailed in Figure 7.

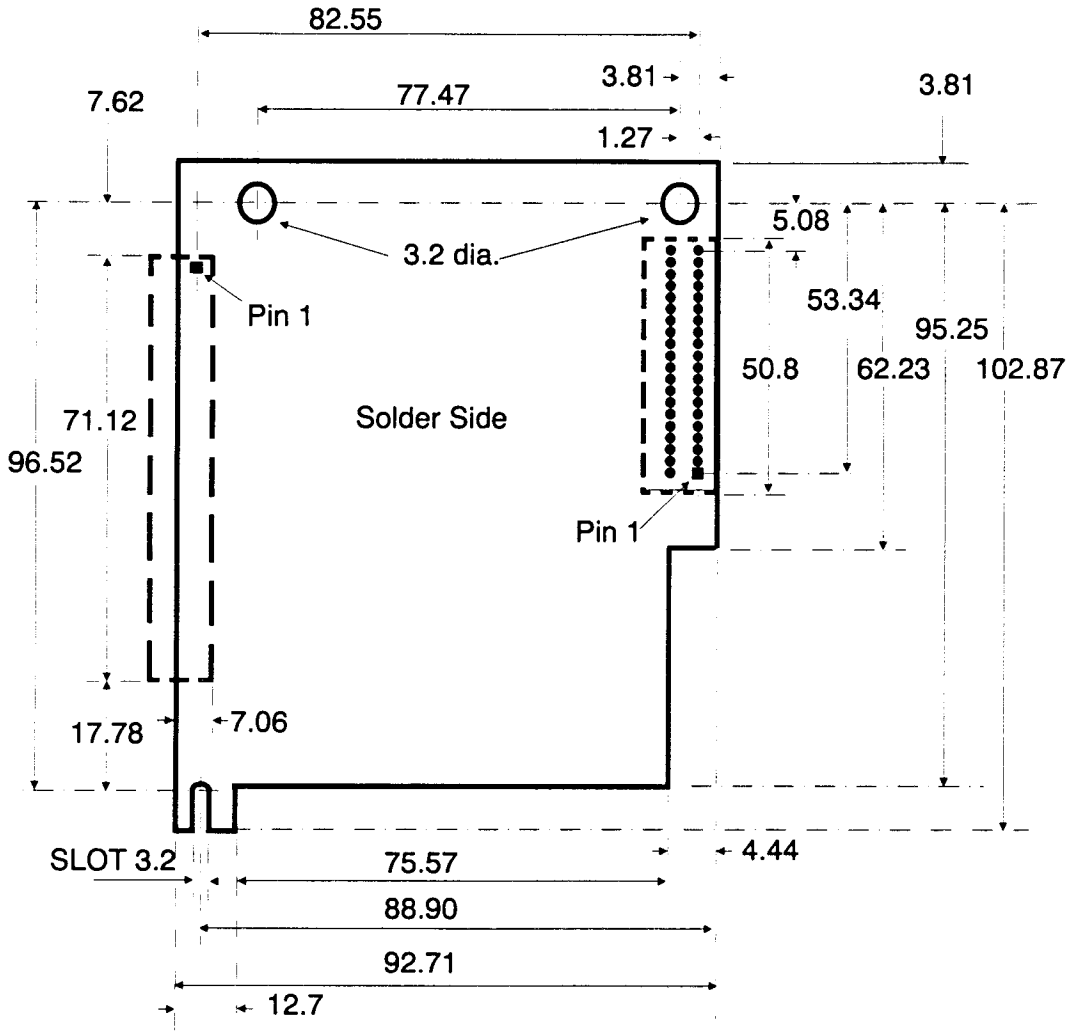
PEX Bus Connectors

The PEX board has two connectors: one to enable connection to be made to the host board, the other to the outside world. The connectors, shown as shaded areas in Figure 6, are mounted on the component side of the board.

The PEX 40-pin connector is on the right hand side of Figure 6. The diagram below shows its precise location. It is recommended that the host connector is a Berg type 76342-320 (or equivalent). The PEX board connector may be any matching type to the host socket, bearing in mind the 10.4mm (maximum) host/PEX board separation. (See Figure 7).

The second connector, mounted on the front edge of the PEX board, is a 50-way plug. When fitted to the host it protrudes through the front panel. The postioning of this plug is not as precisely defined as the other one and may be changed vertically (see Figure 5 for orientation) depending on the function of the PEX board. It may not, however, be moved horizontally - nor rotated.

Figure 5 - PEX Board Dimensions (View from Solder Side)



All measurements in millimetres — Dimension tolerances +/-0.25mm

PCB thickness = 1.6mm — Hole tolerances +0.08/-0

Figure 6 - PEX Board Positioning on the Host

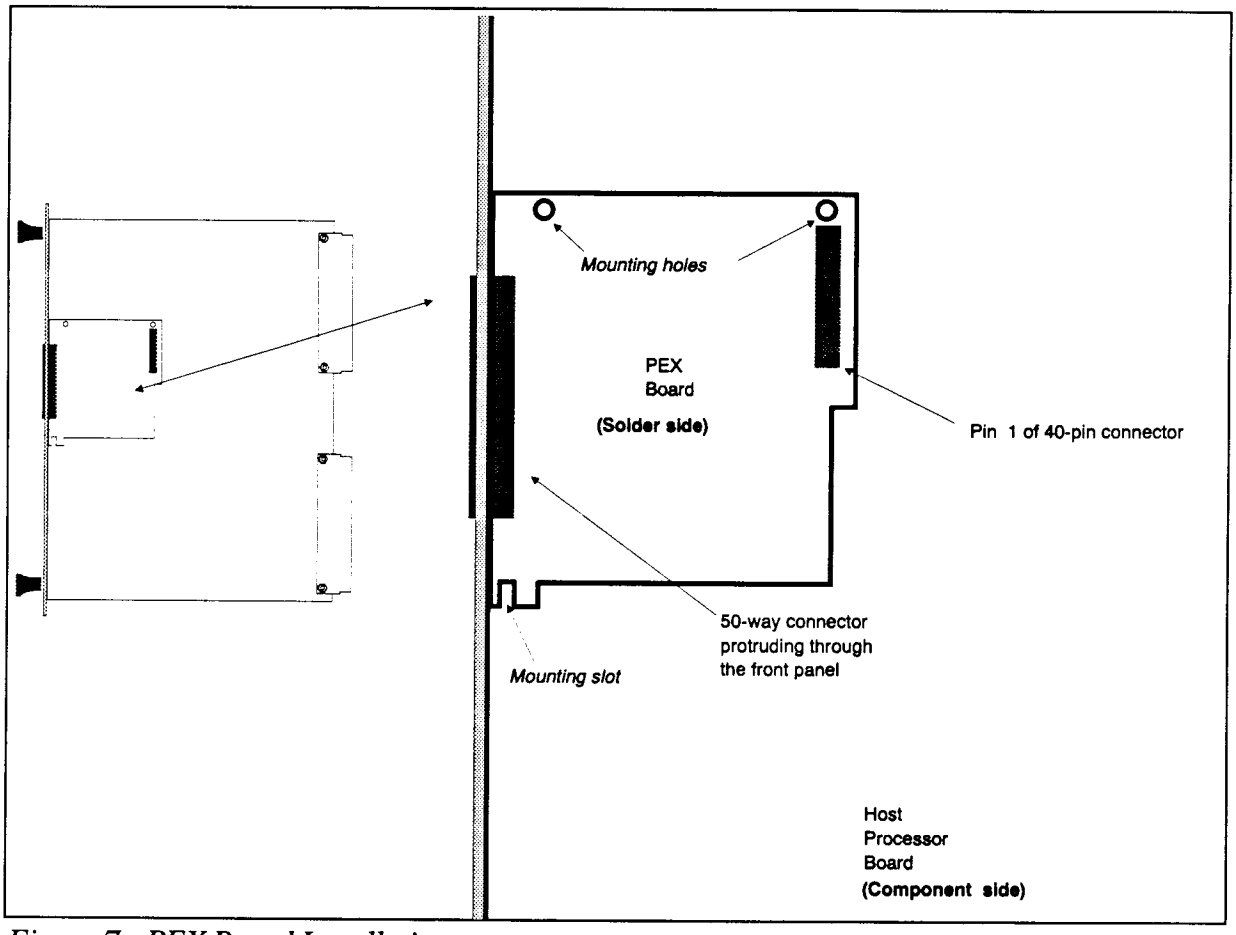
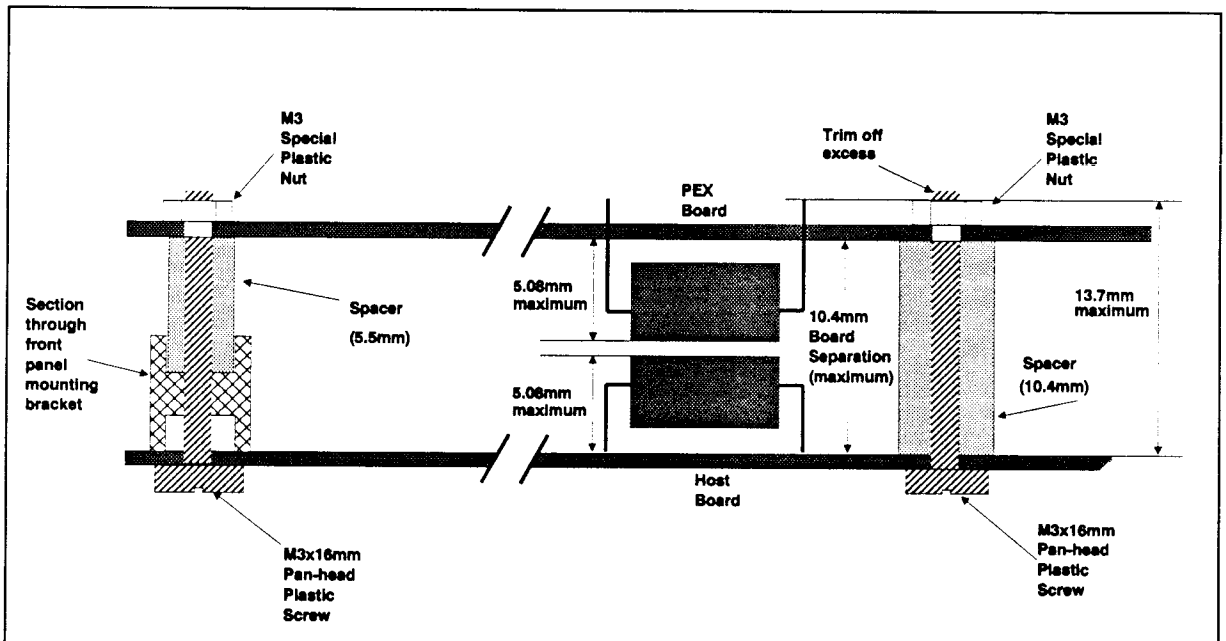


Figure 7 - PEX Board Installation



Trim screw lengths to clear adjacent VME slots after fitting special nuts

The PEX Bus uses a 40-pin connector arranged as 2 x 20 pins. The signal positions on the connector are shown in Figure 8.

Pin 27 is reserved for polarization purposes. On the host board, the socket corresponding to this position **MUST BE FILLED**. On the PEX board, this connector pin **MUST BE OMITTED** to prevent the PEX and host boards being incorrectly plugged together.

Figure 8, when applied to the host, refers to a SOCKET mounted on the component side surface of the board and shows the pin connections as seen from above.

When illustrating the PEX boards connector, Figure 8 refers to a PLUG mounted on the component side of the board viewed from the solder side of the PEX board. The pin length is to be between 7 and 9mm (ideally 8mm) thus allowing connection with a board separation of approximately 10.5mm.

Figure 8 PEX Bus Connector

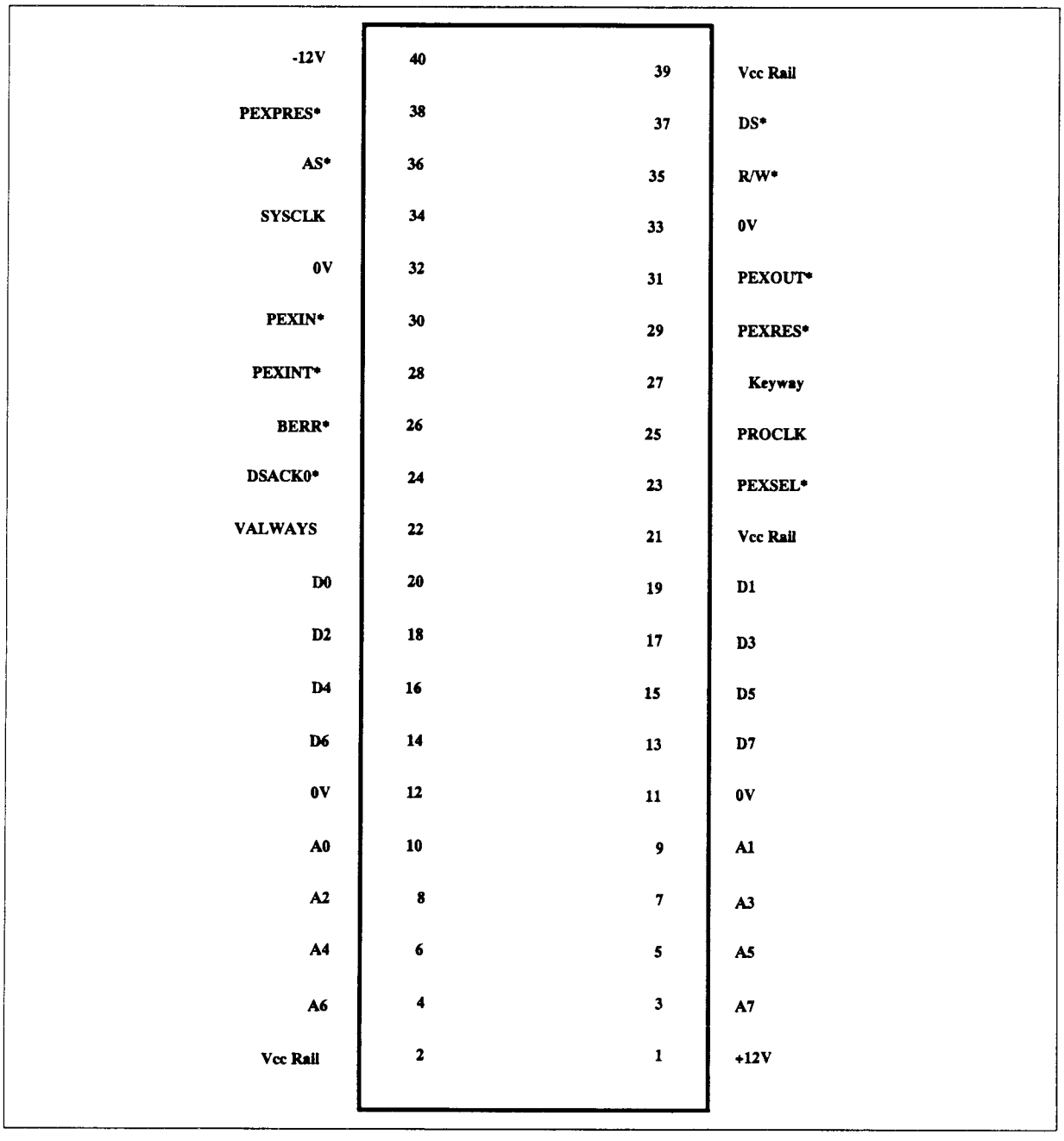
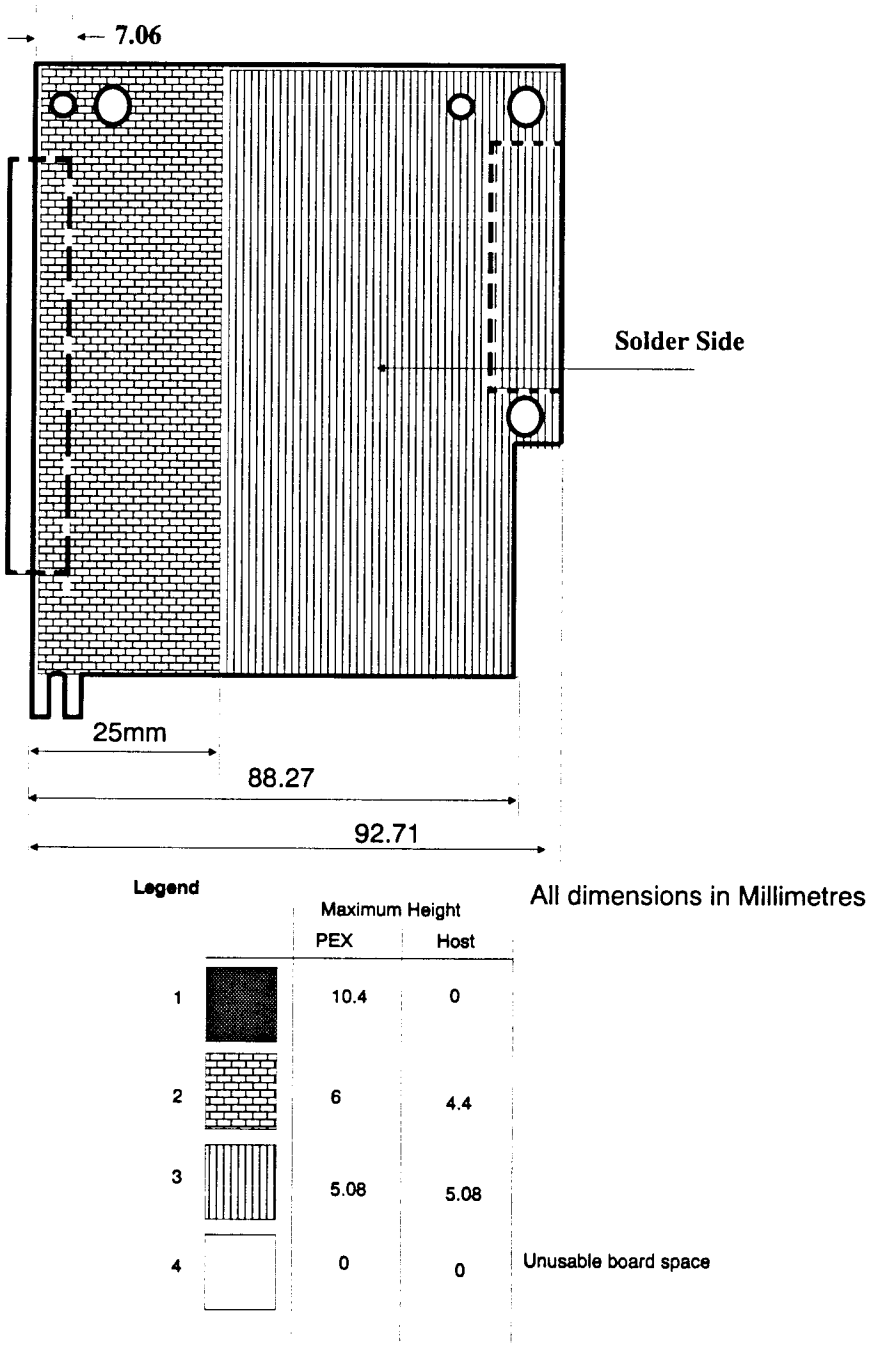


Figure 9 - Component Heights

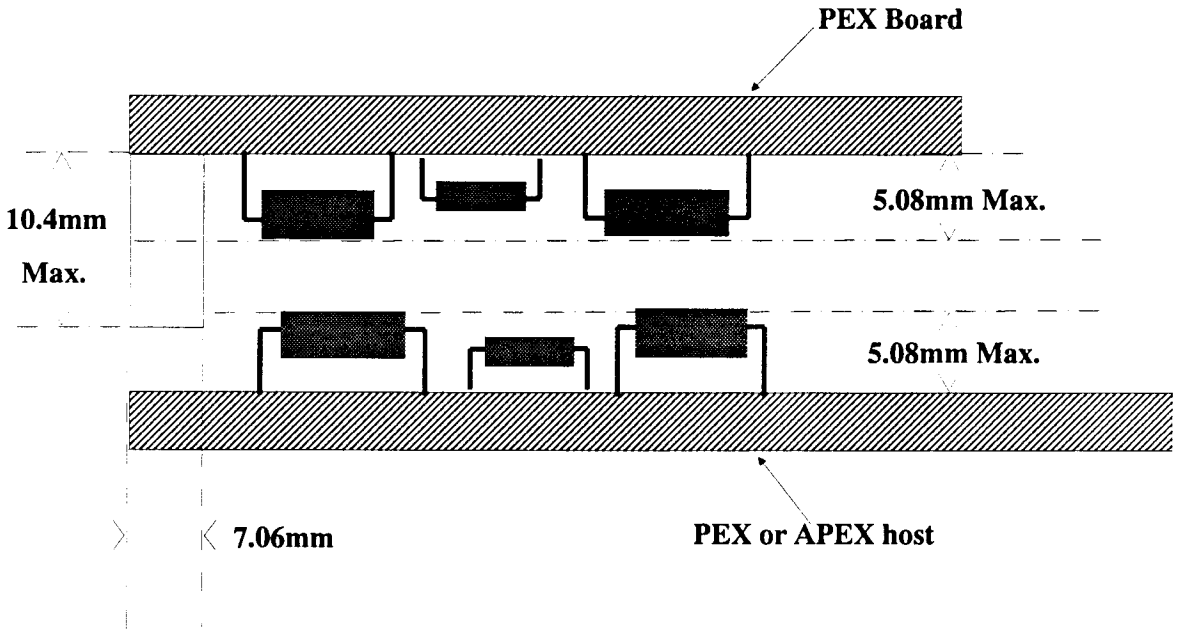


This diagram shows the component height gradient necessary to allow for a range of high profile components to be fitted to the PEX board **but only if the PEX module is fitted to an APEX host;** otherwise the height restriction is 5.08mm across the whole area (except for connector locations, as marked). See diagrams on next page.

The legend details the allowed maximum height of components on the PEX and the host boards, and the corresponding areas in which this restriction must be adhered to.

Figure 10 - Component Heights with PEX/APEX Hosts

1. Conventional PEX board, will fit any PEX host or APEX host.



2. Height profile if the PEX module is to be fitted to APEX hosts ONLY