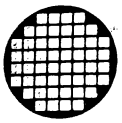


IMS B403 user guide

The IMS B403 is a dual-in-line transputer module (DITmodule) which, when fitted into an INMOS module motherboard, allows the user to evaluate the use of transputers. Alternatively it can be used in an application which requires a large amount of processing power, either on its own or as part of a network of INMOS transputers (which may include other DITmodules).

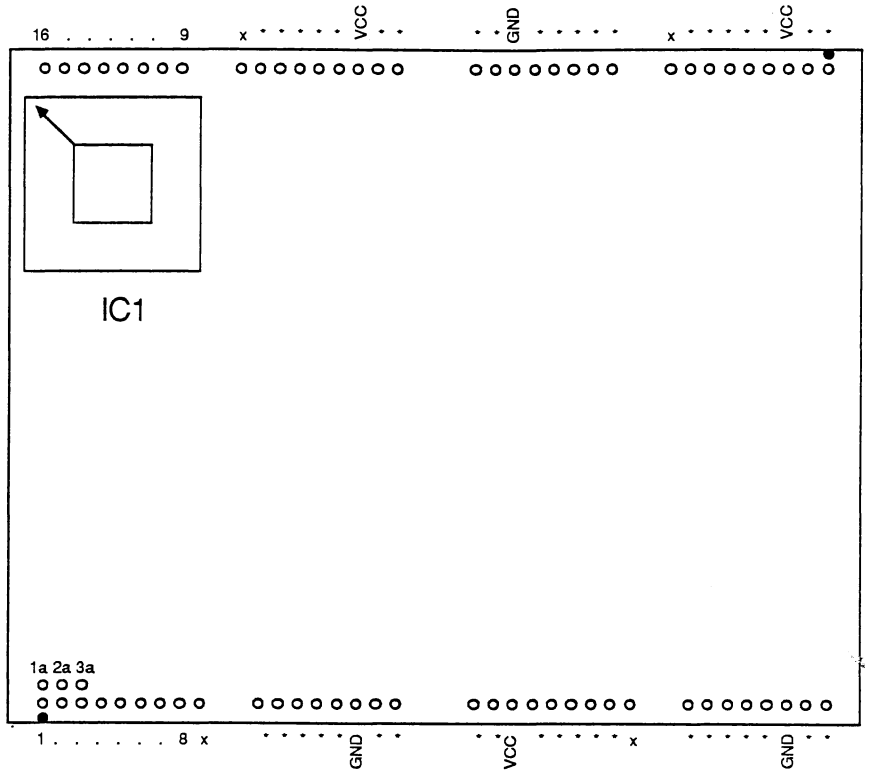
This manual should be read in conjunction with the INMOS DITmodule specification. This contains general information about DITmodules, while this manual details features specific to the B403.

The B403 has 1 Mbyte of RAM and is thus able to run the Transputer Development System (TDS). This is available as a separate product from INMOS, complete with documentation.

In order to use the B403 in a custom motherboard, the transputer reference manual and the occam programming manual will be required. These are available as separate publications from INMOS.

The B403 is a size4 DITmodule, dimensions 4.35 x 3.5 inches (110.5 x 88.9mm). A diagram is shown below (actual size).

Fig.1 - B403 mechanical drawing



See the DITmodule specification for more detailed dimensions.

The pinout is as follows:

Standard pins:

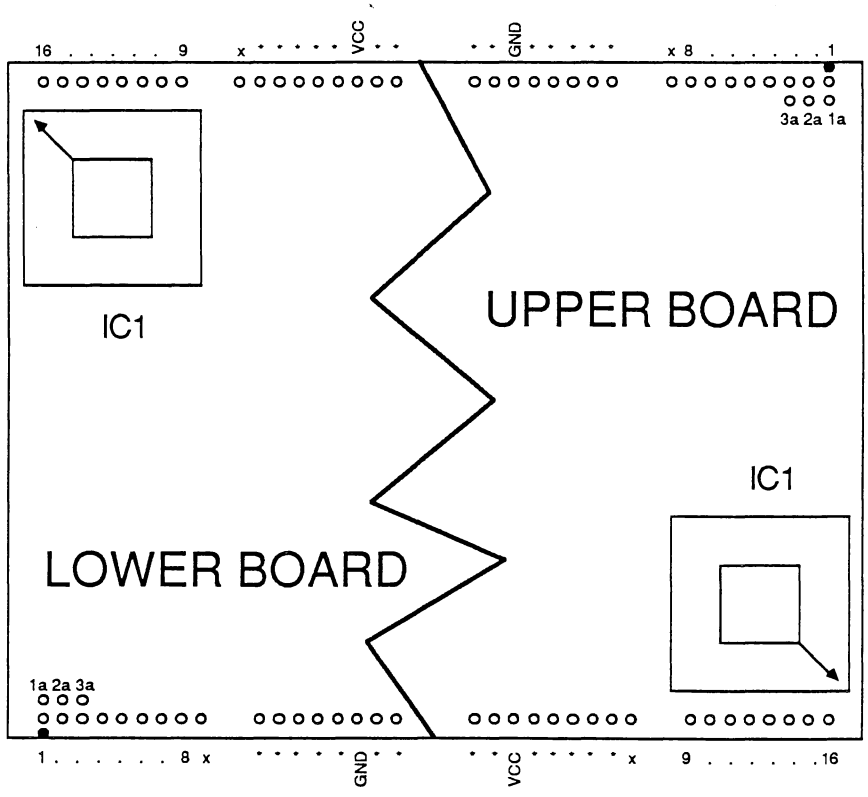
1	Link2out	Link3in	16
2	Link2in	Link3out	15
3	VCC	GND	14
4	Link1out	Link0in	13
5	Link1in	Link0out	12
6	LinkSpecialA	notError	11
7	LinkSpecialB	Reset	10
8	Clockin (5 MHz)	Analyse	9
x	GND		
*	No connection on B403		

Special pins:

1a	SubSystemNotError
2a	SubSystemReset
3a	SubSystemAnalyse

Only 19 pins at one end of the board are used for signals; others are left unconnected except for power pins. This allows two boards to be stacked on top of each other with the uppermost board rotated through 180 degrees:

Fig.2 - Double stacking of B403



With this arrangement, the 16 signals from the uppermost board are connected to 16 unconnected pins on the lower board. The pins on which the two groups of signals appear are shown in fig.2, together with the 32 remaining unused pins.

Note that the subsystem port on the upper board cannot be used because of the components present on the lower board.

2.1 Location of memory

The B403 has 1 Mbyte of external RAM appearing at the following addresses (the '#' sign indicates a hexadecimal number):

B403 with T414

	Hardware byte address	Occam word address
From:	#80000800	#00000200
To:	#801007FF	#000401FF

B403 with T800

	Hardware byte address	Occam word address
From:	#80001000	#00000400
To:	#80100FFF	#000403FF

The B403 with T414 has internal RAM occupying the first 2 Kbytes of address space, whereas internal RAM occupies the first 4 Kbytes on the B403 with T800. See the memory map in appendix A.

2.2 Use of standard DITmodule signals

A DITmodule can be regarded as a transputer with extra RAM attached and some of its signals appearing on the pins 1-16. A few of these signals are slightly different from the transputer specification as follows:

notError (pin 11) is an open collector signal. It is driven low when there is an error; otherwise it is allowed to float. This enables the error signals on many modules to be wire-ORed together.

LinkSpecialA and **LinkSpecialB** (pins 6 and 7): when these are both low, the transputer links operate at 10 Mbits/sec. When they are both high, the links operate at 20 Mbits/sec. Other states of these pins are reserved for future enhancements.

All link signals: These obey a protocol identical to that described in the transputer reference manual, but there are differences in electrical characteristics. The link inputs have pull-down resistors to ensure that there is no activity on them when they are not connected. Diodes are also included for protection against electrostatic discharge. Link outputs have resistors connected in series for matching to a 100 ohm transmission line. This is all shown in the circuit diagram (appendix D).

All other DITmodule pins function in the same way as the corresponding transputer signals. See the transputer reference manual for details.

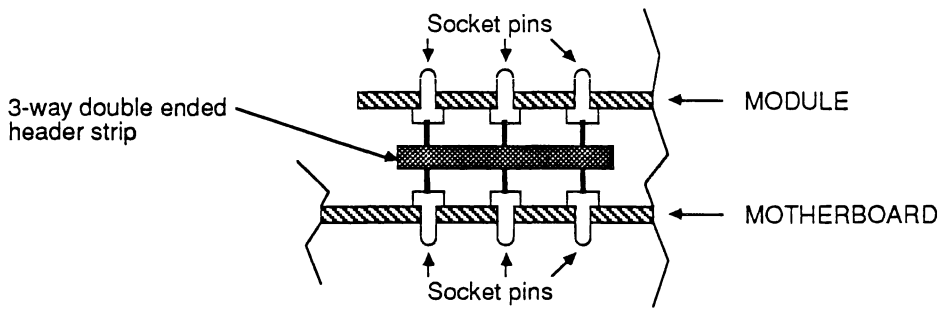
2.3 Special signals

The B403 has a subsystem port in addition to the usual DITmodule signals. This enables the DITmodule to reset or analyse a subsystem of other DITmodules and/or boards. The polarity of these signals is the same as that of the Reset, Analyse and notError standard DITmodule signals. Therefore the B403 subsystem can drive other DITmodules on the same motherboard with no intermediate logic. SubSystemReset and SubSystemAnalyse must go through inverting buffers if they are to drive a subsystem off the motherboard.

2.3.1 Physical connections

The subsystem port appears on zero profile socket pins located 0.1 inches inside module pins 1-3, but soldered in upside-down. See the module pinout (fig.1) for details. The motherboard will also have three similar socket pins, but soldered in the correct way up. The connection between the module and the motherboard is then made by a double ended header strip. See fig.3.

Fig.3 - Subsystem port connections



2.3.2 Address locations

The registers which control the subsystem port are located at the following addresses:

Register	Hardware byte address	Occam word address
SubSystemReset (write only)	#00000000	#20000000
SubSystemAnalyse (write only)	#00000004	#20000001
notSubSystemError (read only)	#00000000	#20000000

Setting bit 0 in either the reset or the analyse registers asserts the corresponding signal. Similarly, clearing bit 0 deasserts the signal. When an error occurs in the subsystem, bit 0 of the error location becomes set.

Occam locations #20000002 and #20000003 are unused. The SubSystemReset register is repeated at locations #20000004, #20000008 etc., i.e. every fourth word location in the positive address space. Similarly the SubSystemAnalyse register repeats at #20000005, #20000009 etc. See the memory map in appendix A.

2.4 Transputer and memory speed

The board has been designed to allow for many speed variants of both memory and transputer and is available in several such variants. Alternatively it can be user-modified to change the external memory cycle time and/or the transputer speed.

Provision has been made for transputer speeds of 15, 20, 22, 25 and 30 MHz. These different speeds are selected by the position of the surface mounted resistors R23 and R24 - details are shown in appendix B, fig.5.

The transputer generates programmable strobes which can be used to interface to external memory. The resulting flexibility enables a faster configuration to be used if the user wishes to upgrade to faster memory. Alternatively it may be necessary to lengthen the external memory cycle if the transputer is replaced by another with a shorter clock cycle. Full details of how to program the strobes are given in the transputer reference manual.

The B403 provides several preset configurations which are selected by cutting a track on the board and adding a wire link. The information on the various configurations available is shown in appendix C (figs.6-11) together with the links that need to be made in order to select them.

3.1 Installation

If the B403 has been purchased as a separate entity, it has to be plugged into the particular motherboard being used. Precautions against static damage should be taken, hence it is recommended that the following procedure is used:

1) Keep the B403 in conductive material while it is not plugged in.

2) Before touching the B403, touch the conductive material.

3) While still touching the conductive material, touch one of the ground pins on the B403. Then pick up the B403.

4) Check that none of the B403 pins have been damaged.

5) If the subsystem signals are required, plug the 3-way header strip into the solder-side sockets on the B403.

5) Touch chassis ground on the motherboard.

6) Plug the B403 into the motherboard. The spot which marks pin 1 on the module (see fig.1) and on the motherboard (if it is an INMOS type) should be used for orientation.

7) Should it be necessary to unplug the B403, it is advised that it is gently levered out while keeping it as flat as possible. This precaution helps to prevent damage to the pins.

3.2 Testing

If the B403 is being used in an INMOS module motherboard, then the test software provided with that motherboard should be used. Otherwise it will have to be user-provided or obtained as a separate item from INMOS.

3.3 Running programs

The B403 has no ROM on board, so it must be booted with program code down one of its links. See the transputer reference manual for details on booting.

The B403 has enough memory to run the Transputer Development System (TDS) and can therefore be used to develop occam programs. Once these programs have been run and tested on the B403, the code can be passed to a network of transputers by means of links. This network could be made up of other INMOS modules, or it could be built from transputer chips on a user-designed board. See the occam reference manual for more information on programming.

The TDS is available as a separate product from INMOS.

Fig.4 - Memory map

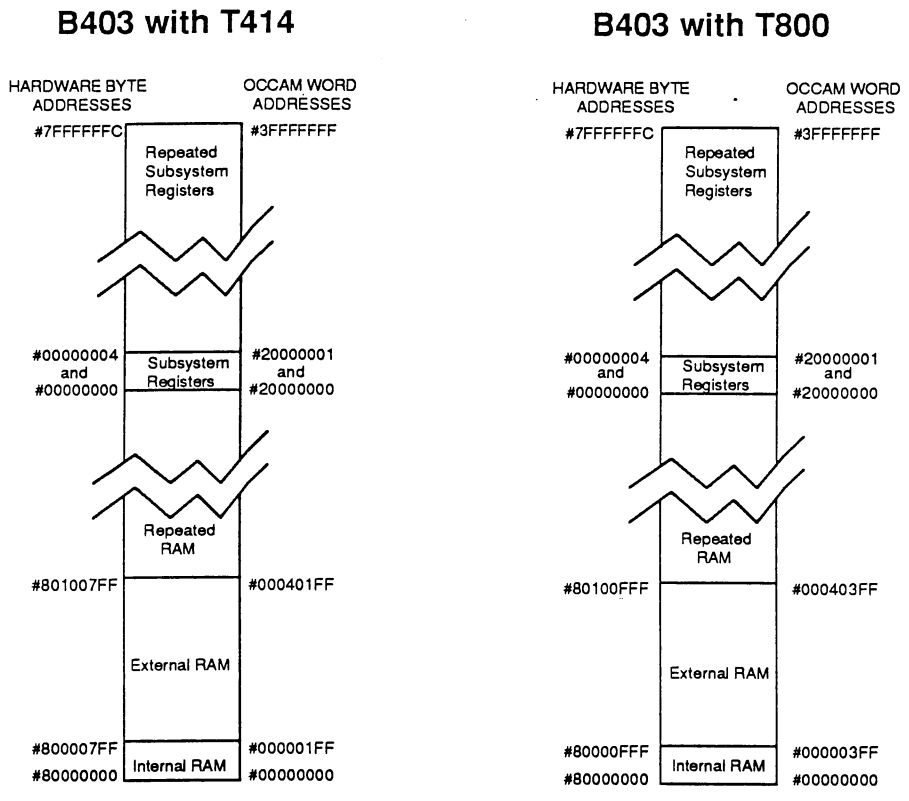
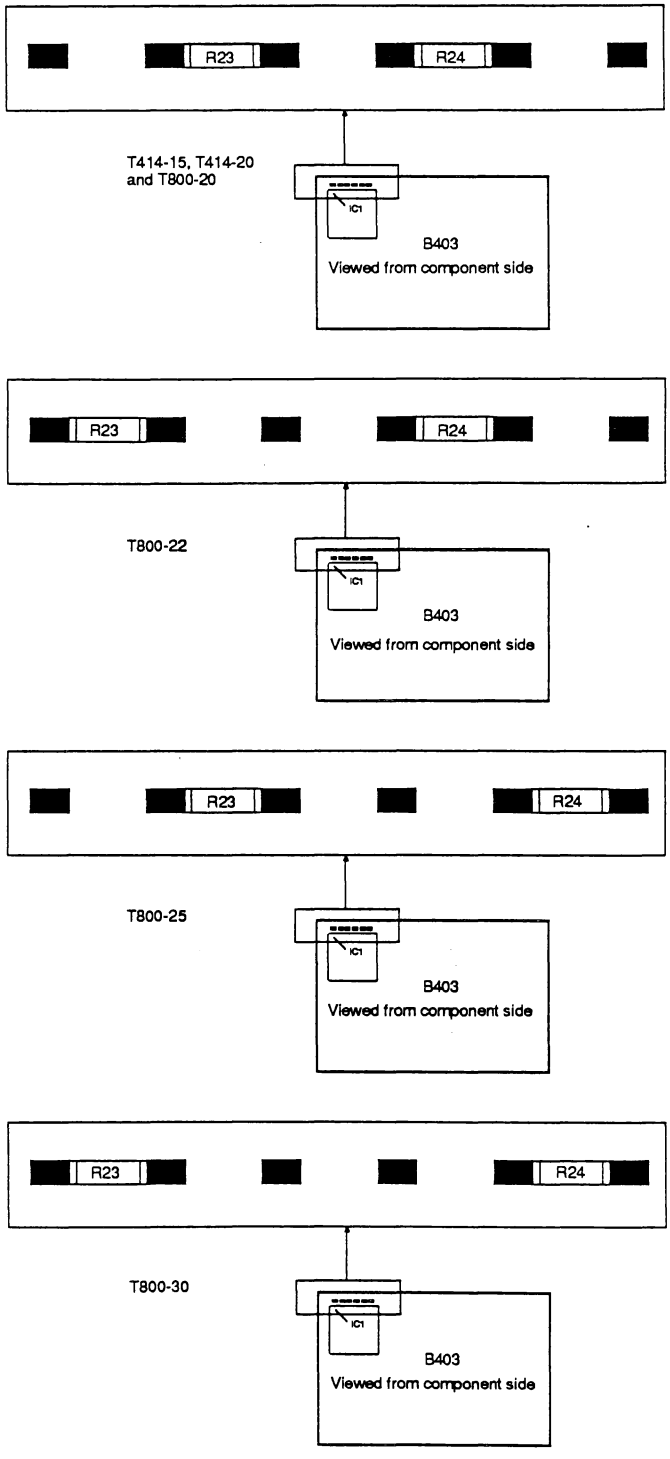


Fig.5 - Resistor mounting details for selecting processor speed



This appendix explains how to alter the external memory cycle time of the transputer. The following points should be noted:

1) The default memory configuration runs in 4 processor cycles and is labelled 'IV' on the board. It is shown in fig.7.

2) The configurations labelled 'IVb' and 'Vb' (figs.10 and 11) are available only on boards fitted with T800 transputers.

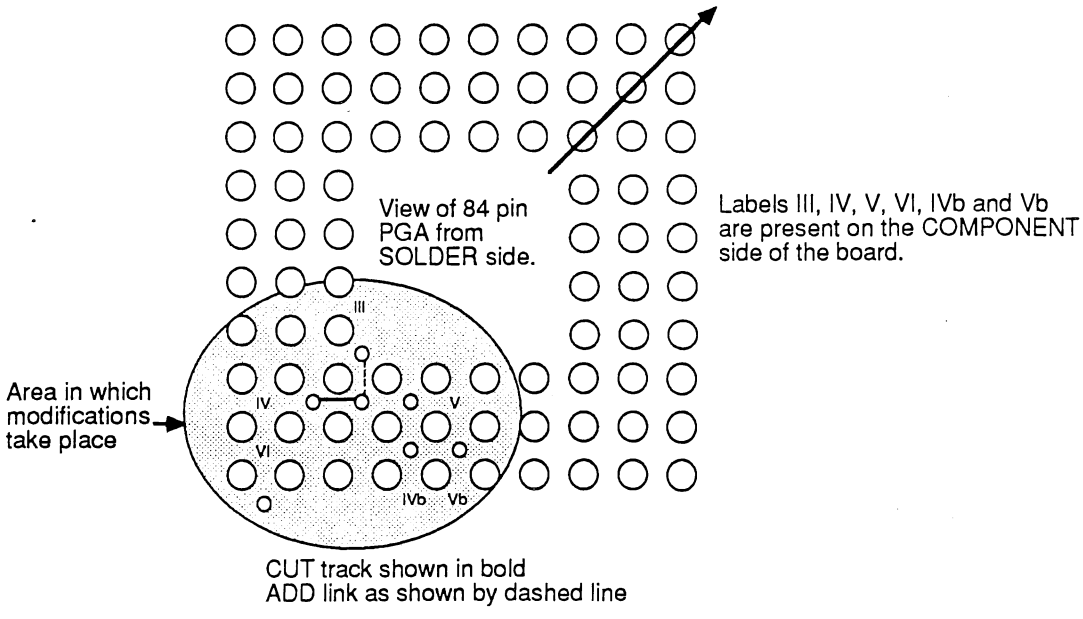
3) The divisions on all the timing diagrams represent half a clock period. For example, using a 20 MHz transputer, one division equals 25 nS.

4) In all the configuations the strobe **notMemS1** is used as **RAS**, while **notMemS3** is used for **CAS**.

5) Note that all the timing diagrams shown are idealised, i.e. they do not take skew or gate delays into account. Refer to the circuit diagram (appendix D) if any modifications to the B403 are to be made.

Fig.6 - Memory configuration III (3 cycles)

Modifications required:



Timing diagram:

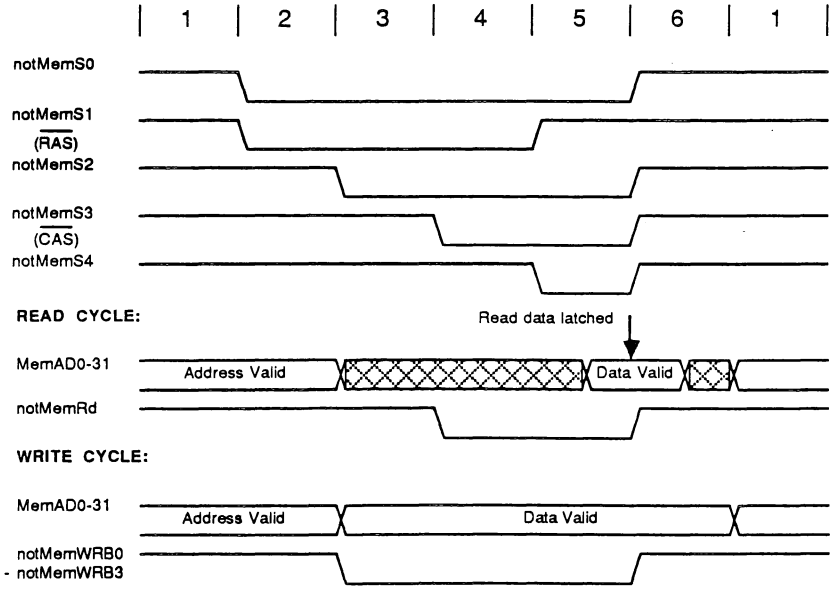


Fig.7 - Memory configuration IV (4 cycles)

Modifications required: None

Timing diagram:

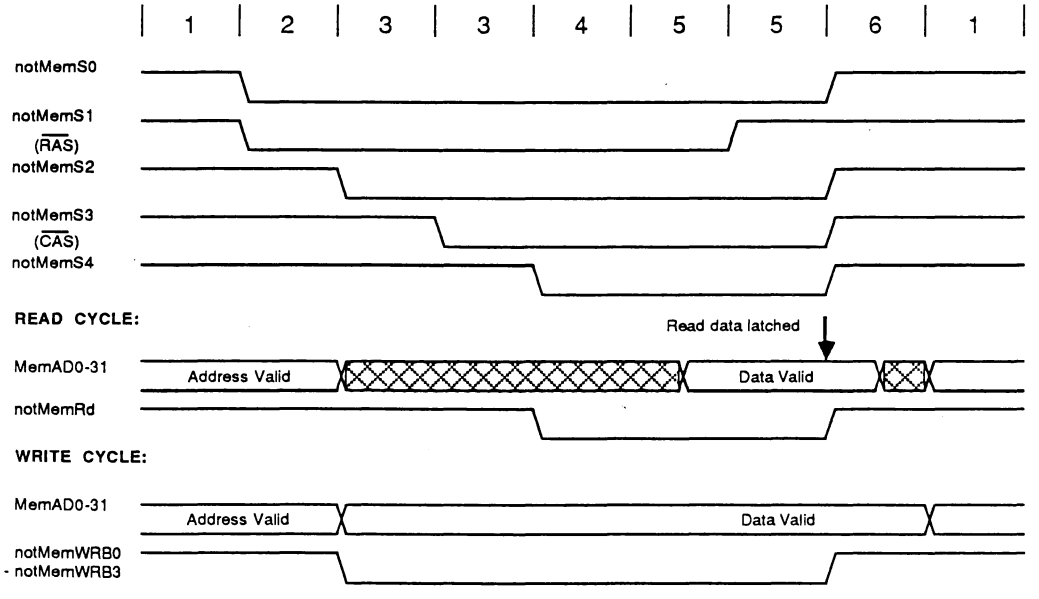
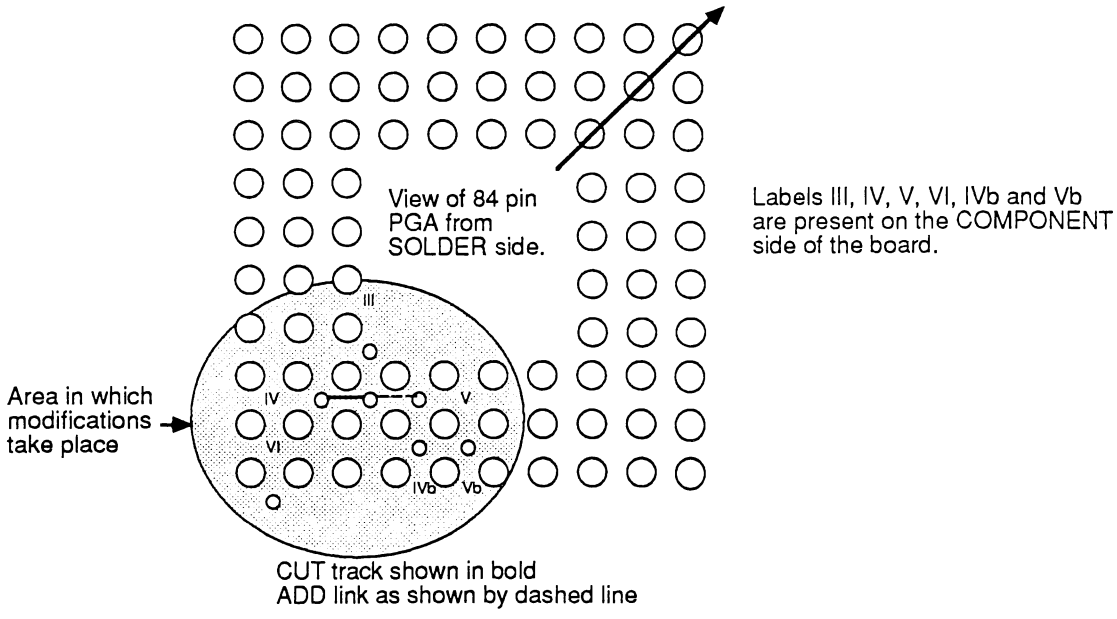


Fig.8 - Memory configuration V (5 cycles)

Modifications required:



Timing diagram:

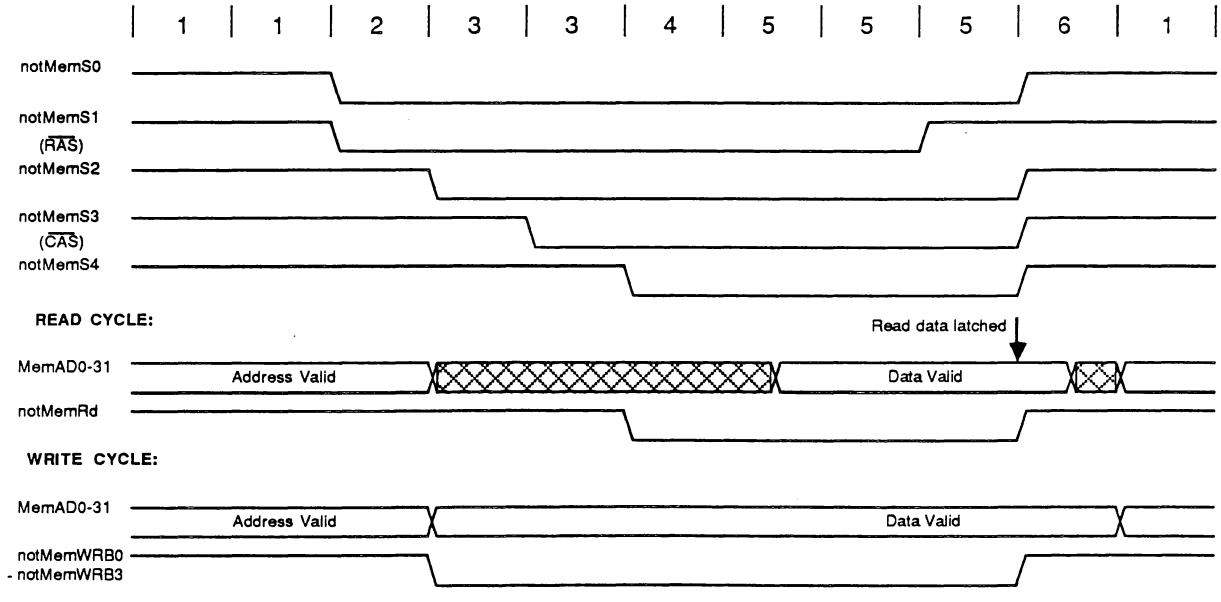
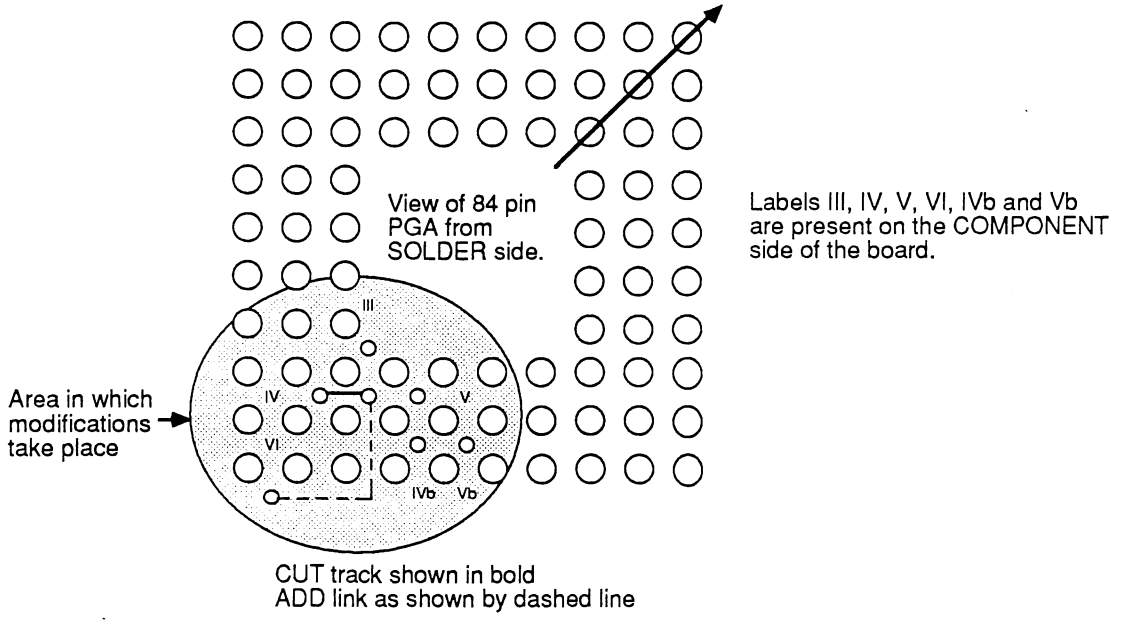


Fig.9 - Memory configuration VI (6 cycles)

Modifications required:



Timing diagram:

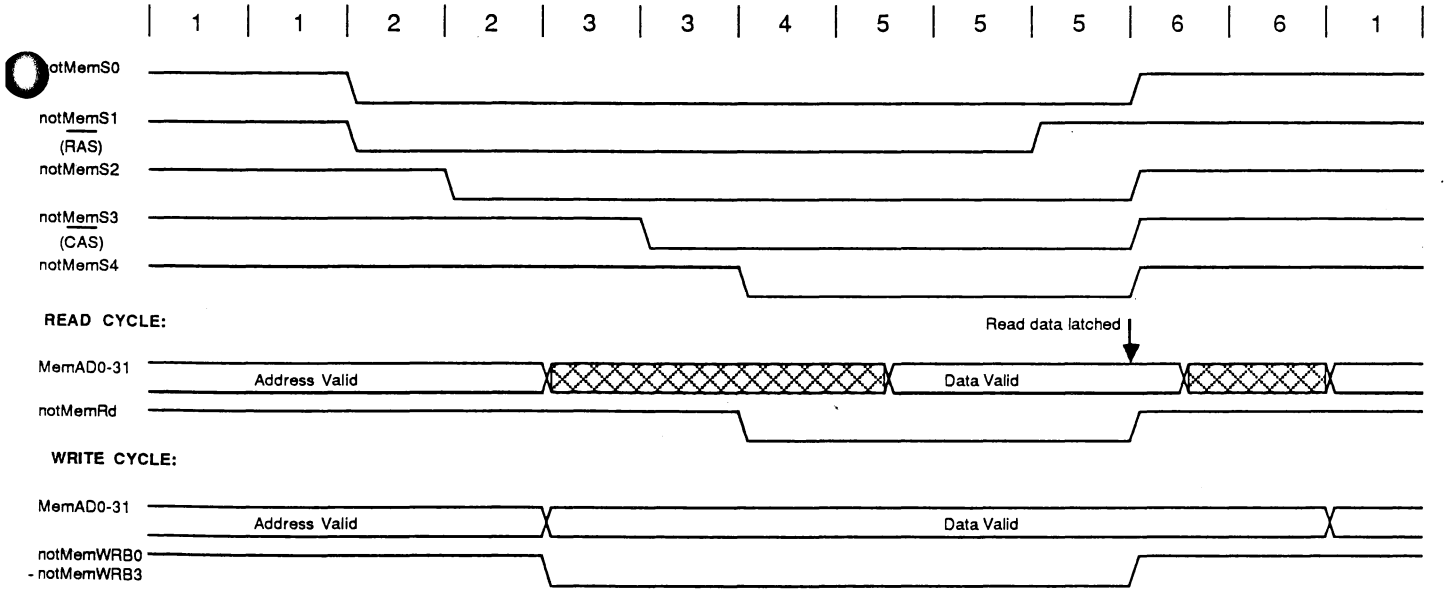
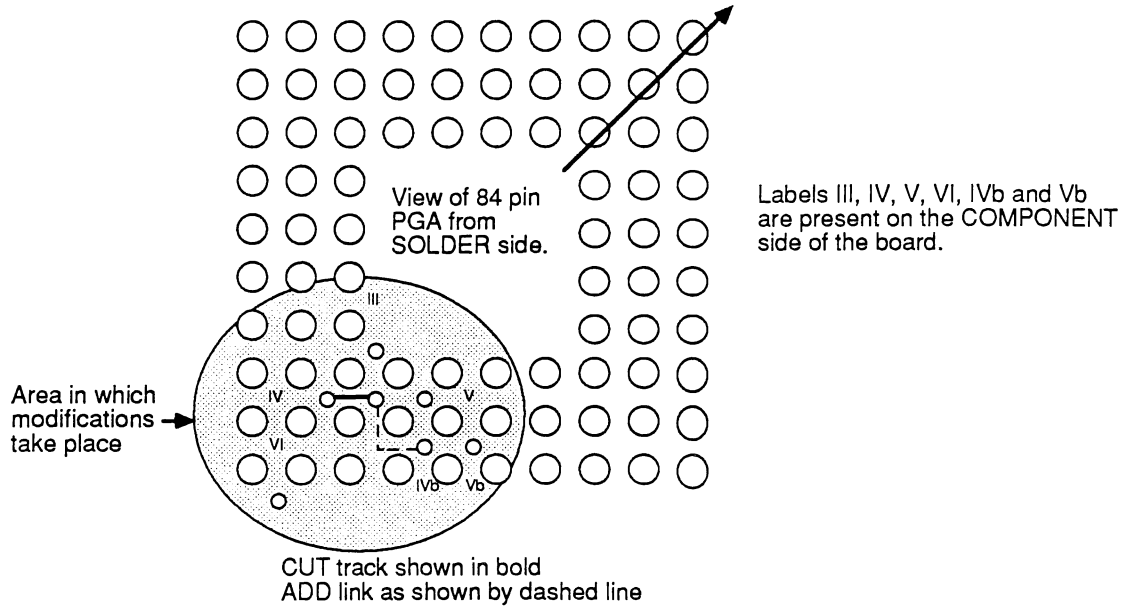


Fig.10 - Memory configuration IVb (4 cycles - T800 only)

Modifications required:



Timing diagram:

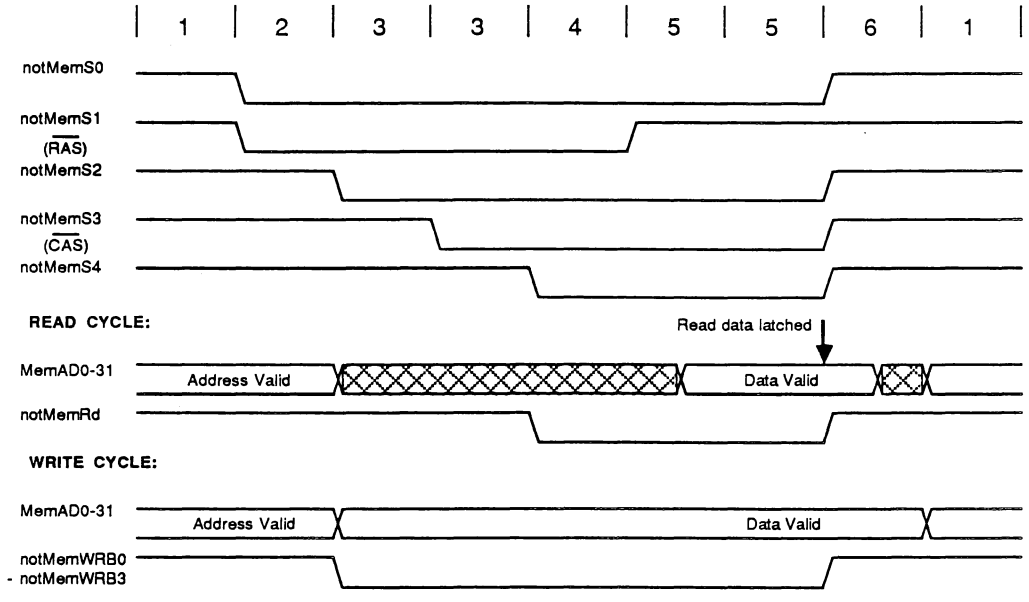
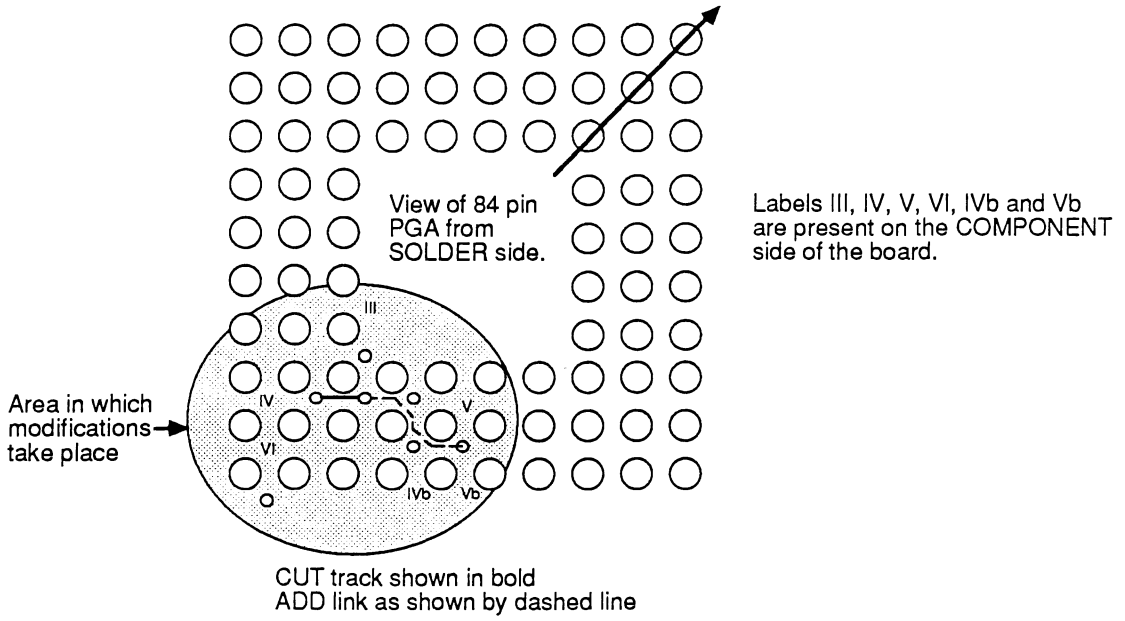


Fig.11 - Memory configuration Vb (5 cycles - T800 only)

Modifications required:



Timing diagram:

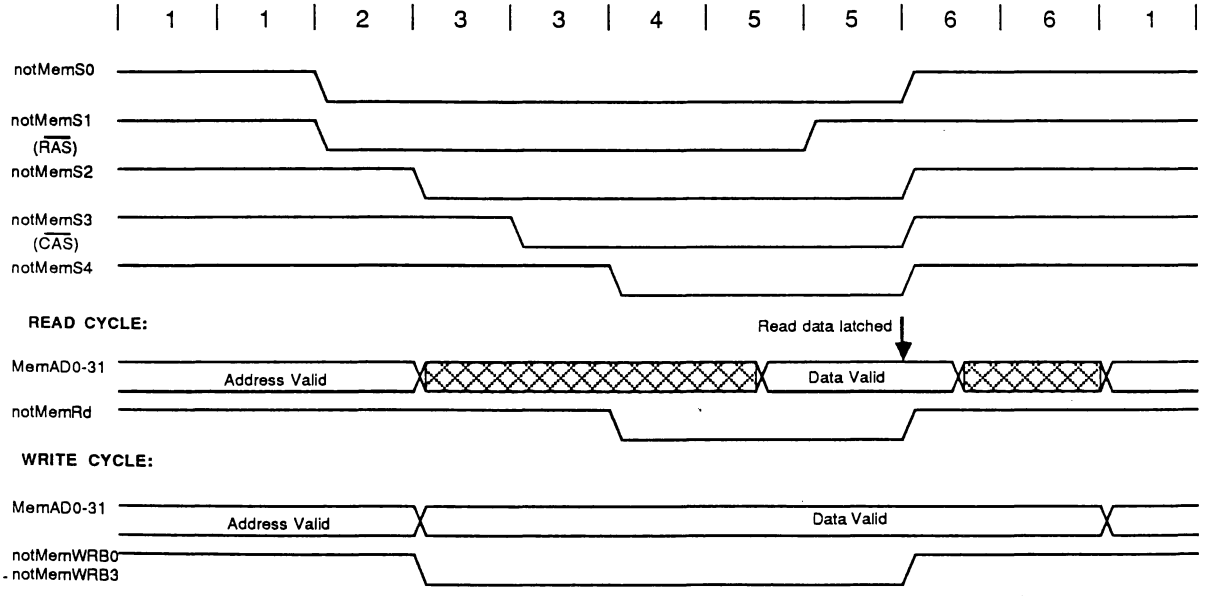


Fig.12 - Transputer, memory drivers and subsystem logic

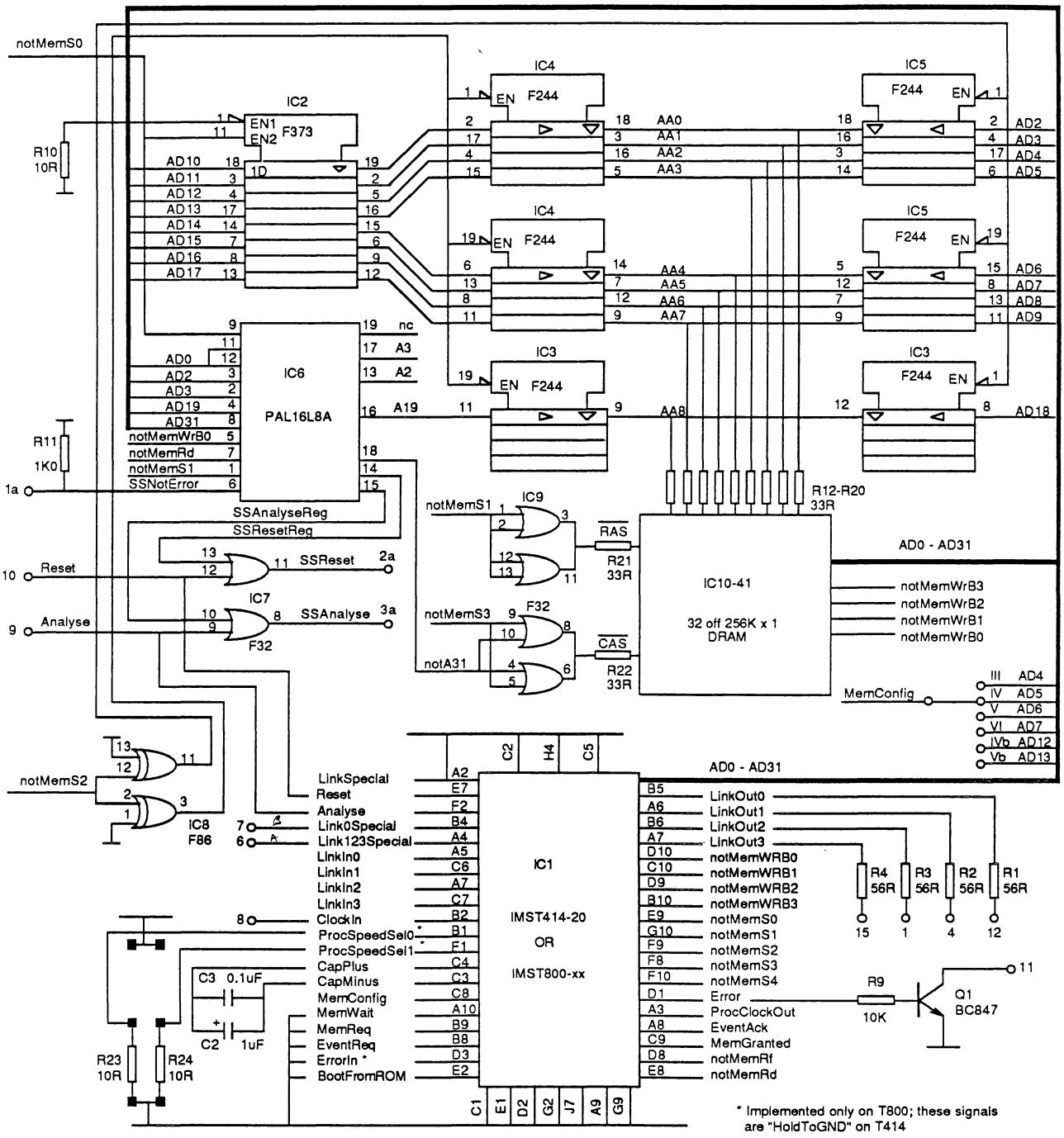
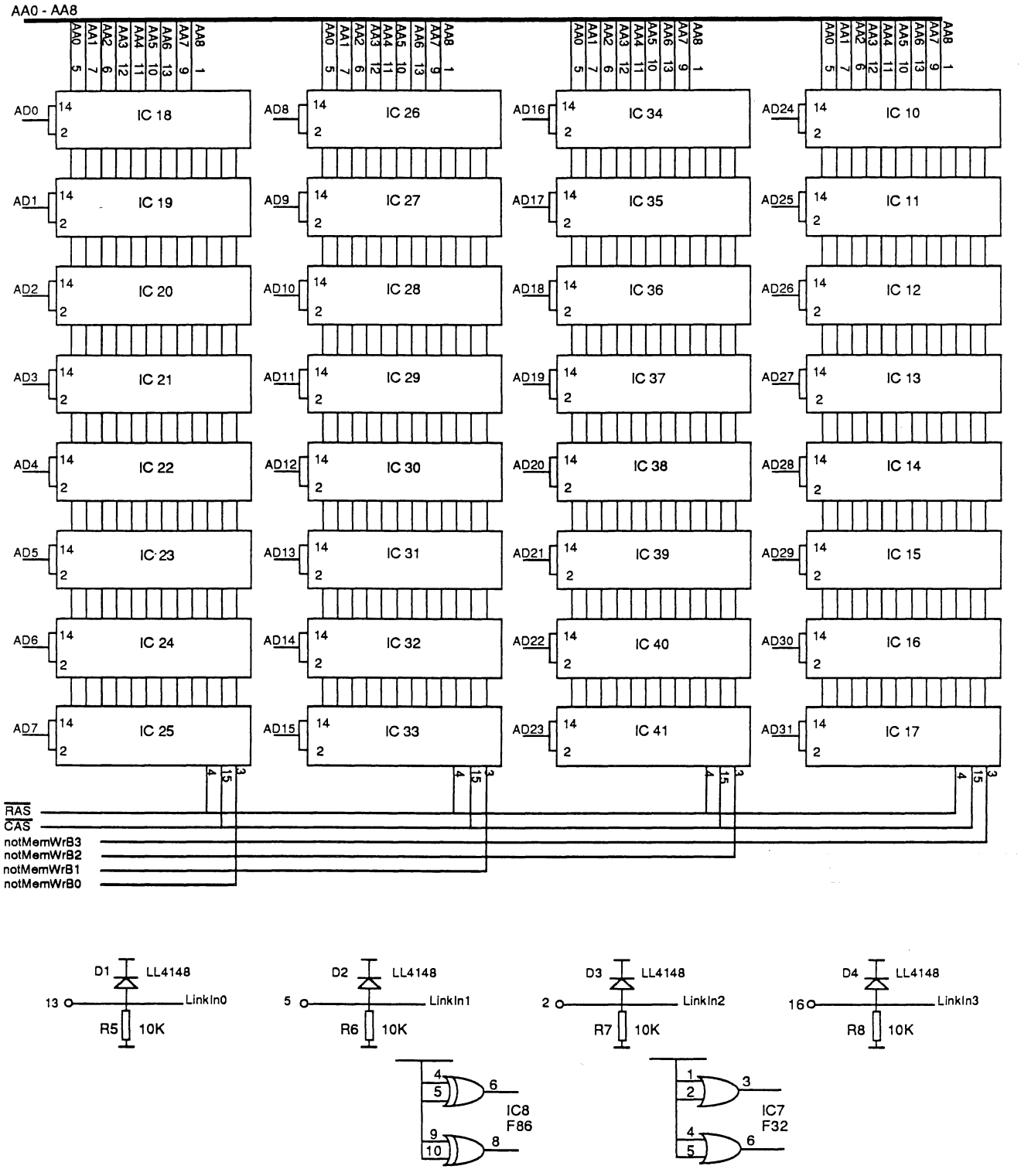


Fig.13 - Memory array, link protection and unused gates



```
*************************
* PAL TYPE: 16L8A *
*************************


/** Pin Declarations **/

PIN 1 = notMemS1 ;
PIN 2 = AD3 ;
PIN 3 = AD2 ;
PIN 4 = AD19 ;
PIN 5 = notMemWRB0 ;
PIN 6 = !SSNotError ;
PIN 7 = notMemRd ;
PIN 8 = AD31 ;
PIN 9 = notS0 ;
PIN 11 = inAD0 ;
PIN 12 = outAD0 ;
PIN 13 = LatchedA2 ;
PIN 14 = SSResetReg ;
PIN 15 = SSAnalyseReg ;
PIN 16 = LatchedA19 ;
PIN 17 = LatchedA3 ;
PIN 18 = !LatchedA31 ;
PIN 19 = nc ;

FIELD Select = [LatchedA2..LatchedA3] ;


/** Logic Equations **/

outAD0 = SSNotError ;
outAD0.OE = Select:[0] & !LatchedA31 & !notMemRd ;

LatchedA2 = AD2 & notS0
# LatchedA2 & !notS0
# AD2 & LatchedA2 ;
LatchedA3 = AD3 & notS0
# LatchedA3 & !notS0
# AD3 & LatchedA3 ;
LatchedA19 = AD19 & notS0
# LatchedA19 & !notS0
# AD19 & LatchedA19 ;
LatchedA31 = AD31 & notS0
# LatchedA31 & !notS0
# AD31 & LatchedA31 ;

ResetClock = Select:[0] & !LatchedA31 & !notMemS1 & !notMemWRB0 ;
SSResetReg = inAD0 & ResetClock
# SSResetReg & !ResetClock
# inAD0 & SSResetReg ;

AnalyseClock = Select:[4] & !LatchedA31 & !notMemS1 & !notMemWRB0 ;
SSAnalyseReg = inAD0 & AnalyseClock
# SSAnalyseReg & !AnalyseClock
# inAD0 & SSAnalyseReg ;
```

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February 1987

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