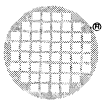

The design of a high resolution graphics system using the IMS G300 Colour Video Controller

Dave Japp
INMOS Bristol

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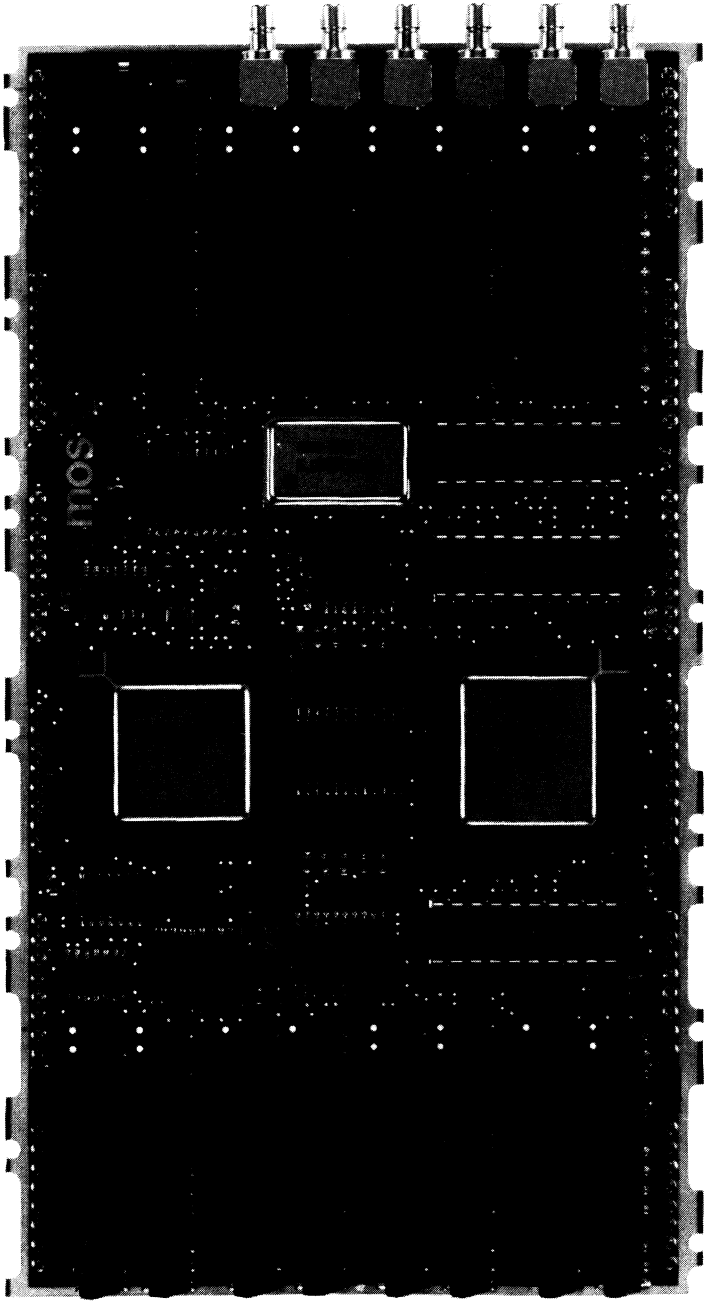
Contents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1 Introduction

The chip count in graphic systems was substantially reduced in 1985 when INMOS introduced the IMS G170. This device integrates the functions of colour look-up table, digital to analogue converters and micro interface into a single package.

The IMS G300 Colour Video Controller (CVC) is a new addition to the graphic support devices currently produced by INMOS. The G300 CVC integrates colour look-up, data conversion functions with a video timing generator and a Video RAM interface. This level of integration not only increases system performance, but reduces the overall chip count, simplifying design and reducing cost.

This technical note describes the design and implementation of a general purpose graphics system which enables users to evaluate the IMS G300 CVC.

2 The IMS G300 colour video controller

The IMS G300 CVC provides all the necessary functions for controlling real time operation of a raster scan video system.

The micro-port is used for programming both the video timing generator screen description registers and the colour look-up table. It appears as a block of memory occupying 1/2Kword of address space, an additional capability allows the device to operate in byte-wide or word-wide modes, simplifying the interface to various host processors.

The video timing generator (VTG) is a programmable finite state machine which is programmed by the user to suit the particular requirements of the display. When configured to free run it provides either composite or separate synchronisation signals for the monitor and a composite blank to the DACs. In the slave mode the VTG accepts external synchronising signals (HSync and VSync) which may be from another G300 CVC, which gives the potential for multiple, synchronous video systems. The VTG runs at one quarter of the video dot rate.

The VRAMs are supported by a screen refresh mechanism which transfers data via DMA, permitting a seamless mid-line update of the screen. The shift registers within the VRAMs can be made to behave as though they are infinitely long, the pixel flow being controlled by starting and stopping the pixel shift clock at the appropriate times. This enables an efficient use of memory since the screen line length can be made independent of the VRAM shift register length without the use of external strobe generation hardware.

The pixel port on the G300 CVC is 32 bits wide and has two modes of operation. In mode 1 the 32 bit word represents four byte-wide pixel addresses; these are accelerated to the full dot rate before addressing the look-up table (LUT). The 24 bits produced by the LUT are then sent to the DACs for display, allowing 256 colours displayable from a palette of 16 million. This mode allows the VRAMs to run at a relatively low frequency, so that in a 120 MHz system the VRAMs are cycled at 30 MHz. In mode 2 the pixel data is supplied at full video rate. The top byte of the 32 bit word is ignored, the remaining 24 bits are then sent directly to the DACs for display giving a potential of 16 million colours displayable at one time.

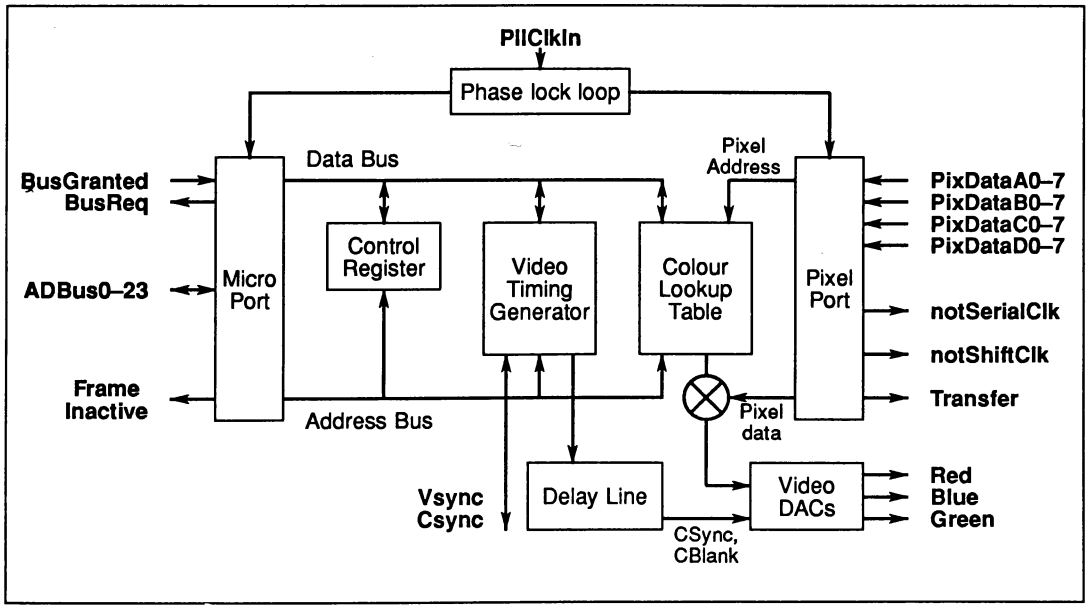


Figure 2.1 IMS G300 Block Diagram

3 IMS G300 TRAM design

3.1 Introduction

The IMS G300 CVC Graphics TRAM implements a complete high performance graphics subsystem. The frame store consists of 2 Mbytes of dual ported Video RAM which supports displays of arbitrary resolution at 8 bit/pixel. The resolution of the system is only limited by the CVCs maximum dot rate and the access time of the serial port on the VRAM. In this particular application the dot rate is up to 110 MHz, the speed of the CVC. Possible screen sizes include 1280 x 1024 8 bit/pixel, 1024 x 1024 8 bit/pixel double buffered and lower resolutions, for example 640 x 480, with multi-buffering. The CVC is configured by the on board IMS T800 which is provided with 2 Mbytes of 200ns cycle DRAM. This store is available for screen manipulation workspace and general program memory. The processor can be used to implement graphics primitives directly or as an intelligent channel receiving data from an array via its four bidirectional links at data rates of up to 10 Mbytes/sec. This makes the TRAM useful for applications as diverse as an add-on accelerator to a PC or Macintosh, as a part of an embedded system in industrial control, for instance or as a graphics output for a 3D graphical supercomputer.

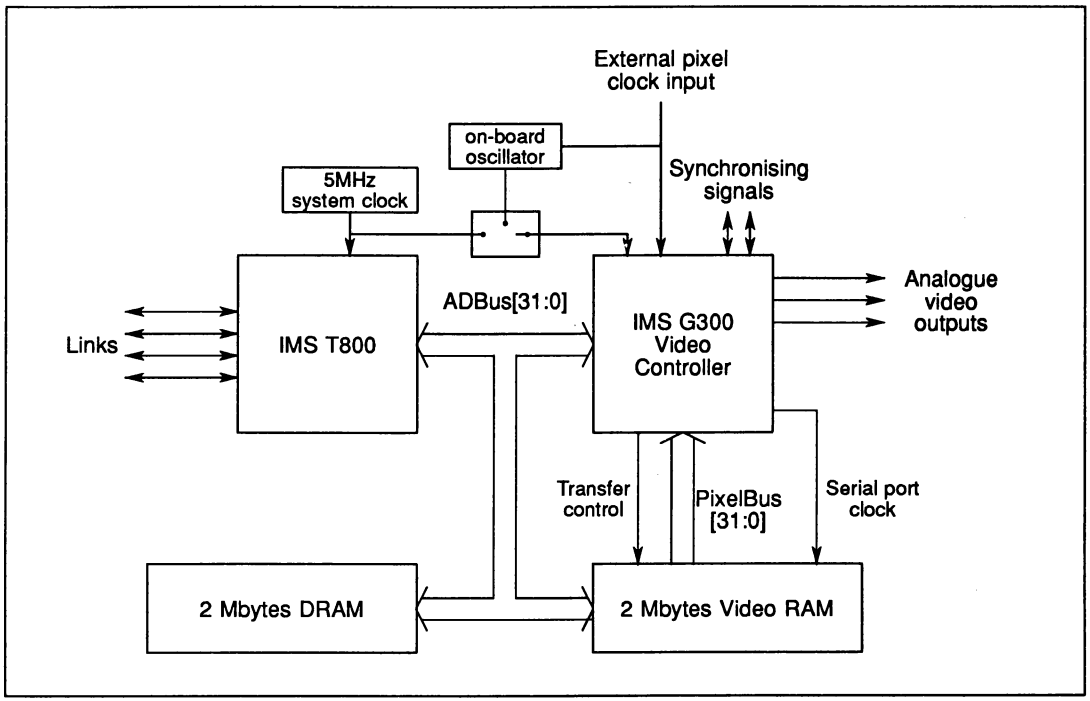


Figure 3.1 IMS G300 TRAM block diagram

3.2 System memory

To provide a program store and frame store each of 2 Mbytes, 1 Mbit devices were chosen, organised as 256K by 4 bits. Sixteen devices are required to provide each 2 Mbyte store, on a 32 bit databus so the VRAM and DRAM are organised in two banks of eight devices.

3.2.1 IMS T800 external memory interface

The external memory interface (EMI) of the IMS T800 supports a wide range of memory devices and provides general purpose DRAM control. It is provided with five output strobes, four of which can be configured by the user. These strobes control the address multiplexing and row, column strobe generation. In this particular application the programmable strobes have been assigned the following functions:

notMemS0	Address latch enable	(**notALE**)
notMemS1	Row address strobe	(**notRAS**)
notMemS2	Address multiplex control	(**notAMUX**)
notMemS3	Column address strobe	(**notCAS**)
notMemS4	Wait state insertion control	

The external memory cycle of the transputer is divided into six segments known as Tstates with the following functions:

- T1 Address setup time before address valid strobe
- T2 Address hold time after address valid strobe
- T3 Read cycle tristate or write cycle data setup
- T4 Extendable data setup time
- T5 Read or write data
- T6 Data hold

Under normal conditions each Tstate may be from one to four periods Tm long, where Tm is half a processor cycle, 25ns for the IMS T800-20. A full description of the IMS T800 EMI can be found in the IMS T800 datasheet.

The configuration of the EMI consists of specifying the falling and rising edges of the programmable strobes relative to the T-states so as to produce the timing needed for the particular memory system being used. The memory interface is programmable to a resolution of one Tm. If slow devices are to be included within the system then the basic cycle time must be increased by adding wait states (T4 states).

The memory devices used have a minimum cycle time of 190 ns, thus the interface cycle time must be set to 4 periods of **ProcClock**, where the period of **ProcClock** is 50 ns. The G300 CVCs microport has a cycle time of 5 periods of **notSerialClock** for a write and 7 periods for a read. With the period of **notSerialClock** set to 50ns this gives the cycle times of 250ns and 350ns respectively. It is not possible to multiple configure the IMS T800, therefore a wait state generator has been included which adds extra T4 states. The wait state generator increases the cycle time to 6 periods of **ProcClock** for a write and 7 periods for a read switching **notMemS4** into the **MemWait** input whenever the G300 CVC is addressed. A delayed **notMemS4** is used for the read cycle, which requires one extra wait state. The cycle times for the microport have been calculated using a Serial clock period of 50 ns, however, if the period of Serial clock is increased the cycle time of the microport increases. The wait states produced by the present configuration will be insufficient, therefore a new configuration must be calculated and implemented in the configuration PAL, which is socketed for this purpose.

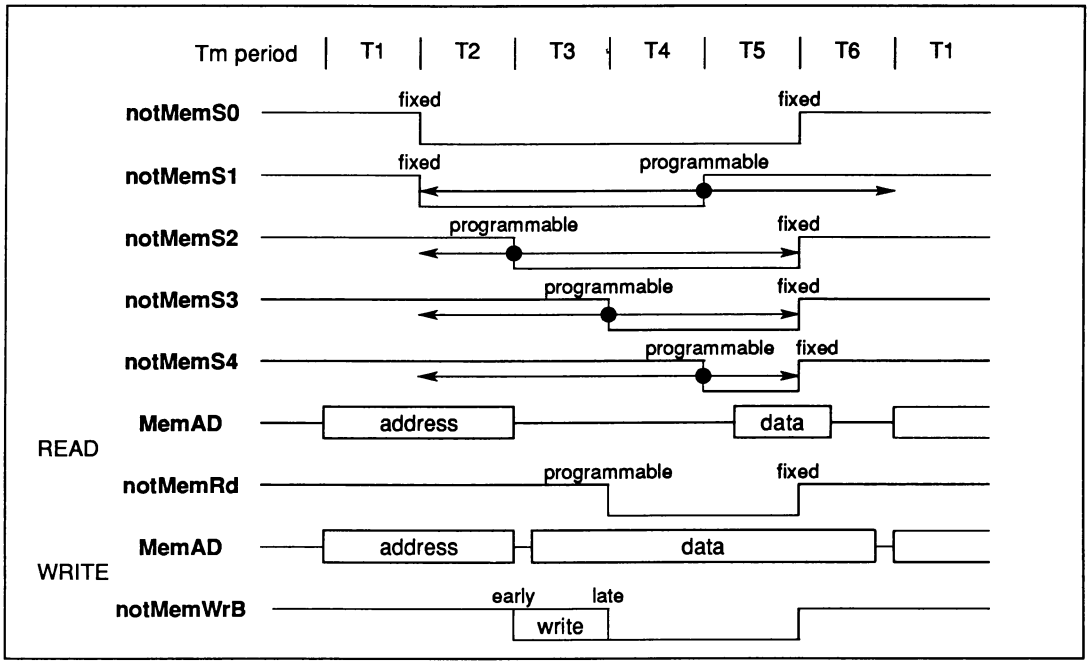


Figure 3.2 Generalised timing for EMI

3.2.2 External memory interface configuration

The IMS T800 has 13 internal pre-defined configuration patterns. The configuration must satisfy the timing requirements for:

1 G300 microport

2 DRAM interface

3 VRAM interface

with the following cycle times:

1 Basic memory cycle, 4 cycles for the DRAM and VRAM

2 Basic cycle extended by S4 to produce 6 cycles for G300 CVC write and 7 cycles for a read. (Serial clock 50ns)

In order to maximise performance an optimum configuration has to be calculated. The 13 pre-defined configurations do not match these requirements, therefore an external configuration has to be chosen. To aid in the calculation of configuration data a program is included in the Transputer Development System which produces data suitable for inclusion in a configuration ROM. A listing of the data produced may be found in the appendix.

A PAL (programmable logic array) is used to store the configuration data. It is programmed as an address decoder which provides a data bit in response to the addresses supplied by the transputer at the configuration stage. When an external configuration is chosen a number of requirements have to be met:

1 During the reset phase the transputer executes an internal configuration scan which takes each **MemAD** pin low successively at intervals of two **ClockIn** periods, the **MemAD** pins stay low until the end of the scan. If one of the **MemAD** pins is connected to **MemConfig** then a preset internal configuration is chosen. For an external configuration to be chosen

the **MemConfig** pin must be held low during the scan period, but must allow the PAL to respond during the read phase of the configuration cycle.

2 If an external device is used to provide the configuration, then the data presented to the **MemConfig** pin must be inverted.

Both these requirements can be matched by the PAL; it is programmed to output a logic '0'(the PAL inverts the data on the output pin) for the addresses which have a '1' associated with them in the configuration data. For any other adddress the PAL does not respond and outputs a '1'. Memory address A31 is included in the logic term to ensure the device only responds to the read cycle of the configuration (figure A.3). Once the configuration has been loaded it does not matter if the PAL is selected as any further activity on the Config pin is ignored.

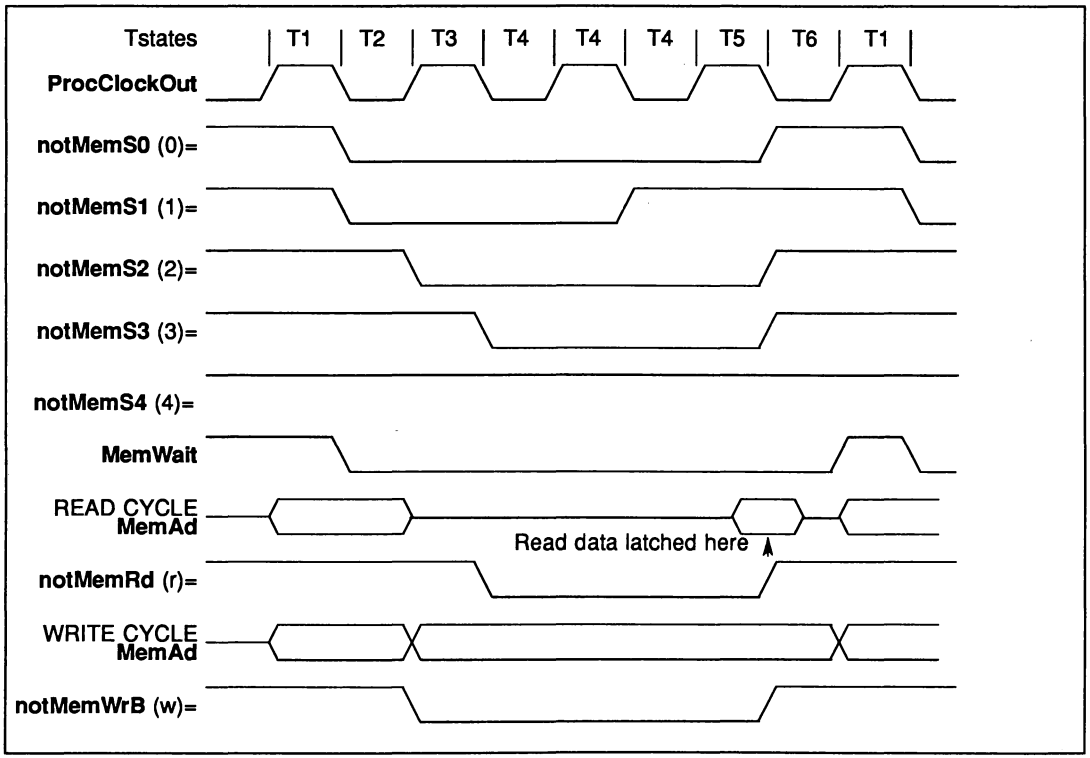


Figure 3.3 Timing for basic memory cycle

3.2.3 VRAM operation

Historically, Dynamic RAMs have been used for graphics memories owing to their low cost per bit. However, since both screen refresh and bitmap redraw must take place simultaneously, using a technique known as 'cycle stealing', the bandwidth of the RAM array imposes a severe restriction on performance. At screen sizes over about 1/4 million pixels, it is no longer feasible to use this approach and Video DRAMs, which contain their own shift register accessed via a second port, are needed. Use of Video DRAMs realises up to 95% of the bitmap bandwidth for the exclusive use of redraw operations and makes it feasible to maintain very large screens without needing a large amount of external hardware.

The VRAM is organised with a RAM port, compatible with the conventional Dynamic RAM and a serial port which operates asynchronously to the RAM port supplying serial data to the display. For further information regarding multi-port Video RAMs refer to the application note on VRAMs published by Hitachi.

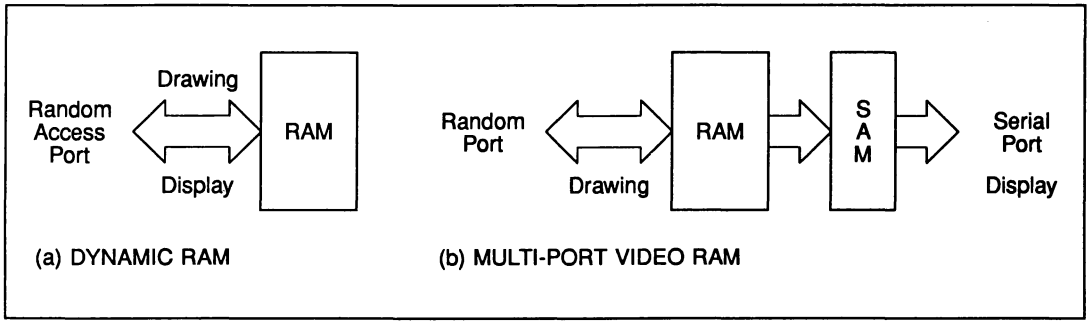


Figure 3.4 Conventional RAM and VRAM

Video RAMs reload their shift registers by performing a read cycle while holding **notDT/notOe** low as RAS falls. The address values presented to the VRAM on the falling edges of **notRAS** and **notCAS** define which row is loaded into the shift register and which bit in the register is shifted out first. The actual transfer takes place on the rising edge of **notDT/notOe**. This operation is timed so that the transfer takes place while data is being streamed out to the screen without producing any visible transfer glitch. This timing is critical and is handled completely by the G300 CVC.

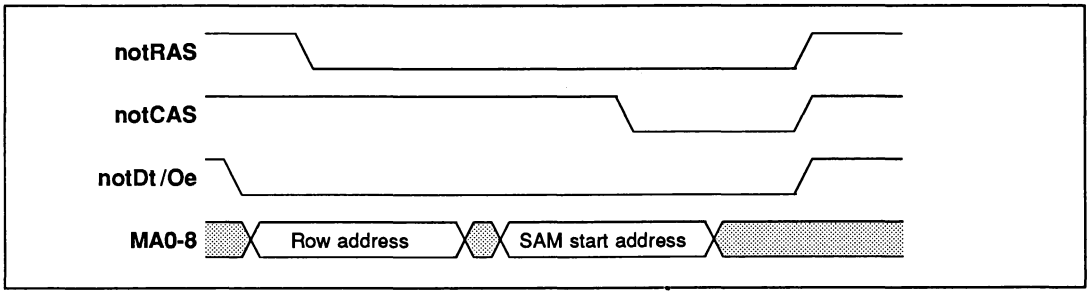


Figure 3.5 VRAM transfer timing

3.2.4 G300 CVC memory interface

The IMS T800 is the primary memory controller in the system, controlling read/write operations to both the DRAM and the VRAM. The G300 CVC performs memory operations to the VRAM on a DMA basis. The G300 CVC gains control of the VRAM by asserting a bus request. The T800 responds by asserting **MemGranted**, tristating the bus and taking the control strobes to an inactive state. The G300 CVC now takes control of the bus and outputs a 22 bit row address. This row address specifies the new row of pixels to be displayed and is incremented before every row transfer, unless the address is supplied by the host. The G300 CVC does not provide any specific memory control signals and any strobes such as RAS and CAS must be generated by the user.

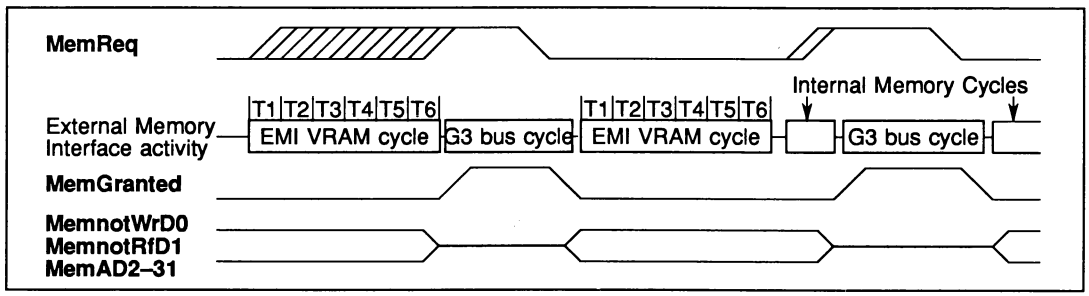


Figure 3.6 MemGranted with G3 bus cycles and external, internal memory cycles

The G300 CVC provides a number of strobes which are used to generate the various control signals required by the VRAMs, two of which are programmable, **BusRequest** and **Transfer**. The user may program these strobes to cause the data transfer cycles to occur at the correct points during the screen display to implement seamless mid-line updates. These strobes are controlled by values loaded into two registers, **MemInit** and **TransferDelay** whose programming is described in the next section.

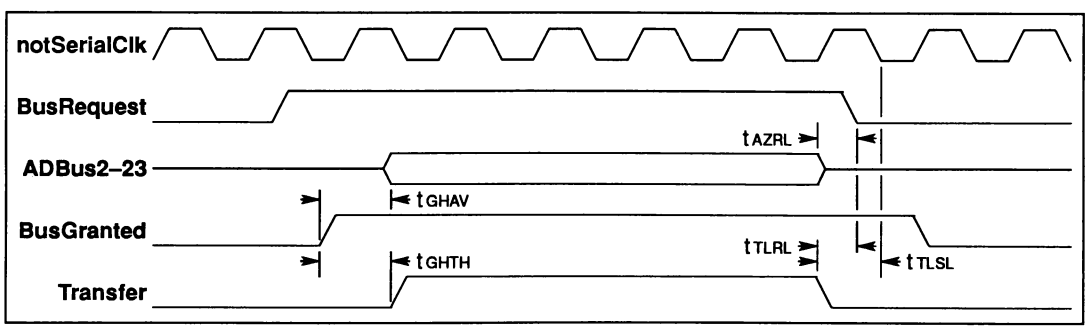


Figure 3.7 Data transfer timings for G300 CVC

Symbol	Description	Min	Max	Units
t_{GHAV}	**BusGranted** high to address valid		3*SClk[1]+30	ns
t_{AZRL}	Address invalid to **BusRequest low**	0		ns
t_{GHTH}	**BusGranted** high to **Transfer** high		SClk+20	ns
t_{TLRL}	**Transfer** low to **Bus Request low**	−5	5	ns
t_{TLSL}	**Transfer** low to **notSerialClk** low	10	SClk−10	ns
Note: These figures are not characterised and are subject to change				

Table 3.1 Micro port DMA and Transfer timings

[1]SClk Period of **notSerialCLK**

The required VRAM strobes, which are inverted by a PAL, are generated by clocking a '1' through an 8 bit shift register which is clocked by **notSerialClk**. The first three bits are not used as this produces a 3 **SerialClk** delay to satisfy the **BusGranted** to address valid timing parameter (tGHAV). When the G300 bus cycle is complete the shift register is cleared which deactivates the derived memory strobes. The shift register is cleared by the signal **G3BusCycle** in order to observe the RAS precharge time for the next VRAM cycle.

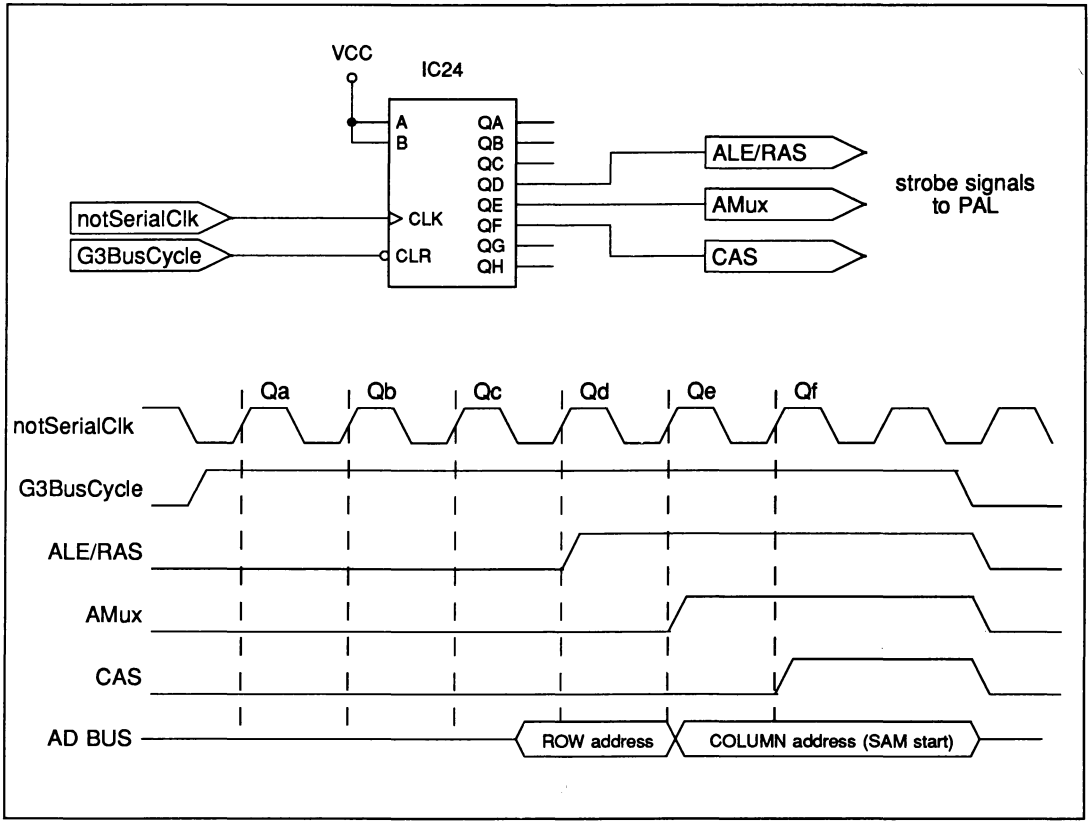


Figure 3.8 Memory strobe generation for G300 VRAM interface using a shift register

Figure 3.9 shows the generation of **G3BusCycle**, which is used to clear the shift register ready for the next transfer and de-selects the relevant logic in the latch control PAL. The rising edge of **MemGranted** causes the control signal **G3BusCycle** to go high which indicates the start of the transfer cycle. When the transfer is complete, i.e. **Transfer** goes low, **G3BusCycle** returns low ending the current cycle.

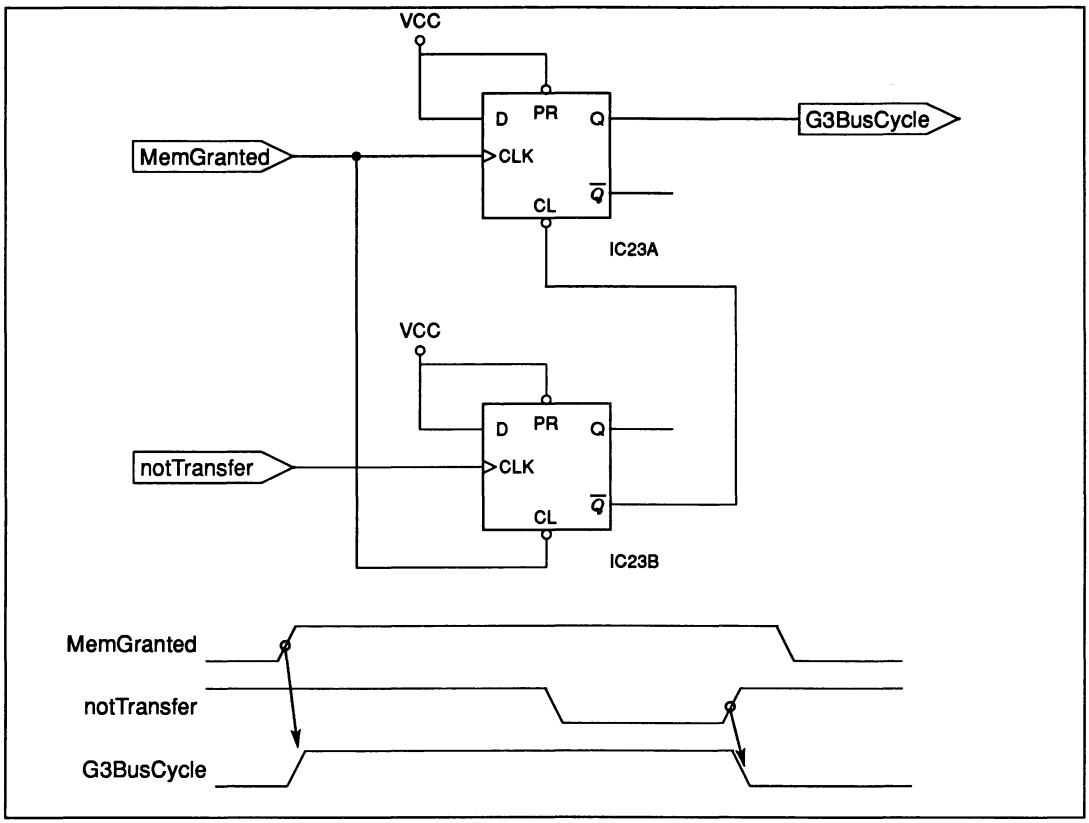


Figure 3.9 Generation of **G3BusCycle**

When the G300 CVC initiates a transfer cycle the transfer occurs in both banks of VRAM. In order to avoid data conflict on the pixel bus the serial output enables (SOE) are used to select which bank produces pixel data. This bank swap must be synchronised to the serial clock, otherwise the wrong pixel data would be displayed. The D-type circuit shown in figure 3.10 is used to latch the bank address bit on the rising edge of **notTransfer**, the serial outputs are enabled/disabled on the rising edge of **notSerialClk**. This scheme ensures that the bank swap is completed with sufficient setup time before the G300 latches the pixel.

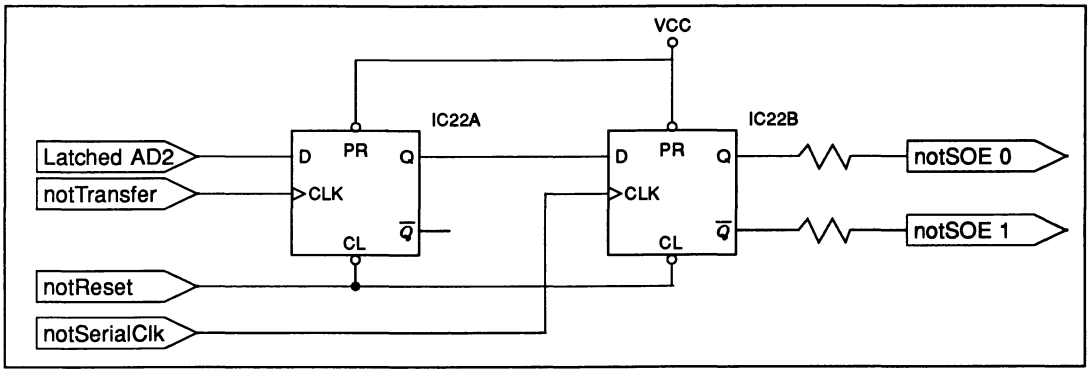


Figure 3.10 SOE decode

3.2.5 Calculation of memory control parameters

In many systems the reloading of the shift registers takes place during flyback. However when the G300 is used with VRAMs the shift registers can be reloaded midline. This allows screens with an arbitrary number of pixels per line to be constructed with any length shift register. In order to do this some look-ahead is required in order to be able to make the transfer at exactly the right point without any discontinuity on the screen. This look-ahead is provided by programming the appropriate values into the **MemInit** and **TransferDelay** registers inside the CVC.

At the start of each display frame, the G300 CVC initiates a transfer cycle at the beginning of the backporch period of the first line and performs the data transfer with the delay specified in the **TransferDelay** register. The G300 has the following requirement:

$$\text{TransferDelay} \leq \text{BackPorch} - 1$$

This ensures that there is data loaded ready for the first line scan to begin.

The G300 then begins to count **notShiftClk** cycles and initiates a further transfer cycle after **MemInit** cycles of **notShiftClk**. After a further number of cycles of **notShiftClk** equal to **TransferDelay**, the G300 CVC takes **Transfer** low and the new data is loaded into the shift registers.

Thus the period of row transfer operations is

$$\text{MemInit} + \text{TransferDelay}$$

The critical parameter as far as DMA accesses are concerned is **TransferDelay** which needs to be long enough to allow for the DMA latency of the controlling processor as well as the access time of the video RAMs. The G300 CVC imposes an extra overhead of four **notSerialClk** periods which needs to be added to the **TransferDelay** parameter but which does not appear as part of the delay between **BusReq** and **notDataTransfer**. Thus:

$$\begin{aligned}\text{TransferDelay} &= \text{system DMA Latency} \\ &+ \text{VRAM Access time} \\ &+ 4\ \text{SClk}\end{aligned}$$

From the IMS T800 data sheet the memory request response time has a minimum time of 2 Tm and a maximum of 5 Tm, but, this assums that no external memory cycles are in progress. If an external cycle is active the maximum time could be:

$$(1\ \text{EMI cycle Tmx}) + (1\ \text{refresh cycle TRfLRfH}) + (6\ \text{periods Tm})$$

In this case we have:

Tm = 25ns (IMS T800-20)

1 EMI cycle Tmx = 200ns

TRfLRfH = Tmx + Tm + 6ns = 200 + 25 + 6

TRfLRfH = 231ns

Therefore:

200ns + 231ns + 150ns = 581ns

DMA latency = 581ns

TransferDelay	=	581ns	(SClk = 50ns)
	+	200ns	
	+	200ns	
TransferDelay	=	981ns	

or in terms of SClk, TransferDelay = 20

MemInit + TransferDelay = 512

MemInit = 492

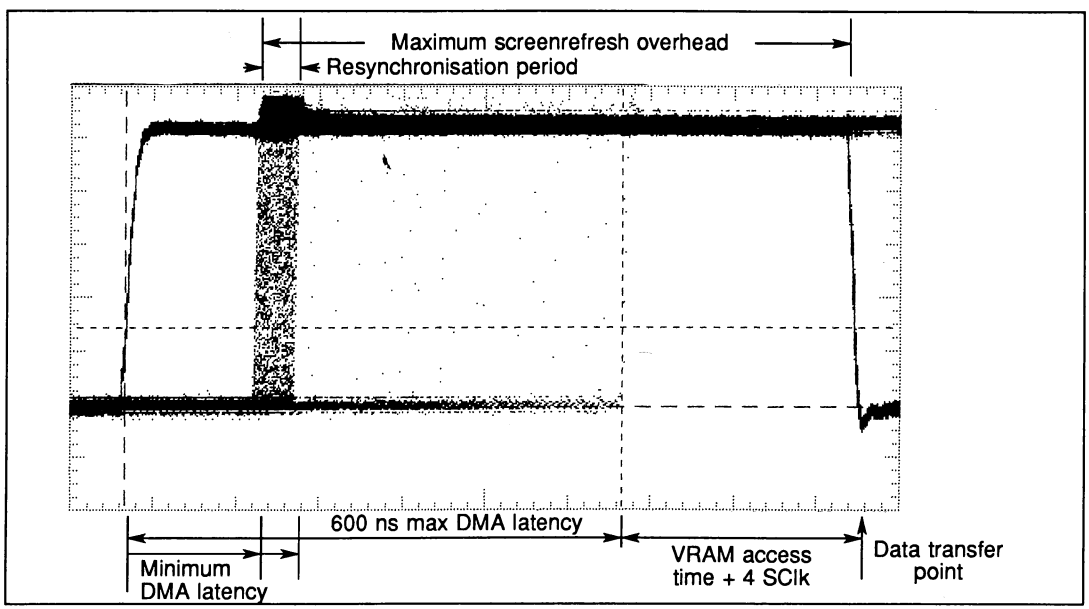


Figure 3.11 Measured DMA latency

3.2.6 Memory addressing considerations

This section describes the memory addressing problems associated with video systems. In this type of application the processor and CVC must have access to the frame store for the specification and display of data. This unfortunately poses various problems as both devices have conflicting addressing requirements.

In order to simplify programming, the frame store must appear as contiguous memory, in software this would be set up as a two dimensional byte array.

In a normal dynamic memory system the processors address bus is split into two fields, known as the ROW and COLUMN address, which relates to the internal structure of the RAM array. If the low order bits (A10..2) as in figure 3.12 are used for the ROW address and data is written to the array, starting at the first address, the first 512 words are written to ROWs 0–511, COLUMN 0, the COLUMN address is then incremented and the next 512 words written to ROWs 0–511, COLUMN 1 etc.

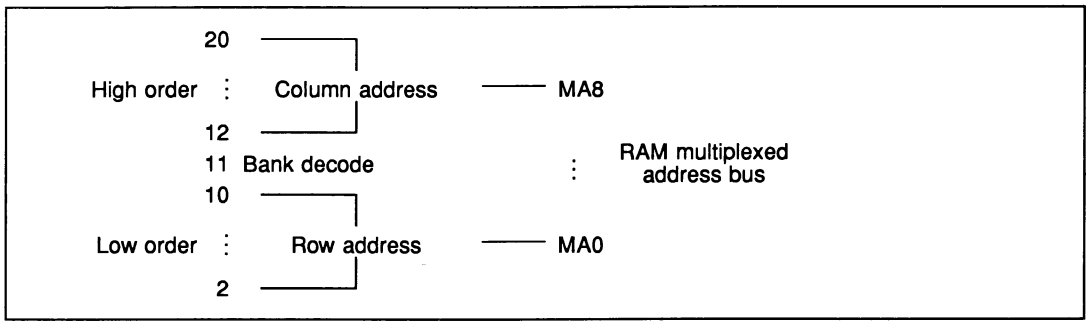


Figure 3.12 Conventional DRAM multiplexing

This method for writing and storing data does not cause any problems at the processor side, but causes problems for display. This occurs when the CVC initiates a transfer as the transferred ROW contains data written to COLUMNs 0–511, but the data is stored in ROWs 0–511. Therefore if the display is to be correct the first 512 words must be written to ROW 0, COLUMNs 0–511. To achieve this the ROW and COLUMN addresses must be swapped for a processor and CVC access.

The addressing arrangements for the processor and CVC are shown in figure 3.13. The VRAM banks are decoded by address bit A11 from the processor side, which swaps banks every 512 words. Although this does not disturb the appearance of contiguity to the software the displayed screen would become non-contiguous;

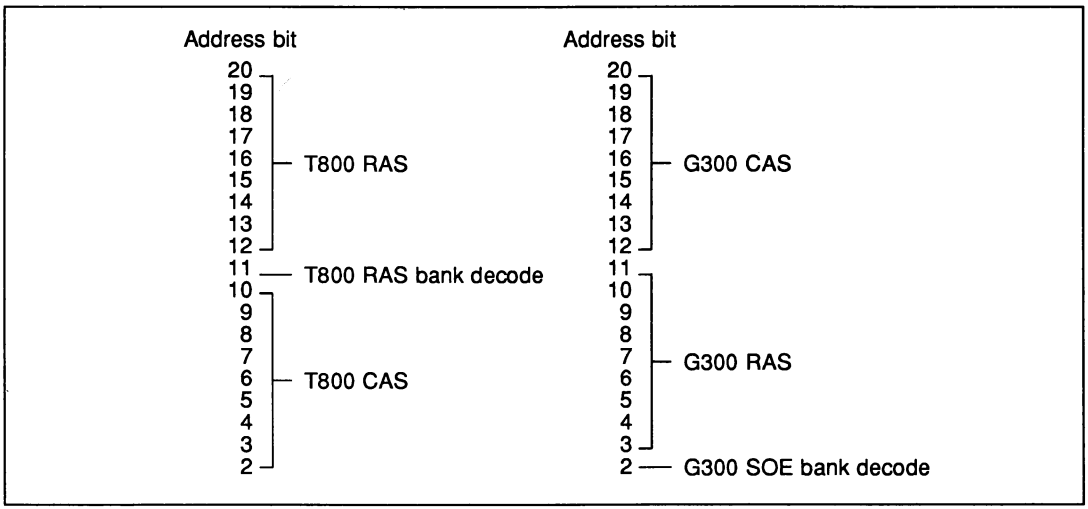


Figure 3.13 TRAM address multiplexing

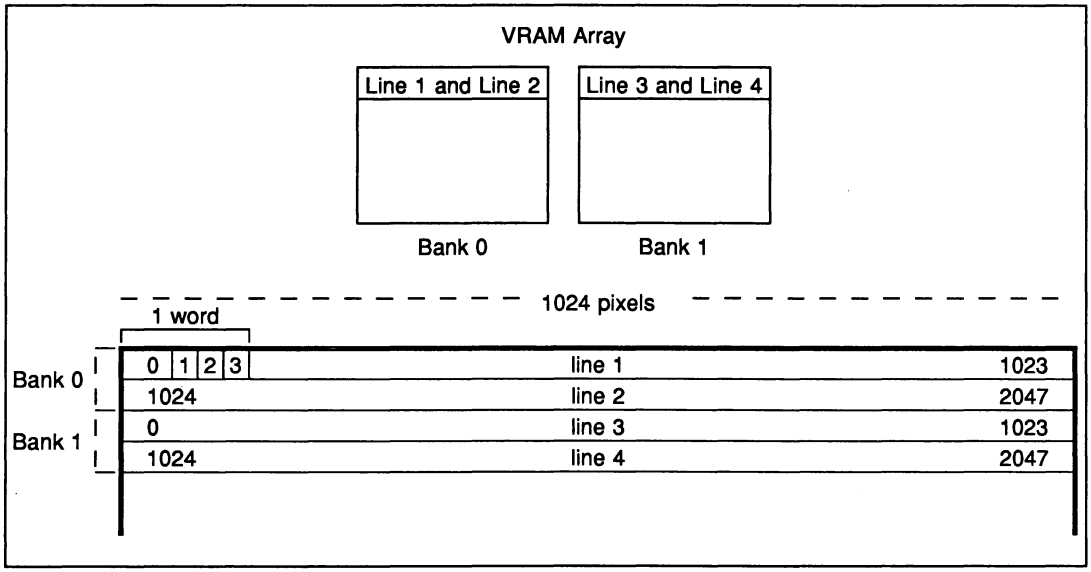


Figure 3.14 Example of 1024 x 1024 screen layout

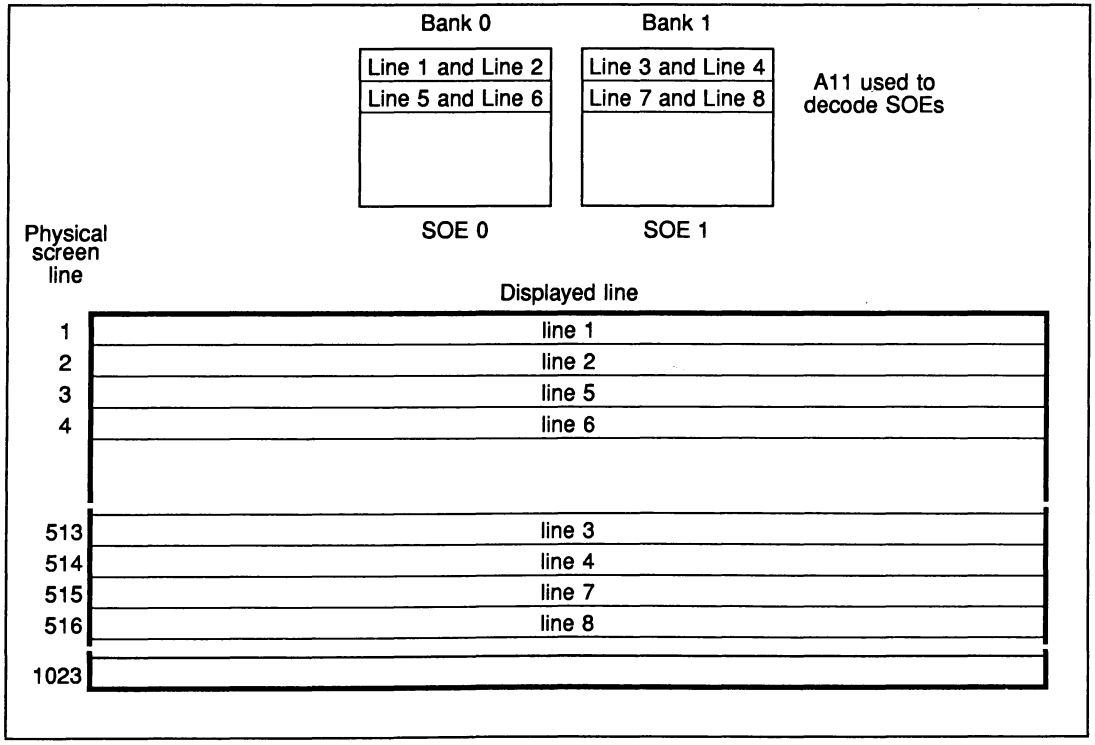


Figure 3.15 Effect of untransposed addresses on display

On each transfer 512 x 4 bits per VRAM are moved from the RAM to the serial access memory, giving a total of 512 x 32 bits or 2048 pixels for the whole bank. For the example in figure 3.14, each transfer produces

2048 pixels or two screen lines. The bank is then swapped and another 2048 pixels transfered. If the screen line length is increased to 1280 pixels the transfer still occurs after 2048 pixels, but occurs as a seamless midline update.

The screen refresh addresses provided by the CVC are multiplied by the shift register length, 512 bits in this case. Therefore when address bit A11 is used to select the banks from the CVC side a strange display is produced (figure 3.15) as the first 512 screen lines come from bank 0. To produce the correct display, address bit A2 is used to swap the banks every other transfer, regardless of the display size.

3.2.7 PAL functions

In order to reduce the complexity of decode/driver logic high speed PALs are used to select the multiplexors and generate the various strobes required by the memories.

Address multiplexor output control

This PAL controls the latch and output enables of the address multiplexors. It replaces discrete logic with the following functions:

1 Selection between T800 and G300 derived strobes.

2 Row, Column swapping for T800 addresses.

3 Logic inversion for G300 derived strobes.

4 Refresh control using low order bits (RAS only refresh).

Truth table for address multiplexor PAL

```
Inputs / Outputs

          - notMemS0          1  0  0    X  X  X    1  0
   T800     notMemS2          1  1  0    X  X  X    1  1
          - notMemRf          1  1  1    1  1  1    0  0
                                                              Inputs
            G3BusCycle        0  0  0    1  1  1    0  0
   G300   - G3ALE              0  0  0    0  1  1    0  0
          - G3AMux            0  0  0    0  0  1    0  0

            notALE            1  0  0    1  0  0    1  0
            notT8HoOe         0  0  1    1  1  0    1  1
            notT8LoOe         1  1  0    1  1  1    0  0   Outputs
            notG3LoOe         1  1  1    0  0  1    1  1

                              |_____|    |_____|    |___|
                                 |          |          |
                                 |          |       Refresh
                                 |       G300 Memory access
                            T800 Memory access
```

Where:

notT8HoOe	T800 High Order address Output enable (A20..12)
notT8LoOe	T800 Low Order address Output enable (A10..2)
notG3LoOe	G300 Low Order address Output enable (A11..3)
notALE	Address Latch Enable

Row and Column strobe generation

In order to meet critical timings a high speed PAL is used to generate the required RAS and CAS strobes for the memory arrays. Separate strobes are used to drive each bank on both the DRAM and VRAM as this decreases the capacitive loading on the respective strobe, thus removing the need for further buffering of these signals.

It provides the following functions:

1 Arbitration of T800 and G300 RAS, CAS strobes.

2 Selection of banks using RAS decode.

3 Provides RAS only refresh.

Full logic diagrams and CUPL listings for these PALs may be found in the appendix.

3.2.8 System memory map

The memory space on board may be divided into two non-contiguous areas, bitmap and workspace, so that operating systems which use automatic workspace sizing will not trespass on the screen space. A series of PCB links are provided which enables the bitmap and workspace to become contiguous, this enables any spare video ram to be used as program space if required.

Jumper JP4 selects VRAM start address as #80200000
Jumper JP5 selects VRAM start address as #C0000000

Figure 3.16 shows how the memory is mapped into the address space of the IMS T800.

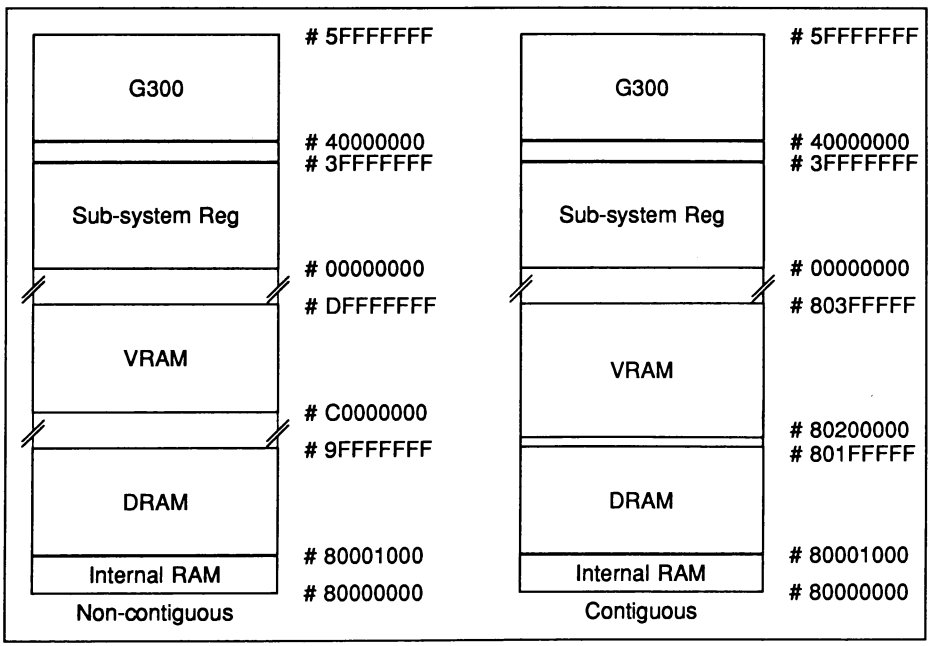


Figure 3.16 Non-contiguous and contiguous address maps

During a refresh cycle A2..11 provides the refresh address, A12..30 are set high and A31 is set low. This decodes as #7FFFFFFF and anything placed at this address would be selected during a refresh cycle,

therefore this address is not used.

3.2.9 SubSystem registers

The user may require the G300 Graphics TRAM to control a network of transputers and/or other TRAMs. A set of control signals are provided which enables the master to control these slaves or subsystems. The SubSystem port consists of three signals: **SubSystemReset** and **SubSystemAnalyse**, which enables the master to reset and analyse its subsystem; and **SubSystemnotError**, which is used to monitor the error flag in the subsystem.

To maintain software compatibility between TRAMs the SubSystem registers start at hardware address #00000000. These registers are located as shown in table 3.2

Register		Hardware byte address
SubSystemReset	(Wr only)	#00000000
SubSystemAnalyse	(Wr only)	#00000004
SubSystemnotError	(Rd only)	#00000000

Table 3.2

The SubSystem port operates as follows:

Writing a '1' into bit 0 of #00000000 asserts SubSystemReset.
Writing a '0' into bit 0 of #00000000 deasserts SubSystemReset.

Writing a '1' into bit 0 of #00000004 asserts SubSystemAnalyse.
Writing a '0' into bit 0 of #00000004 deasserts SubSystemAnalyse.

A '1' read from bit 0 of #00000000 indicates that SubSystemnotError is TRUE.
A '0' read from bit 0 of #00000000 indicates that SubSystemnotError is FALSE.

A further two registers are included which enables users to reset the G300 CVC and to switch between the system clock or the on board oscillator. The first of these registers enables users to reset the G300 CVC without reseting the IMS T800, this is important when the application running must not be interrupted. The second register allows users to select a particular pixel dot rate, which may not be attainable using the 5 MHz system clock and PII multiplication factors. Refer to the section on G300 clock selection for further information on input clocks and multiplication factors.

The auxiliary control registers operate as follows:

Writing a '1' into bit 0 of #000000F0 asserts G300 CVC reset
Writing a '0' into bit 0 of #000000F0 deasserts G300 CVC reset

Writing a '1' into bit 0 of #000000F4 selects the on board Osc for PLLClkIn
Writing a '0' into bit 0 of #000000F4 selects 5 MHz for PLLClkIn

On power up, or on a system reset the Clock selection register defaults to '0'

3.3 Event request hardware and software considerations

In some graphic applications such as animation it is useful to have at least two displays mapped onto the same frame store. This allows one frame to be displayed whilst the other is being updated. Flipping the display during frame flyback allows frames to be drawn before being displayed, preventing disturbing visual effects.

In order for the user to swap frames or update the display memory in frame flyback the signal **FrameInactive** is used to produce an event request to the T800. To avoid confusion only, one event request is made at the beginning of frame flyback and it is up to the user to ensure that the process finishes before the active display is entered. Thus for a 1024 x 1024 screen the user has approximately 580 us process time.

It must be noted that the event request logic will only clear on an event acknowledge from the transputer, therefore it is possible that an event will not be serviced until the active display area has been entered. To prevent this the following structure should be used in an occam program.

```
CHAN OF ANY Event, EventAck, EventReq :
PLACE Event AT 8  :
INT any :

PRI PAR
  {{{ Event Handler
  WHILE TRUE
    PRI ALT
      {{{ acknowledge unwanted events
      Event ? any
        SKIP
      }}}
      {{{ service user events
      EventReq ? any
        SEQ
          Event ? any
          EventAck ! any
      }}}
  }}}

  {{{ user process
  .
  .
  .
  {{{ use whenever an event is required
  INT any :
  SEQ
    EventReq ! any
    EventAck ? any
  }}}
  .
  .
  .
  }}}
```

3.4 Video outputs and current reference

The G300 CVC complies with both the RS170a and EIA-343 video standard. It provides RGB analogue outputs which are brought out to the edge of the board on three SMB connectors. The outputs are designed to drive a doubly terminated 75R line, thus the effective load seen by the device is 37.5R. To provide a stable reference current an LM334 precision current reference is used with the reference current set to 8.8mA, this produces a 1V pk-pk signal across the 37.5R load.

SMB identification from top to bottom of the board.

1	Pixel clock in	Input (note)
2	Vertical Sync	Output
3	Composite or Horizontal Sync	Output
4	Blue	Output 75R
5	Green	Output 75R
6	Red	Output 75R

Note maximum Pixel clock input is 110 MHz in this case, the speed of the G300 CVC.

3.5 G300 clock selection

Alternate clocking schemes are provided which offer a high degree of system flexibility. The primary clocking system utilises the on chip phase-locked loop to multiply the input clock to the full video clock rate.

The second method which involves disabling the Pll and using a times one clock from the on board oscillator or from an external source.

Table 3.3 shows the recommended input clocks and multiplication factors.

Video data rate (MHz)	PllClkIn (MHz)	Clock Multiplication
30	6	5
40	6.66	6
50	7.142	7
60	7.5	8
70	7.777	9
80	8	10
90	8.181	11
100	8.333	12
110	8.461	13
120	8.571	14

Table 3.3

The figures shown in the above table are for maximum phase-locked loop stability. The G300 Graphics TRAM uses the system clock (5 MHz) to drive the the Pll. To achieve a video data rate of 105 MHz a multiplication factor of 21 is used, although these figures are not recommended for use in a noisy environment they provide an extremely stable picture.

If the required video data rate can not be achieved using the system clock and relevant multiplication factor the on board crystal oscillator may be used by writing a '1' into address #000000F4 and setting the appropriate

jumper.

JP1 Enable PLL (Jumper removed)
JP2 On board Osc to PixClk in (JP3 removed)
JP3 External Pix Clock Enable (JP2 removed)

3.6 Calculation of VTG parameters

The calculation of the frame timing parameters can be derived from the following equations:

During a full line cycle (VBlank, VDisplay)

Halfsync = Horizontal Sync/2
BackPorch = Backporch
Display = Display
FrontPorch = Linetime – (2*HalfSync + BackPorch + Display)

During an Equalisation Cycle

Low period = HalfSync
ShortDisplay = LineTime/2 – (2*HalfSync + BackPorch + FrontPorch)
High period = HalfSync + BackPorch + ShortDisplay + FrontPorch
FrontPorch = LineTime/2 – (2*HalfSync + BackPorch + ShortDisplay)

During a VSync cycle

Low period = BroadPulse
High Period = FrontPorch
FrontPorch = Linetime/2 – BroadPulse

The following restrictions on parameter values must be observed:

All parameters must be non-zero

Linetime must be an even multiple of the period of **notSerialClk**

The Halfline point must fall within the active display period with at least one **notSerialClk** period of display either side of it.

The total number of displayed lines in each frame must be a whole number (Note this means each field of an interlaced frame may have half a line)

The vertical blanking period must be a whole number of lines.

Backporch must exceed **TransferDelay** by at least one **notSerialClk** period.

TransferDelay must not exceed **ShortDisplay**.

See appendix for programming example.

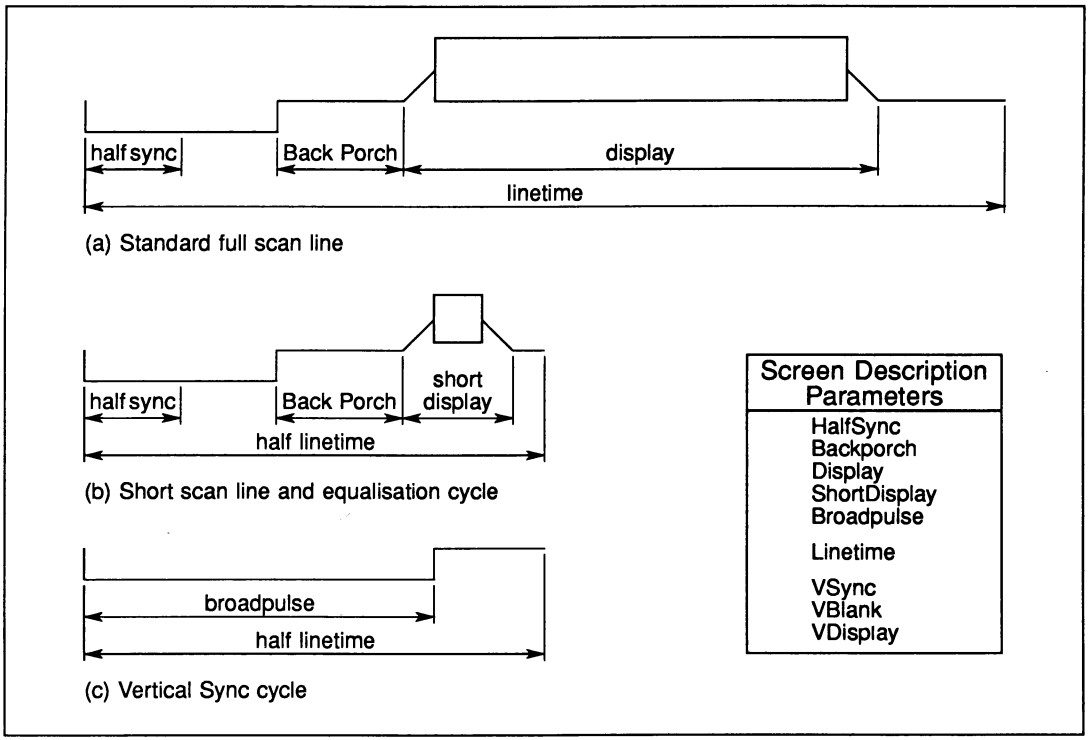


Figure 3.17 Screen description parameter definitions

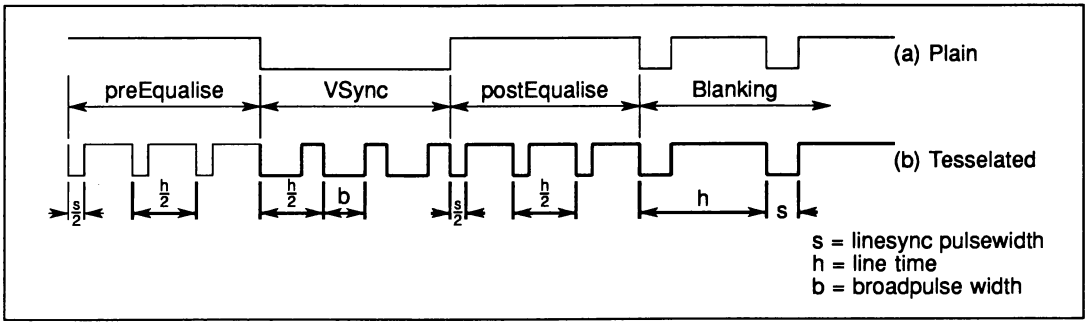


Figure 3.18 Composite sync frame flyback waveforms

3.7 Design considerations for buffering and PCB layout

The design is layed out on a Size6 module (3.3" x 6.4") using six signal layers and separate VDD, GND planes. The separate power planes provide shielding between the signal layers and ensures a good low inductance power supply with distributed capacitive coupling.

The memory control signals are buffered by ACT logic. These devices have TTL threshold inputs and offer rail to rail outputs for maximum noise margins. When compared to 'F' logic devices ACT offers higher output drive currents and a lower dynamic power consumption. The ACT data books state that the input and output diode clamps will match most transmission line impedances. However, the output impedance is around 20R, therefore, it is recommended that a series matching resistor is used at the buffer output to prevent signal reflections along the line. As with any type of termination the resistor must be placed close to the output driver to avoid mistermination. The value of this resistor may be in the range of 15R - 100R and will depend on the characteristic impedance of the line and load. The local decoupling of these devices is also important; a changing supply voltage affects system speed, noise immunity and power consumption. These problems are avoided by implementing good supply and ground busing and using leadless monolithic ceramic capacitors placed close to the device to ensure a low overall inductance.

The following diagrams show the effects of termination using ACT devices.

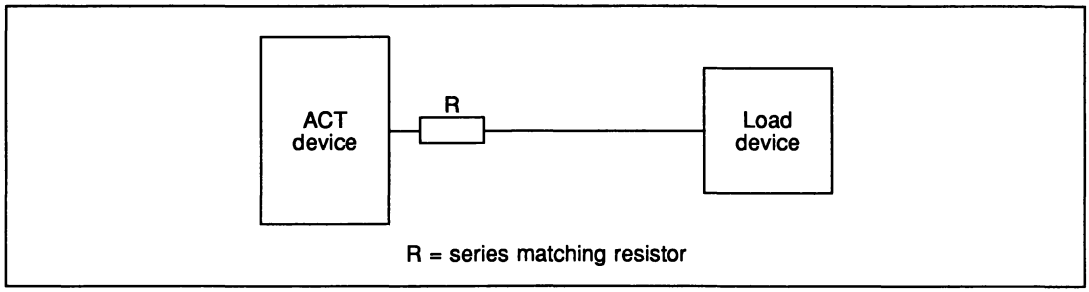


Figure 3.19 Test circuit for the effects of series matching resistor on damping

The under damped response in figure 3.20 could cause the load device to latch-up as the output swings to below -0.5V.

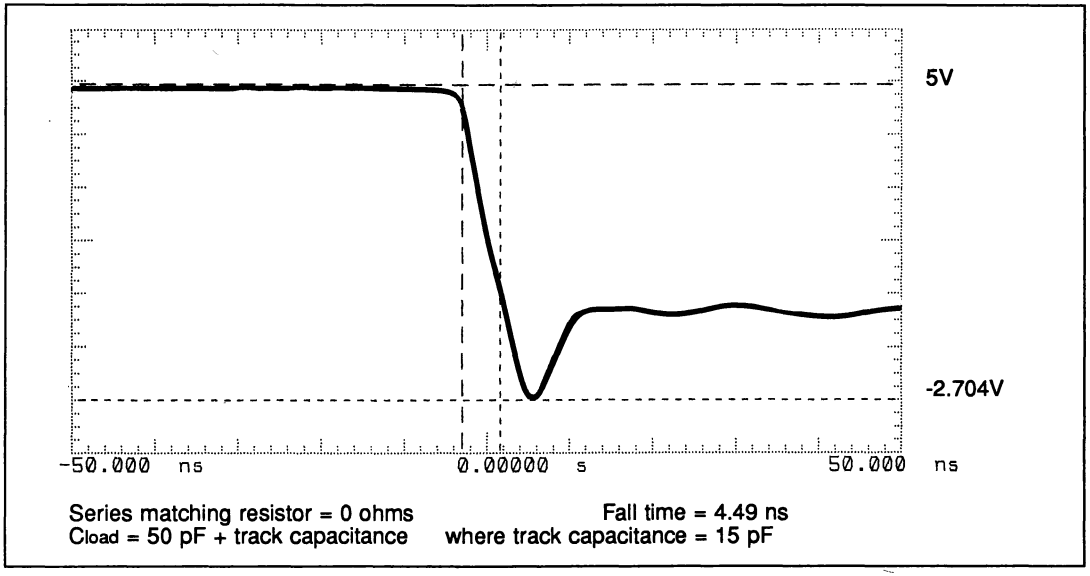


Figure 3.20 Under damped response

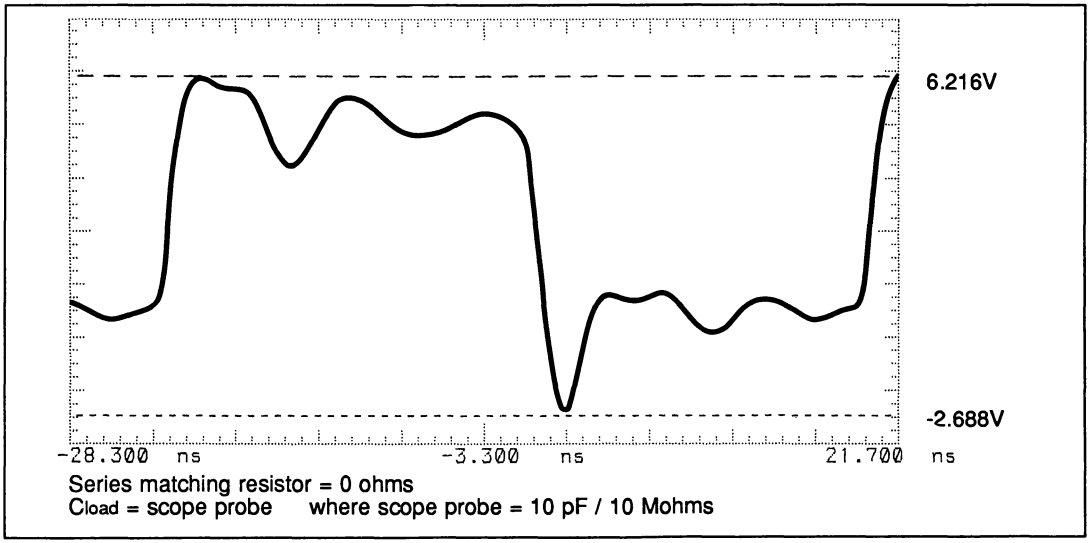


Figure 3.21 Under damped response (scope probe load)

The example in figure 3.21 shows an under damped response, where the series matching resistor has been removed and a scope probe substituted for the load. The signal sweeps outside the supply rails, which could cause a load device to latch-up, possibly causing its destruction.

Over damping the signal as in figure 3.22 increases the rise and fall times of the signal to unacceptable values, therefore the series matching resistor must be chosen to optimally damp the signal.

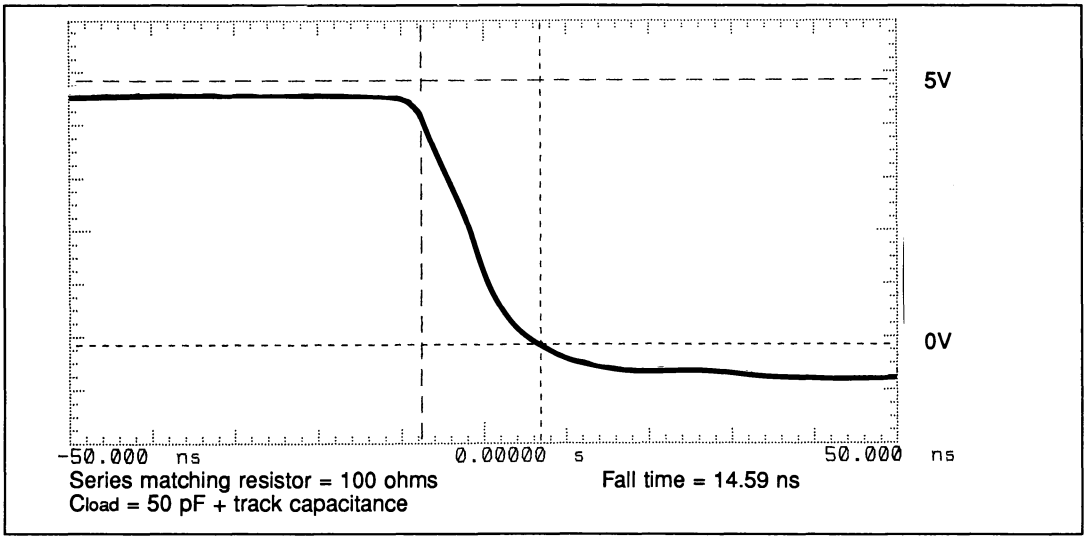


Figure 3.22 Over damped response

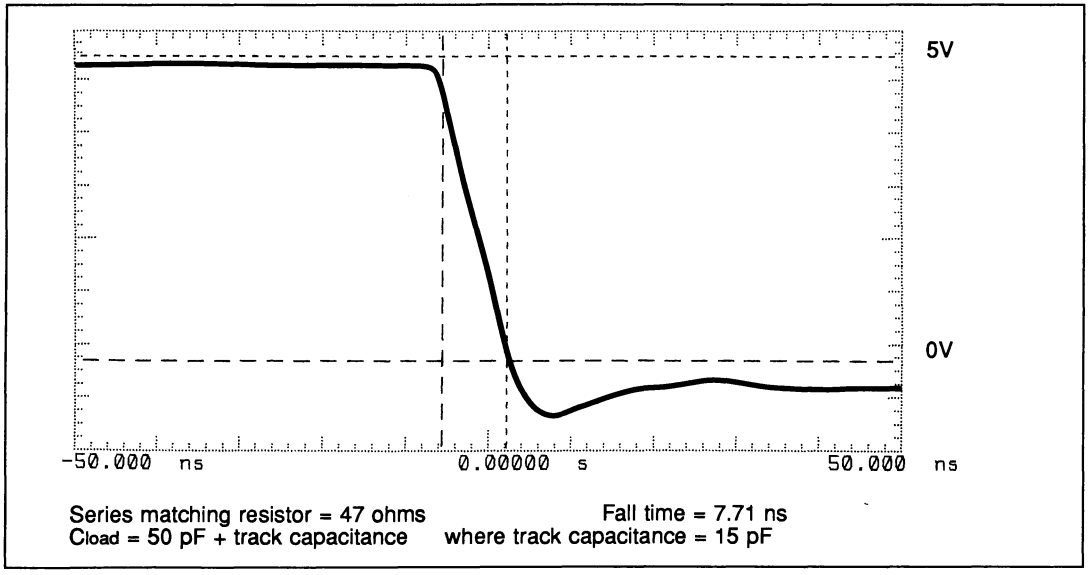


Figure 3.23 Optimally damped response

3.8 Pixel inputs and DAC outputs

The edge rates on the pixel inputs should be kept as slow as possible, consistent with the timing requirements on the pixel port; this will ensure the minimum of clock noise pick up on the analogue outputs. If board layout constraints make the pixel port tracks longer than 3 inches, then series termination resistors placed at the VRAM outputs will improve the matching between the output and the impedance of the PCB track, minimising ringing and undershoot. In order to minimise noise on the DAC outputs it is important to minimise noise on

the power supply to the analogue stage of the CVC, this noise should be no more than 200–300mV. A more important factor than the absolute magnitude of the noise is the ability of the current reference to track the power supply noise on the Iref pin. In practice it is possible to achieve a very clean analogue output, so long as the current source has sufficiently fast response time to keep the voltage on Iref tracking these fluctuations, and so keeping the voltage difference between VDD and the Iref pin constant. The current reference used is based on the LM334 device used in the zero temperature coefficient mode with R39 and D3 providing temperature compensation.

The DAC outputs of the CVC are designed to drive into a singly or doubly terminated 75R load. Double termination is used as both ends of the transmission line are correctly matched and the outputs are less likely to suffer from reflections returning from any mismatch along the length of the transmission line between the DAC outputs and the monitor. The DAC output traces are also treated as transmission lines with shunt resistors placed as close as possible to the CVC. This ensures minimal degradation of the final image quality.

The maximum capacitive loading on the **notShiftClk** output is only 20 pF, in order not to over-drive this signal only one buffer is used. Both the input and output are series terminated, as in Figure 3.24, firstly to slow the edge rate down and secondly to prevent ringing.

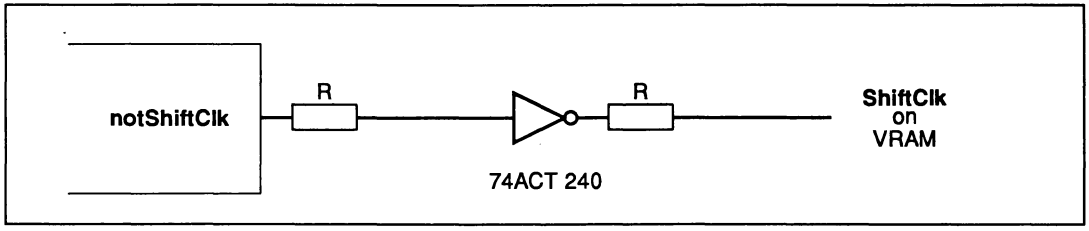


Figure 3.24

A Appendix

A.1 Sample VTG parameters using Hitachi HM-4219/4119 monitor

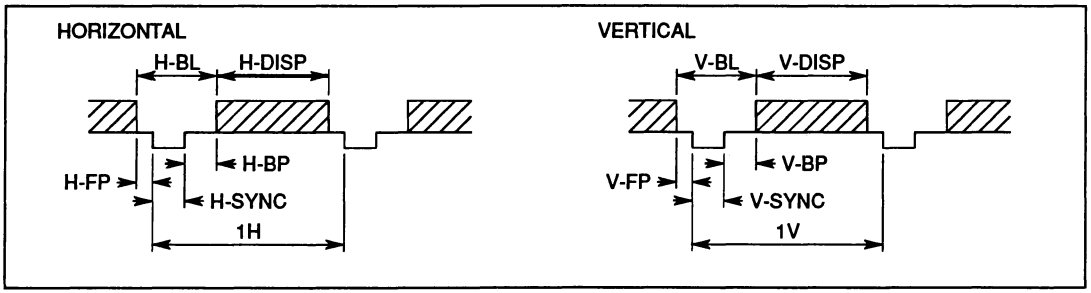


Figure A.1 Hitachi HM-4219/4119 timing

	Item	Equation	Rating (64KHz Version)	Unit
a	Resolution H		1280	Pixel
b	Resolution V		1024	Pixel
c	Pixel rate		9.296	ns
d	Pixel frequency	1/c	107.573	MHz
e	H-DISP	a × c	11.899	μs
f	H-BL	g + h + i	3.800	μs
g	H-FP		0.200	μs
h	H-SYNC		1.600	μs
i	H-BP		2.000	μs
j	1H		15.699	μs
k	H frequency	1/j	63.7	KHz
l	V-DISP	b × j	(1024H)	ms
m	V-BL	n + o + p	(37H)	ms
n	V-FP		(0H)	ms
o	V-SYNC		(3H)	ms
p	V-BP		(34H)	ms
q	1V	l + m	(1061H)	ms
r	V frequency	1/q	60.0	Hz

Table A.1 Recommended timings for monitor (64Khz version)

A.1.1 Calculation of parameters

At the recommended pixel rate of 9.296ns,

$$1 \text{ screen unit} = 4 \times 9.296\text{ns} = 37.184\text{ns}$$

All line timing parameters are calculated as multiples of this figure.

Line Scan period

$$\text{Linetime} = 15.699\mu\text{s} / 37.184\text{ns} = 422.19$$

$$\text{so set Linetime} = 422$$

This obeys the rule associated with the Linetime parameter; that it should be an even number of screen units.

If it is absolutely necessary to meet the recommended linescan frequency then it is best to specify the input clock frequency as the variable but, in practice, all monitors will synchronise to a close approximation.

Line sync pulse

The G300 constructs this from two halfsync periods so:

$$\text{Halfsync} = 1.6\mu s / (2 \times 37.184ns) = 21.5$$

so set Halfsync = 21 screen units

Backporch

$$\text{Backporch} = 2\mu s / 37.184ns = 53.7$$

so set Backporch = 54 screen units

Display

This parameter is set in terms of the number of pixels you wish to display so in this case:

$$\text{Display} = 1280 / 4 = 320 \text{ screen units.}$$

Frontporch

There is no explicit frontporch parameter; this period being implied as the difference between the sum of the other parameters and the linetime period.

$$\begin{aligned}\text{Frontporch} &= \text{Linetime} - ((\text{Halfsync} \times 2) + \text{Backporch} + \text{Display}) \\ &= 422 - (21 \times 2 + 54 + 320) \\ &= 6 \text{ screen units} \\ &= 6 \times 37.184 \text{ ns} = 0.223 \ \mu s\end{aligned}$$

Which compares with the monitor requirement of 0.2 μs.

The 'halfline point' rule is obeyed by these timings since:

$$(\text{HalfSync} \times 2) + \text{Backporch} + \text{Display} < \text{Linetime} / 2 > (\text{HalfSync} \times 2) + \text{Backporch}$$

In a non interlaced system such as this the remaining two line parameters are actually used only during frame flyback in order to count in multiples of half a line time. In an interlaced system, the parameter Shortdisplay is used to construct the short displayed lines at top and bottom of the screen if the total number of displayed lines is odd. BroadPulse is used to produce the low pulses in a tesselated frame sync period. Both of these parameters must always be programmed whether or not your system explicitly uses them.

ShortDisplay

$$\begin{aligned}\text{Shortdisplay} &= (\text{Linetime} / 2) - [(\text{HalfSync} \times 2) + \text{Backporch} + \text{FrontPorch}] \\ &= 211 - (42 + 54 + 6) \\ &= 109 \text{ screen units}\end{aligned}$$

$$\begin{aligned}\text{BroadPulse} &= (\text{Linetime} / 2) - \text{Frontporch} \\ &= 211 - 6 \\ &= 205 \text{ screen units}\end{aligned}$$

Frame timing parameters

All frame timings are specified in terms of half line times.

Number of Displayed lines is 1024

$$\text{VDisplay} = 1024 \times 2 = 2048$$

Which complies with the requirement that each frame must contain an even number of half lines.

The G300 produces frame flyback waveforms in accordance with the broadcast standards which means that:

$$VSync = PreEqualisation = PostEqualisation$$

$$VSync = 6$$

Total Blanked period is 37H so :

$$VBlank = 74 - (6 \times 3) = 56$$

Which is a whole number of lines.

Thus the complete list of screen parameters is:

HalfSync	=	21
BackPorch	=	54
Display	=	320
LineTime	=	422
ShortDisplay	=	109
BroadPulse	=	205
VSync	=	6
VBlank	=	56
VDisplay	=	2048

The remaining three parameters are concerned with management of the video ram bitmap. Since 1M video rams are used, the shift register length will be 512 bits. The sum of the parameters MemInit and TransferDelay must not exceed this figure unless some external form of multiplexing is used which generates an effective register length greater than this. It is possible to use parameters which total less than 512 in order to implement a hardware pan function, but for the purpose of this example, we will assume that all of the bitmap is to be displayed. Thus:

$$MemInit + TransferDelay = 512$$

Transfer delay is

System DMA latency + VRAM access time + 4 Screen units

From the calculations in section 3.2.6:

TransferDelay	= 20
To provide some leeway TransferDelay	= 21

This extra screen unit takes into account the non-synchronisation between the T800 and the G300 clocks.

Which obeys the conditions for TransferDelay that:

$$TransferDelay < Backporch$$
$$TransferDelay < ShortDisplay$$

(These are the only screen related limitations on the value of the VRAM management parameters)

$$MemInit = 512 - 21 = 491 \text{ screen units.}$$

LineStart is the top of screen pointer and it can be programmed to any value but with the following restrictions.

If the bitmap is to appear byte-linear to the processor, the SAM start address must be zero.

The SAM start address must never become greater than (512 – TransferDelay)

A.2 EMI configuration program data

Device selection - T800-20
External Memory Interface clock period (Tm) = 25 ns
Input clock frequency = 5000khz
Wait States = 0

Address setup time		T1 = 1 periods Tm
Address hold time		T2 = 1 periods Tm
Read cycle tristate / Write data setup		T3 = 1 periods Tm
Extended for wait		T4 = 3 periods Tm
Read or write data		T5 = 1 periods Tm
End tristate / Data hold		T6 = 1 periods Tm
Programmable strobe **notMemS1**	**1**	S1 = 4 periods Tm
Programmable strobe **notMemS2**	**2**	S2 = 1 periods Tm
Programmable strobe **notMemS3**	**3**	S3 = 2 periods Tm
Programmable strobe **notMemS4**	**4**	S4 = 7 periods Tm

Refresh period	72 clockin periods	Wait	0
Write mode	Early	Configuration	-

Non-Programmable strobe (S0)	**notMemS0**	0
Read cycle strobe	**notMemRd**	r
Write cycle strobe	**notMemWrB**	w

Symbol	Parameter	min (ns)	max (ns)	notes
T0L0L	Cycle time	200	-	= 4 processor cycles
TAVQV	Address access time	-	175	
T0LQV	Access time from 0	-	150	
TrLQV	Access time from r	-	100	
TAV0L	Address setup time	25	-	
T0LAX	Address hold time	25	-	
TrHQX	Read data hold time	0	-	
TrHQZ	Read data turn off	-	25	
T0L0H	0 pulse width low	150	-	
T0H0L	0 pulse width high	50	-	
TrLrH	r pulse width low	100	-	
TrL0H	Effective r width	100	-	
T0LwL	0 to w delay	25	-	
TDVwL	Write data setup time	0	-	
TwLDX	Write data hold time 1	150	-	
TwHDX	Write data hold time 2	25	-	
TwLwH	Write pulse width	125	-	
TwL0H	Effective w width	125	-	

Table A.2 Timing for 4 cycles

#7FFFFF6C	-	0	#7FFFFFB4	-	0
#7FFFFF70	-	0	#7FFFFFB8	-	0
#7FFFFF74	-	0	#7FFFFFBC	-	0
#7FFFFF78	-	0	#7FFFFFC0	-	0
#7FFFFF7C	-	0	#7FFFFFC4	-	0
#7FFFFF80	-	0	#7FFFFFC8	-	1
#7FFFFF84	-	0	#7FFFFFCC	-	0
#7FFFFF88	-	1	#7FFFFFD0	-	0
#7FFFFF8C	-	0	#7FFFFFD4	-	0
#7FFFFF90	-	0	#7FFFFFD8	-	1
#7FFFFF94	-	0	#7FFFFFDC	-	1
#7FFFFF98	-	0	#7FFFFFE0	-	1
#7FFFFF9C	-	0	#7FFFFFE4	-	0
#7FFFFFA0	-	0	#7FFFFFE8	-	0
#7FFFFFA4	-	1	#7FFFFFEC	-	1
#7FFFFFA8	-	0	#7FFFFFF0	-	1
#7FFFFFAC	-	0	#7FFFFFF4	-	1
#7FFFFFB0	-	1	#7FFFFFF8	-	0

Table A.3 Configuration table

Symbol	Parameter	min (ns)	max (ns)	notes
T1L1H	1 pulse width	100	-	
T1H1L	1 precharge time	100	-	
T3L3H	3 pulse width	100	-	
T3H3L	3 precharge time	100	-	
T1L2L	1 to 2 delay	25	-	
T2L3L	2 to 3 delay	25	-	
T1L3L	1 to 3 delay	50	50	
T1LQV	Access time from 1	-	150	
T2LQV	Access time from 2	-	125	
T3LQV	Access time from 3	-	100	
T3L1H	1 hold (from 3)	50	-	
T1L3H	3 hold (from 1)	150	-	
TwL3H	w to 3 lead time	125	-	
TwL1H	w to 1 lead time	75	-	
T1LwH	w hold (from 1)	150	-	
T1LDX	Wr data hold from 1	175	-	
T3HQZ	Read data turn off	-	25	
TRFSH	256 refresh cycles	-	3650	Time is in microseconds

Table A.4 DRAM timing parameters

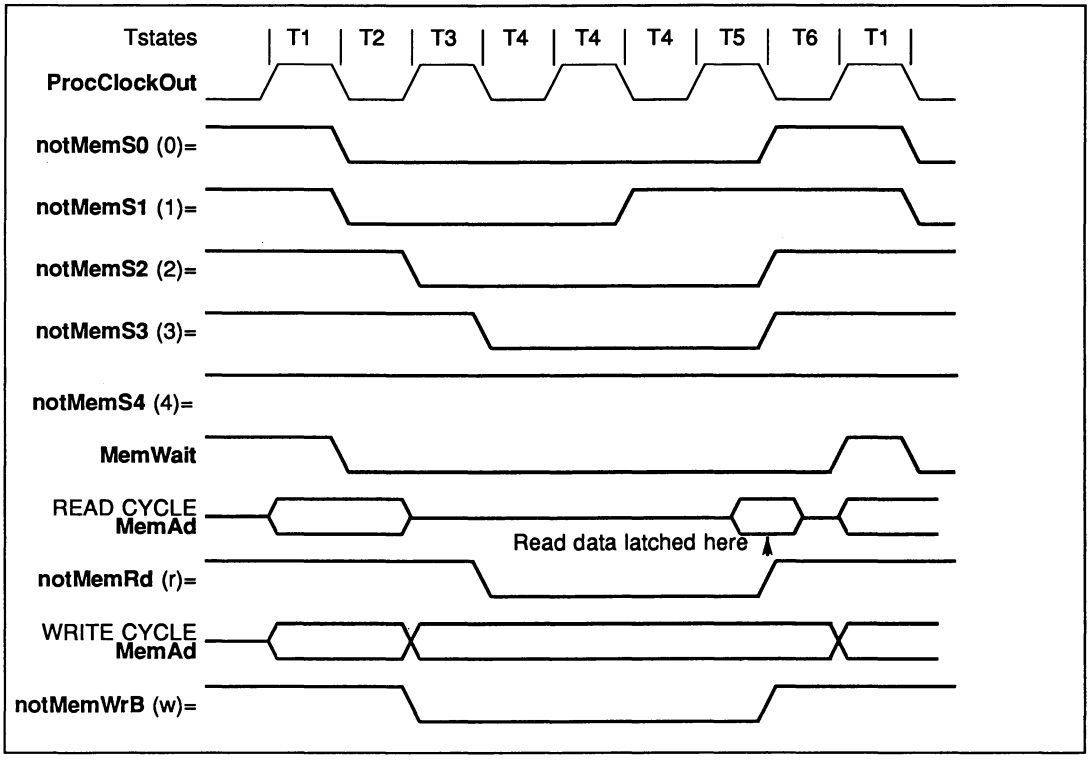


Figure A.2 Timing for basic memory cycle

Device selection - T800-20
External Memory Interface clock period (Tm) = 25 ns
Input clock frequency = 5000khz
Wait States = 4

Address setup time		T1 = 1 periods Tm
Address hold time		T2 = 1 periods Tm
Read cycle tristate / Write data setup		T3 = 1 periods Tm
Extended for wait		T4 = 3 periods Tm
Read or write data		T5 = 1 periods Tm
End tristate / Data hold		T6 = 1 periods Tm
Programmable strobe **notMemS1**	**1**	S1 = 4 periods Tm
Programmable strobe **notMemS2**	**2**	S2 = 1 periods Tm
Programmable strobe **notMemS3**	**3**	S3 = 2 periods Tm
Programmable strobe **notMemS4**	**4**	S4 = 7 periods Tm

Refresh period	72 clockin periods	Wait	7
Write mode	Early	Configuration	-

Non-Programmable strobe (S0)	**notMemS0**	0
Read cycle strobe	**notMemRd**	r
Write cycle strobe	**notMemWrB**	w

Symbol	Parameter	min (ns)	max (ns)	notes
T0L0L	Cycle time	300	-	= 6 processor cycles
TAVQV	Address access time	-	275	
T0LQV	Access time from 0	-	250	
TrLQV	Access time from r	-	200	
TAV0L	Address setup time	25	-	
T0LAX	Address hold time	25	-	
TrHQX	Read data hold time	0	-	
TrHQZ	Read data turn off	-	25	
T0L0H	0 pulse width low	250	-	
T0H0L	0 pulse width high	50	-	
TrLrH	r pulse width low	200	-	
TrL0H	Effective r width	200	-	
T0LwL	0 to w delay	50	-	
TDVwL	Write data setup time	25	-	
TwLDX	Write data hold time 1	225	-	
TwHDX	Write data hold time 2	25	-	
TwLwH	Write pulse width	200	-	
TwL0H	Effective w width	200	-	

Table A.5 Timing for extended cycles

#7FFFFF6C	-	0	#7FFFFFB4	-	0
#7FFFFF70	-	0	#7FFFFFB8	-	0
#7FFFFF74	-	0	#7FFFFFBC	-	0
#7FFFFF78	-	0	#7FFFFFC0	-	0
#7FFFFF7C	-	0	#7FFFFFC4	-	0
#7FFFFF80	-	0	#7FFFFFC8	-	1
#7FFFFF84	-	0	#7FFFFFCC	-	0
#7FFFFF88	-	1	#7FFFFFD0	-	0
#7FFFFF8C	-	0	#7FFFFFD4	-	0
#7FFFFF90	-	0	#7FFFFFD8	-	1
#7FFFFF94	-	0	#7FFFFFDC	-	1
#7FFFFF98	-	0	#7FFFFFE0	-	1
#7FFFFF9C	-	0	#7FFFFFE4	-	0
#7FFFFFA0	-	0	#7FFFFFE8	-	0
#7FFFFFA4	-	1	#7FFFFFEC	-	1
#7FFFFFA8	-	0	#7FFFFFF0	-	1
#7FFFFFAC	-	0	#7FFFFFF4	-	1
#7FFFFFB0	-	1	#7FFFFFF8	-	0

Table A.6 Configuration table

Symbol	Parameter	min (ns)	max (ns)	notes
T1L1H	1 pulse width	100	-	
T1H1L	1 precharge time	200	-	
T3L3H	3 pulse width	200	-	
T3H3L	3 precharge time	100	-	
T1L2L	1 to 2 delay	25	-	
T2L3L	2 to 3 delay	25	-	
T1L3L	1 to 3 delay	50	50	
T1LQV	Access time from 1	-	250	
T2LQV	Access time from 2	-	225	
T3LQV	Access time from 3	-	200	
T3L1H	1 hold (from 3)	50	-	
T1L3H	3 hold (from 1)	250	-	
TwL3H	w to 3 lead time	200	-	
TwL1H	w to 1 lead time	50	-	
T1LwH	w hold (from 1)	250	-	
T1LDX	Wr data hold from 1	275	-	
T3HQZ	Read data turn off	-	25	
TRFSH	256 refresh cycles	-	3650	Time is in microseconds

Table A.7 CVC access timing

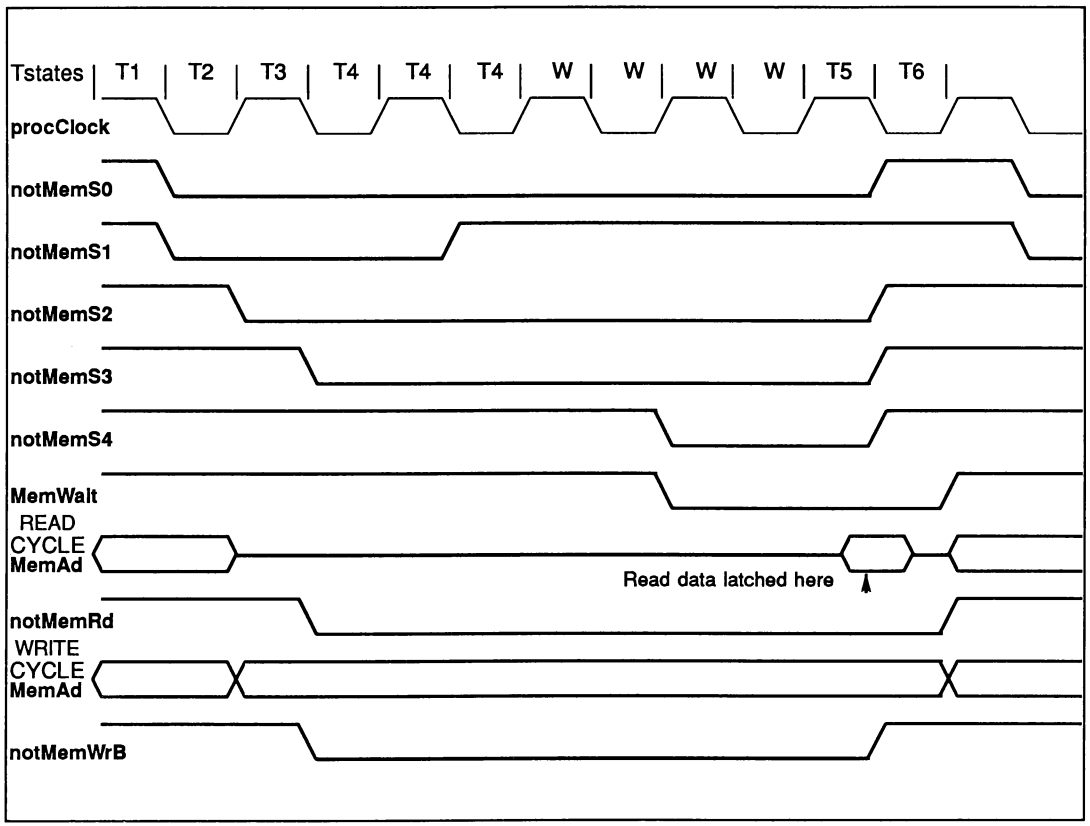


Figure A.3 Timing for extended memory cycle

A.3 CUPL listings of PAL programs

```
PARTNO          003;
NAME            MCA01;
REVISION        0.1;
DATE            12/14/88;
DESIGNER        Dave Japp;
COMPANY         INMOS LIMITED;
ASSEMBLY        G300 Tram;
LOCATION        IC7;
DEVICE          p1618;

/** Configuration and SubSystem Control **/

/** INPUTS **/

pin 1    = LA31          ;
pin 2    = LA2           ;
pin 3    = LA3           ;
pin 4    = LA4           ;
pin 5    = LA5           ;
pin 6    = LA6           ;
pin 7    = LA7           ;
pin 8    = LA30          ;
pin 9    = notMemRd      ;
pin 11   = notSubError   ;

/**   Outputs    **/

pin 19  =  AD0              ;
pin 18  =  notMemWrB0       ;
pin 17  =  MC               ;
pin 16  =  G300SwClk        ;
pin 15  =  G300ResetClk     ;
pin 14  =  MemConfig        ;
pin 13  =  ResetClk         ;
pin 12  =  AnalyseClk       ;

/** Decode  for   Reset  and  Analyse  and   G300 functions   **/
/** SubSys @ \#00000000, \#00000004 . G300 @ \#000000F0, \#000000F4 **/

RDecode       = ( !LA31 & !LA30 & !LA7 & !LA6 & !LA5 & !LA4 & !LA3 & !LA2 )
;
ResetClk      = notMemWrB0  # ! RDecode ;

AnaDecode     = ( !LA31 & !LA30 & !LA7 & !LA6 & !LA5 & !LA4 & !LA3 &  LA2 )
;
AnalyseClk    = notMemWrB0 #  ! AnaDecode ;

GRDecode      = ( !LA31 & !LA30 &  LA7 &  LA6 &  LA5 &  LA4 & !LA3 & !LA2 )
;
G300ResetClk = notMemWrB0 #  ! GRDecode ;

GSDecode      = ( !LA31 & !LA30 &  LA7 &  LA6 &  LA5 &  LA4 & !LA3 &  LA2 )
;
G300SwClk     = notMemWrB0 #  ! GSDecode ;


AD0.OE       = !LA31 & !LA30 & !LA2 &        !LA4 & !LA5 & !LA6 & !LA7 &
                 !notMemRd
```

```
!AD0        = notSubError & !LA3 # LA3

/** T800 EMI Configuration Data **/

!MC         =    LA7 & !LA6 & !LA5 & !LA4 &  LA3 & !LA2
               #  LA7 & !LA6 &  LA5 & !LA4 & !LA3 &  LA2
               #  LA7 & !LA6 &  LA5 &  LA4 & !LA3 & !LA2
               #  LA7 &  LA6 & !LA5 & !LA4 &  LA3 & !LA2
               #  LA7 &  LA6 & !LA5 &  LA4 &  LA3
               #  LA7 &  LA6 &  LA5 & !LA4 & !LA3 & !LA2
               #  LA7 &  LA6 &  LA5 & !LA4 &  LA3 &  LA2      ;

!MemConfig =    LA7 &  LA6 &  LA5 &  LA4 & !LA3 # !MC # LA31 ;
```

```
PARTNO          001;
NAME            LOC01;
REVISION        0.1 ;
DATE            02/13/89;
DESIGNER        Dave Japp;
COMPANY         INMOS LIMITED;
ASSEMBLY        G300 Tram;
LOCATION        IC25 ;
DEVICE          p1618;

/** Address Latch Output Control **/

/** INPUTS **/

pin 1    = notMemS0     ;
pin 2    = notMemS2     ;
pin 7    = notMemRf     ;
pin 8    = G3BusCycle   ;
pin 9    = G3ALE        ;
pin 11   = G3AMux       ;


/**   Outputs     **/

pin 19   = PS0           ;
pin 18   = PS1           ;
pin 17   = PS2           ;
pin 16   = notT8G3HoOe   ;
pin 15   = notT8LoOe     ;
pin 14   = notG3LoOe     ;
pin 13   = notALE        ;


/** Latch Enable/Ouput Control **/

notALE = ( notMemS0 & !G3ALE )                                    ;

notT8G3HoOe = ! (  ( notMemS2 & notMemRf & !G3BusCycle ) #
                   ( G3AMux   & notMemRf &  G3BusCycle )   ) ;

notT8LoOe   = ! (  ( !notMemS2 & notMemRf & !G3BusCycle ) #
                   ( !G3BusCycle & !notMemRf ) )                  ;

notG3LoOe   =    ! ( !G3AMux   & notMemRf &  G3BusCycle )     ;


/** T800 Speed Selection **/

!PS0        = 'B'1 ;

!PS1        = 'B'1 ;

!PS2        = 'B'1 ;
```

```
PARTNO          002;
NAME            RCG00;
REVISION        0.1;
DATE            12/08/88;
DESIGNER        Dave Japp;
COMPANY         INMOS LIMITED;
ASSEMBLY        G300 Tram;
LOCATION        IC26 ;
DEVICE          p1618;

/** Row and Column Address Strobe Generation **/

/** INPUTS **/

pin 1    = notMemS1     ;
pin 2    = notMemS3     ;
pin 4    = notMemRf     ;
pin 5    = LA11         ;
pin 6    = notEnVram    ;
pin 7    = notEnDram    ;
pin 8    = MemGrant     ;
pin 9    = G3Ras        ;
pin 11   = G3Cas        ;

/**   Outputs    **/

pin 19   = notDramRas0  ;
pin 18   = notDramRas1  ;
pin 17   = notVramRas0  ;
pin 16   = notVramRas1  ;
pin 15   = notDramCas0  ;
pin 14   = notDramCas1  ;
pin 13   = notVramCas0  ;
pin 12   = notVramCas1  ;

/** Ras, Cas Generation **/
/**  Vram, Dram  Ras   **/

notVramRas0 = ! ( ( !notMemS1 & !notMemRf ) #
                  ( !notMemS1 & !notEnVram & !LA11 ) #
                  ( G3Ras & MemGrant ) )                    ;
notVramRas1 = ! ( ( !notMemS1 & !notMemRf ) #
                  ( !notMemS1 & !notEnVram &  LA11 ) #
                  ( G3Ras & MemGrant ) )                    ;
notDramRas0 = ! ( ( !notMemS1 & !notMemRf ) #
                  ( !notMemS1 & !notEnDram & !LA11 ) )      ;
notDramRas1 = ! ( ( !notMemS1 & !notMemRf ) #
                  ( !notMemS1 & !notEnDram &  LA11 ) )      ;

/**  Vram, Dram  Cas   **/

notVramCas0 = ! ( ( !notMemS3 & notMemRf & !notEnVram ) #
                  ( G3Cas & MemGrant ) )                    ;
notVramCas1 = ! ( ( !notMemS3 & notMemRf & !notEnVram ) #
                  ( G3Cas & MemGrant ) )                    ;
notDramCas0 = ! ( ( !notMemS3 & notMemRf & !notEnDram ) ) ;

notDramCas1 = ! ( ( !notMemS3 & notMemRf & !notEnDram ) ) ;
```

A.4 TRAM pin description

Pin	In/Out	Function	Pin No.
System Services			
Vcc, GND		Power supply and return	3,14
ClockIn	in	5MHz clock signal	8
Reset	in	Transputer reset	10
Analyse	in	Transputer error analysis	9
notError	out	Transputer error indicator	11
Links			
LinkIn0-3	in	INMOS serial link inputs to transputer	13,5,2,16
LinkOut0-3	out	INMOS serial link outputs from transputer	12,4,1,15
LinkspeedA,B	in	Transputer link speed selection	6,7

Table A.8 TRAM Pin designations

Notes:

1 Signal names are prefixed by **not** if they are active low; otherwise they are active high.

LinkOut0-3 Transputer link output signals. These outputs are intended to drive into transmission lines with a characteristic impedance of 100Ω. They can be connected directly to the **LinkIn** pins of other transputers or TRAMs.

LinkIn0-3 Transputer link input signals. These are the link inputs of the transputer on the IMS B407. Each input has a 10kΩ resistor to **GND** to establish the idle state, and a diode to **Vcc** as protection against ESD. They can be connected directly to the **LinkOut** pins of other transputers or TRAMs.

LinkSpeedA, LinkSpeedB select the speeds of the communication links. Table A.9 shows the combinations defined for present TRAMs.

LinkSpeedA	LinkSpeedB	Link Speeds
0	0	All links 10 Mbits/s
0	1	TRAM specific
1	0	TRAM specific
1	1	All links 20 Mbits/s

Table A.9 Link speed selection

ClockIn A 5MHz input clock for the transputer. The transputer synthesises its own high frequency clocks. **ClockIn** should have a stability over time and temperature of 200ppm. **ClockIn** edges should be monotonic within the range 0.8V to 2.0V with a rise/fall time of less than 8ns.

Reset Resets the transputer, and other circuitry. **Reset** should be asserted for a minimum of 100ms. After **Reset** is deasserted a further 100ms should elapse before communication is attempted on any link. After this time, the transputer on the TRAM is ready to accept a boot packet on any of its links.

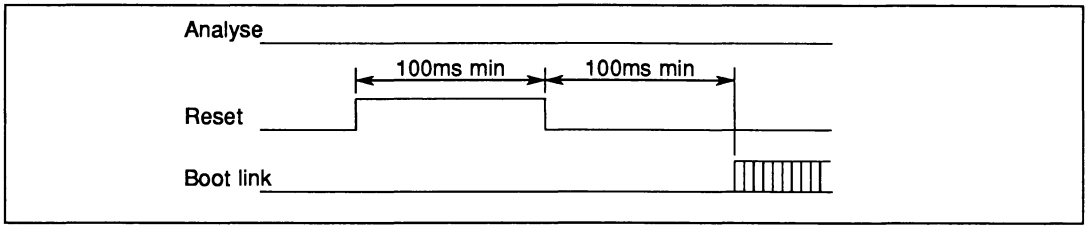


Figure A.4 Reset timing

Analyse is used, in conjunction with **Reset**, to stop the transputer. It allows internal state to be examined so that the cause of an error may be determined. **Reset** and **Analyse** are used as shown in figure A.5. A processor in analyse mode can be interrogated on any of its links.

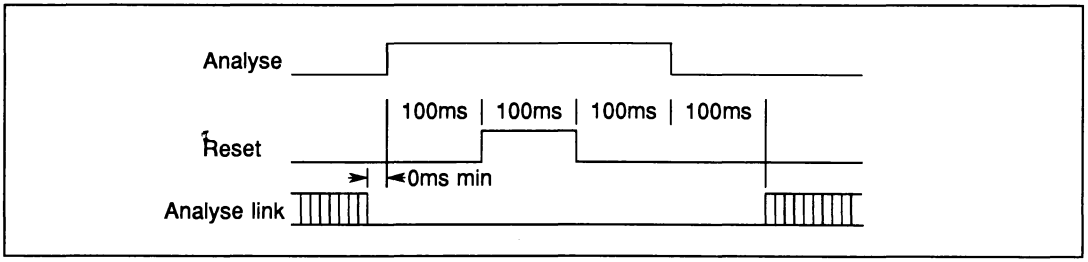


Figure A.5 Analyse timing

notError An open collector output which is pulled low when the transputer asserts its Error pin. **notError** should be pulled high by a 10kΩ resistor to **Vcc**. Up to 10 **notError** signals can be wired together. The combined error signal will be low when any of the contributing signals is low.

A.5 PCB profile drawing and pinout, TRAM Size6 with subsystem

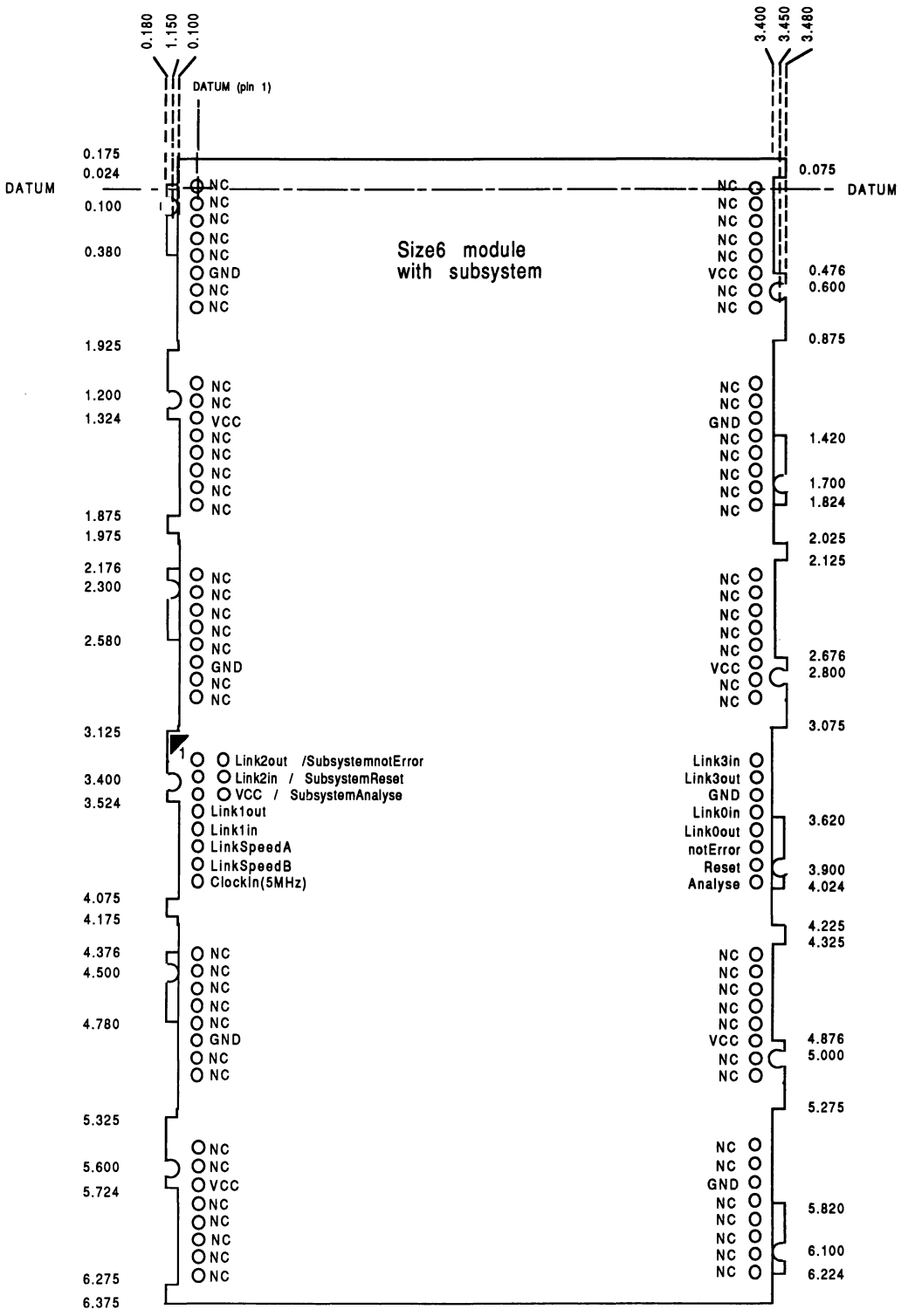

0.180
1.150
0.100
DATUM (pin 1)
3.400
3.450
3.480
0.175
0.024
DATUM
0.100
0.380
1.925
1.200
1.324
1.875
1.975
2.176
2.300
2.580
3.125
3.400
3.524
4.075
4.175
4.376
4.500
4.780
5.325
5.600
5.724
6.275
6.375
0.075
DATUM
0.476
0.600
0.875
1.420
1.700
1.824
2.025
2.125
2.676
2.800
3.075
3.620
3.900
4.024
4.225
4.325
4.876
5.000
5.275
5.820
6.100
6.224
NC
GND
VCC
Size6 module
with subsystem
Link2out /SubsystemnotError
Link2in / SubsystemReset
VCC / SubsystemAnalyse
Link1out
Link1in
LinkSpeedA
LinkSpeedB
ClockIn(5MHz)
Link3in
Link3out
Link0in
Link0out
notError
Reset
Analyse

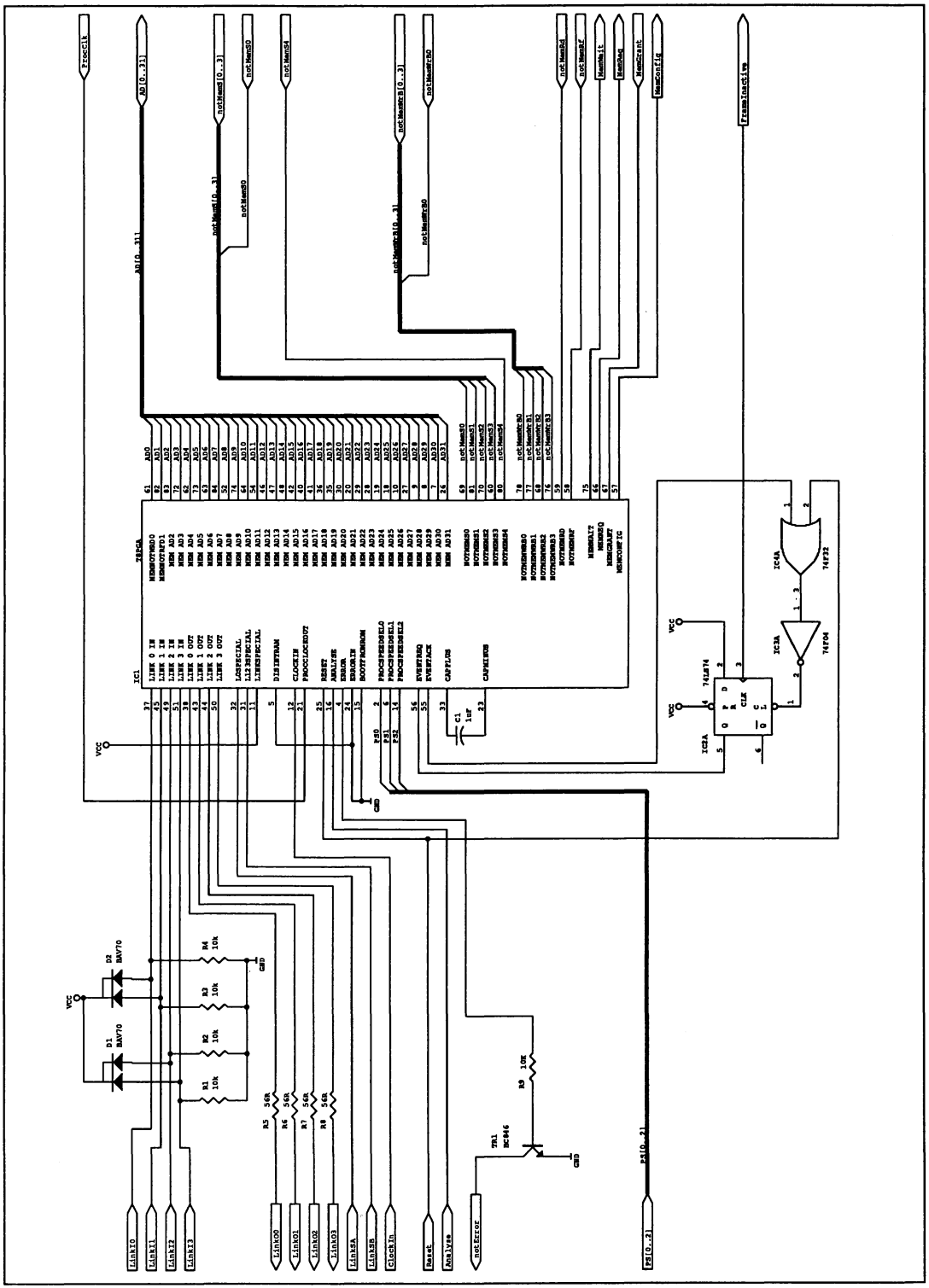
Figure A.6

A.6 Circuit diagrams

Notes:

1 The series termination resistors R10-R18, R19, R20, R21-28 and R29-R37 have arbitrary values which may be used for a guide. The actual values will have to be calculated for the particular layout used.

2 The analogue outputs from the G300 CVC must be treated as matched lines (75R). The track width and length will vary with the pcb material and layout.



72 TCH 062 00 June 1989

Figure A.7 T800

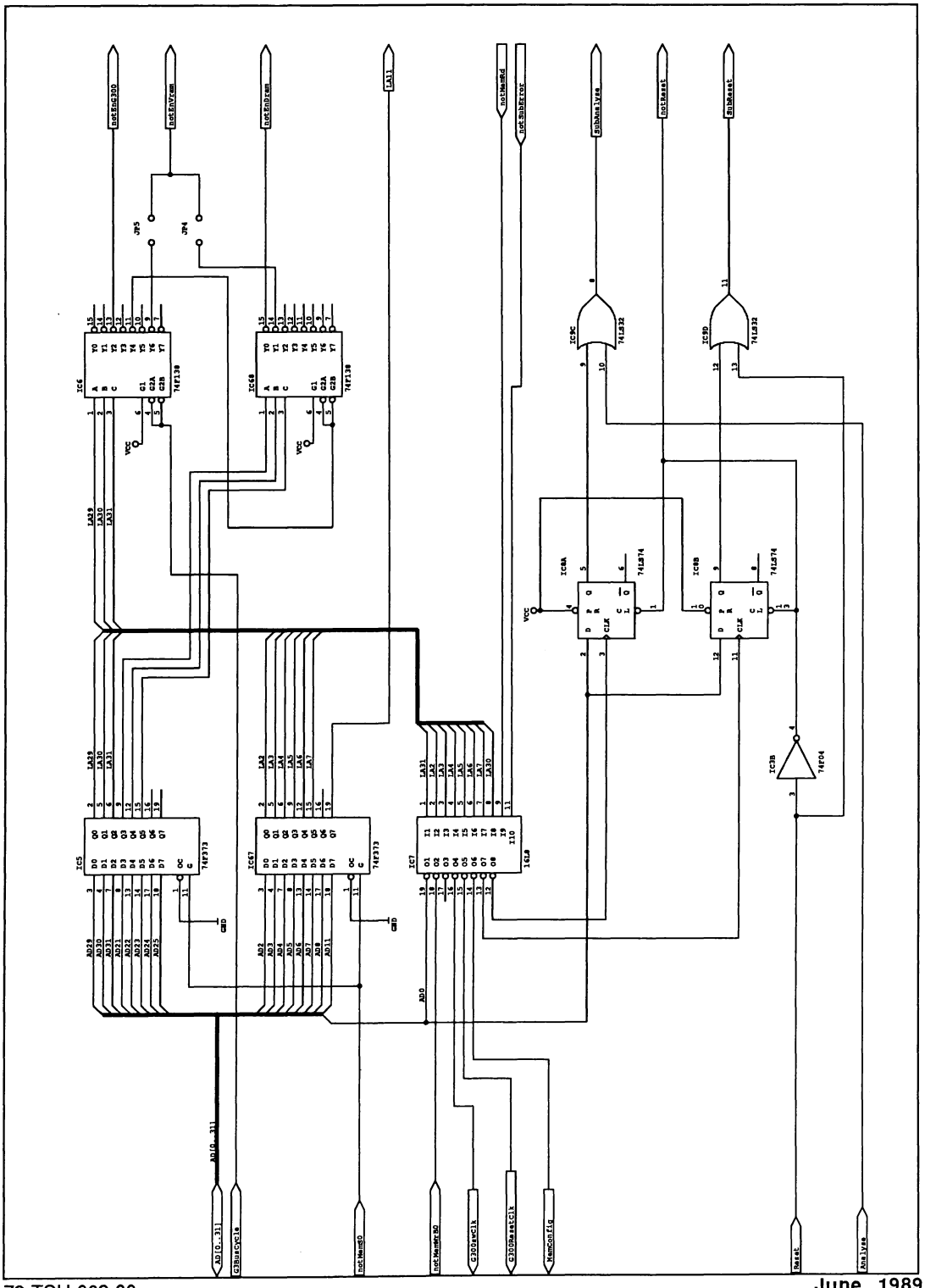


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Figure A.8 Address decode / configuration / subsystem

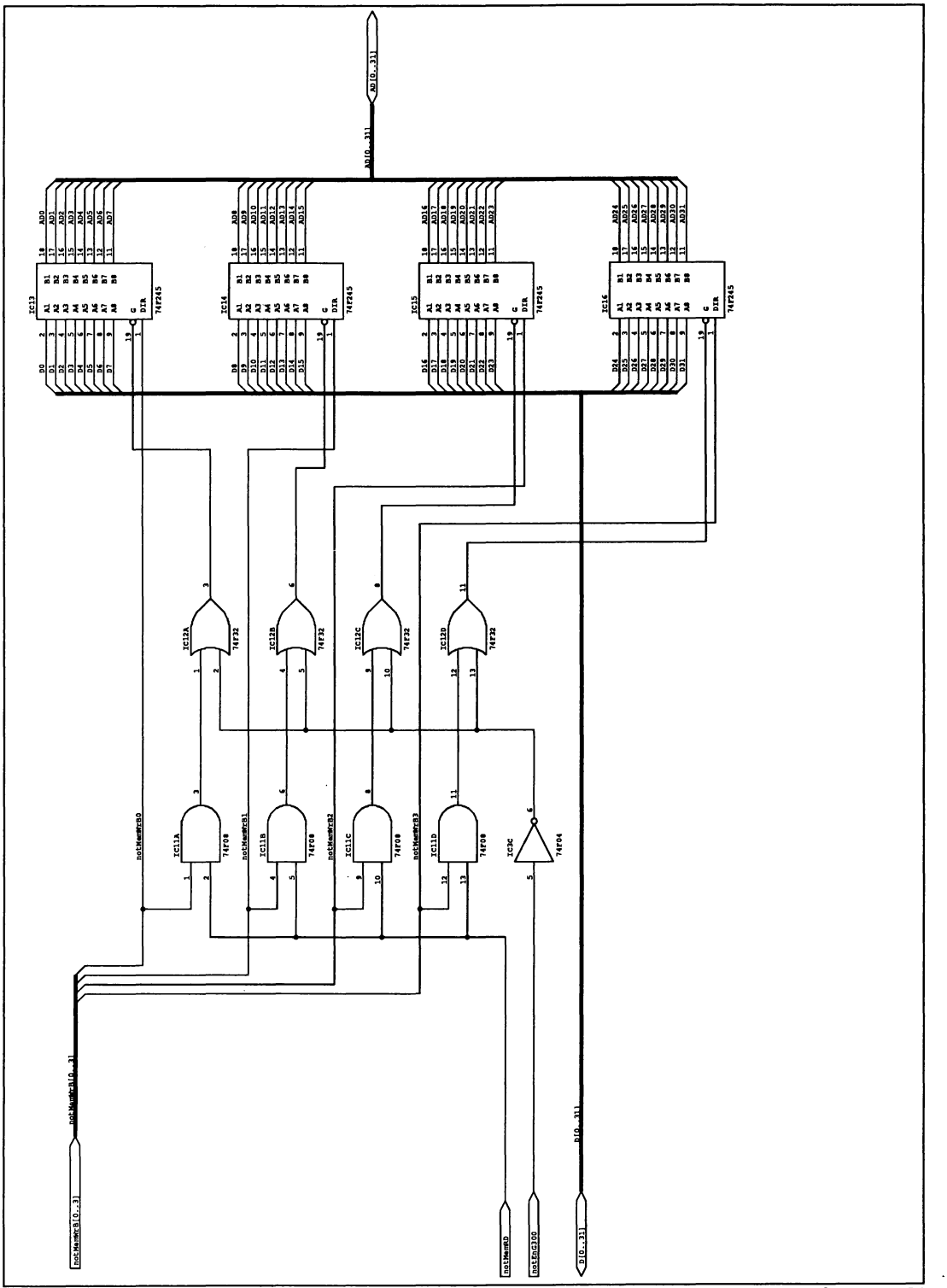

Figure A.9 Data buffers

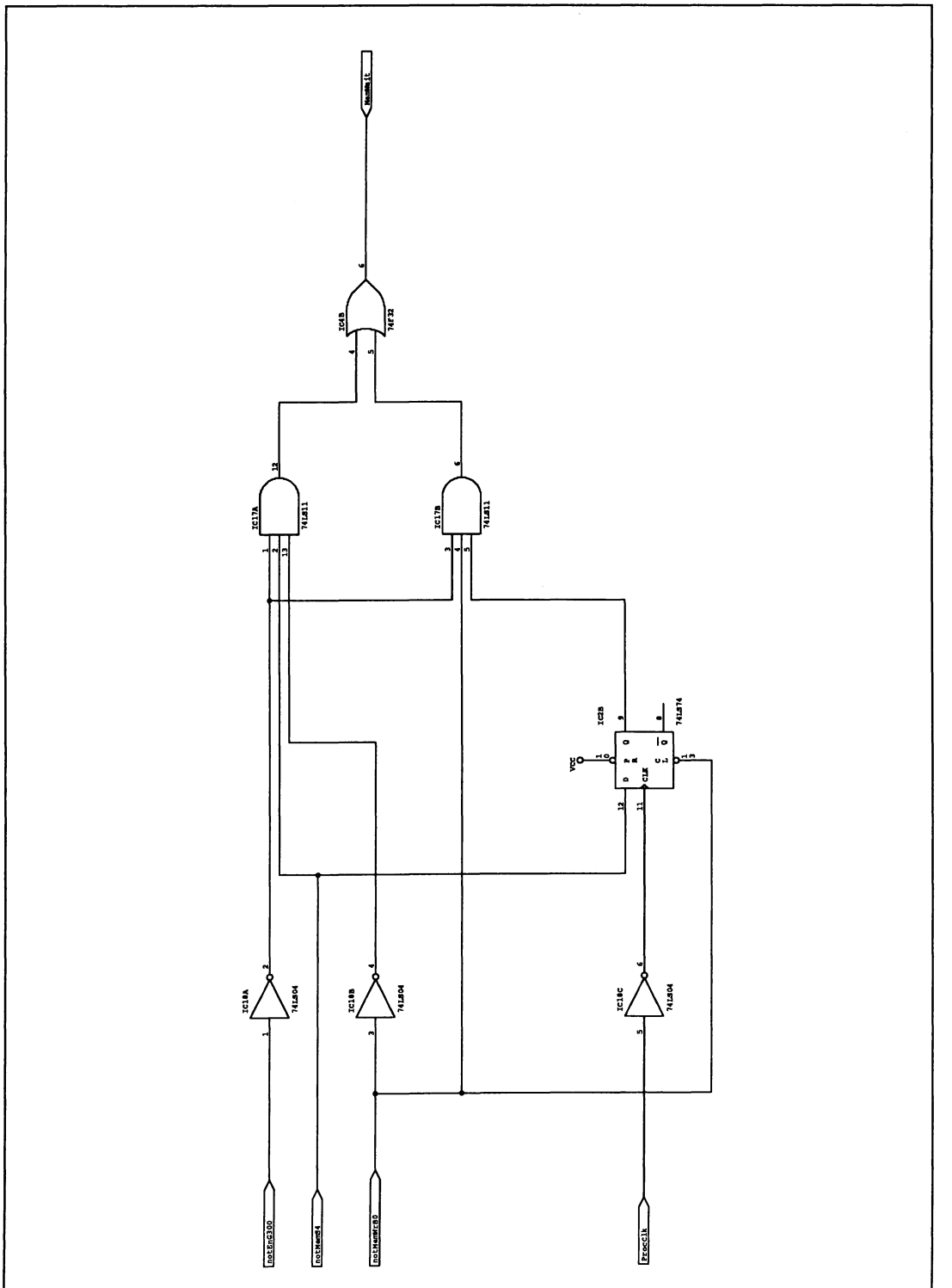

Figure A.10 Wait state generation

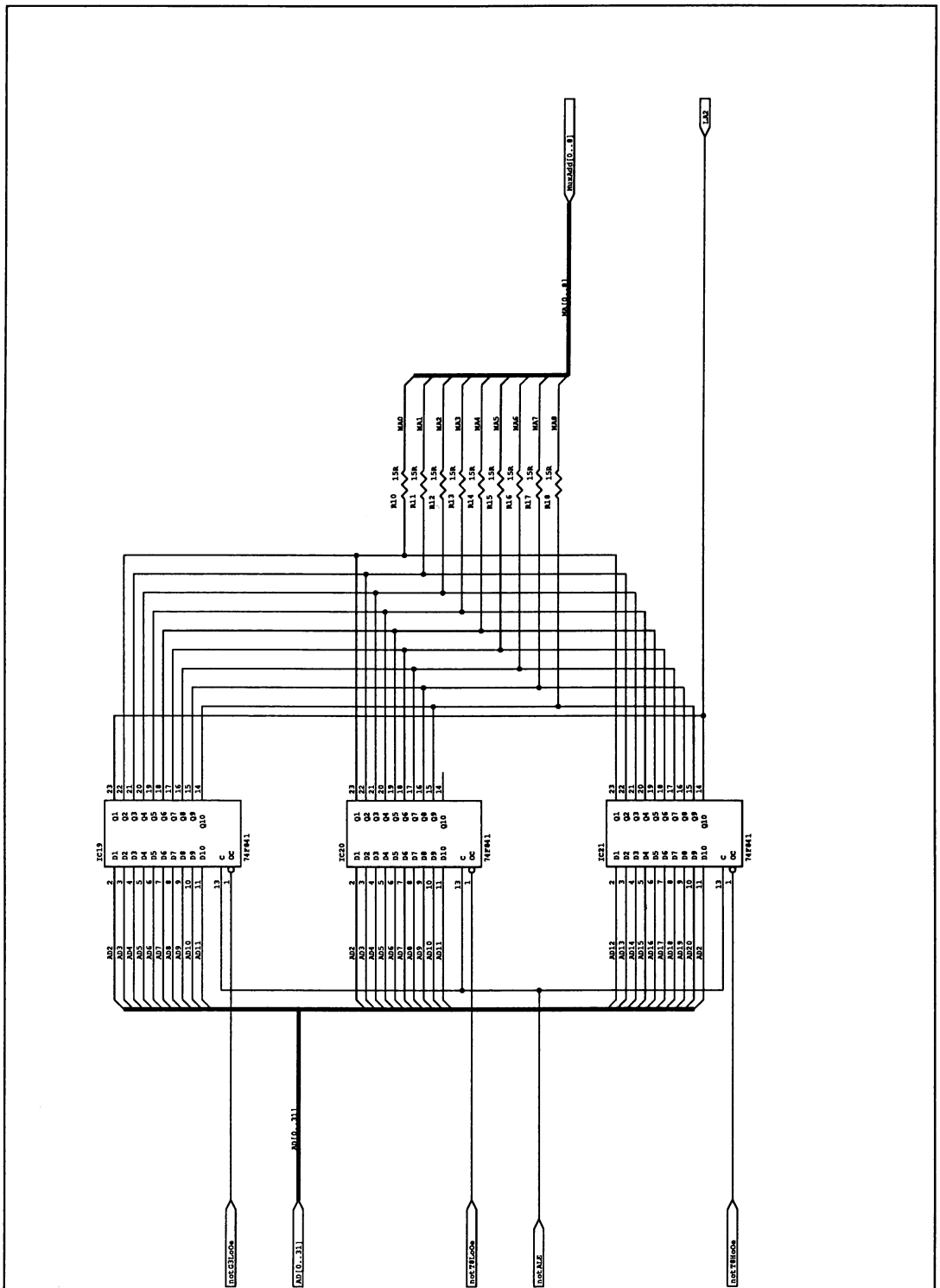

Figure A.11 Address latches

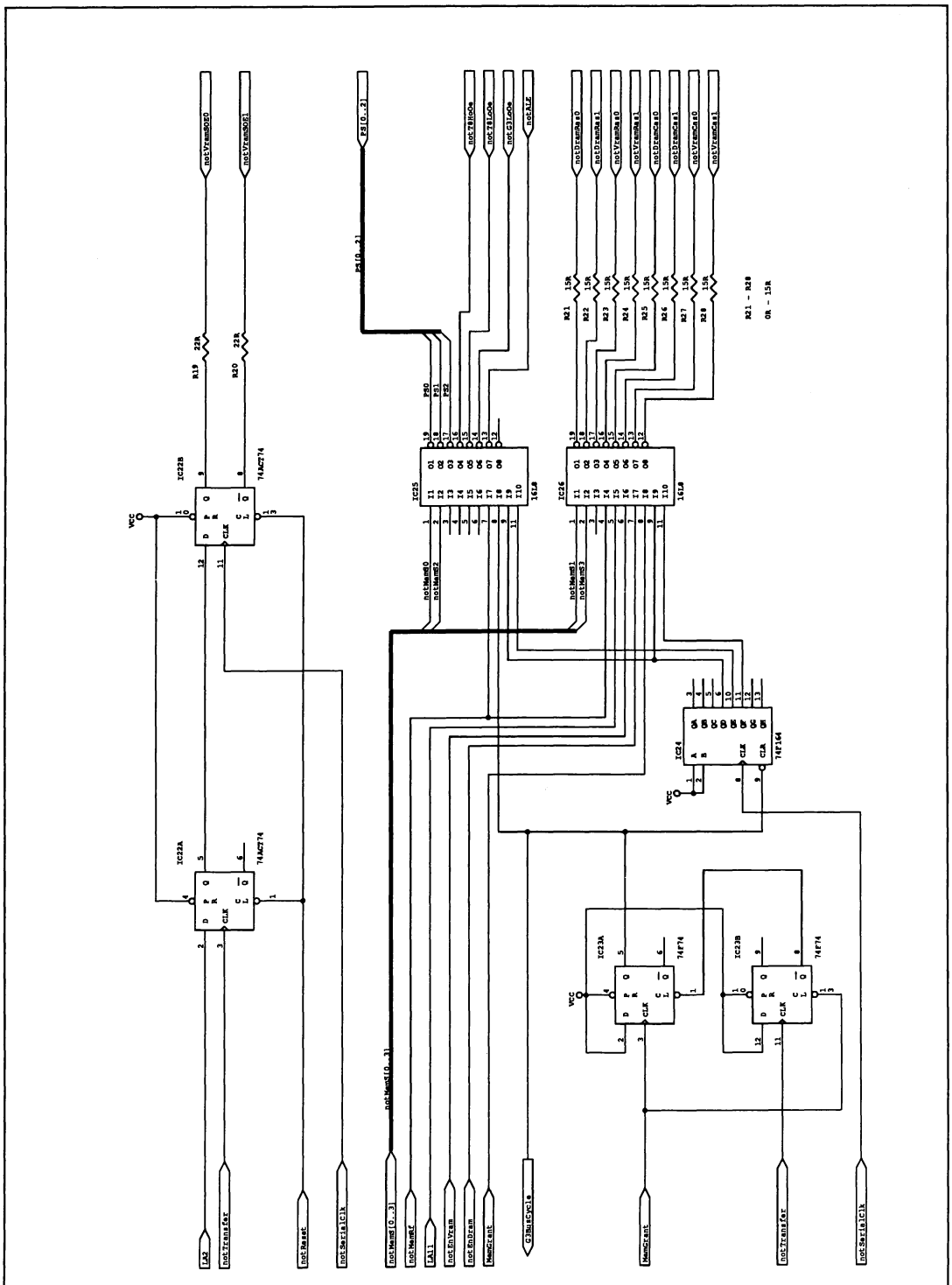

Figure A.12 SOE decode and drive / memory strobe generation

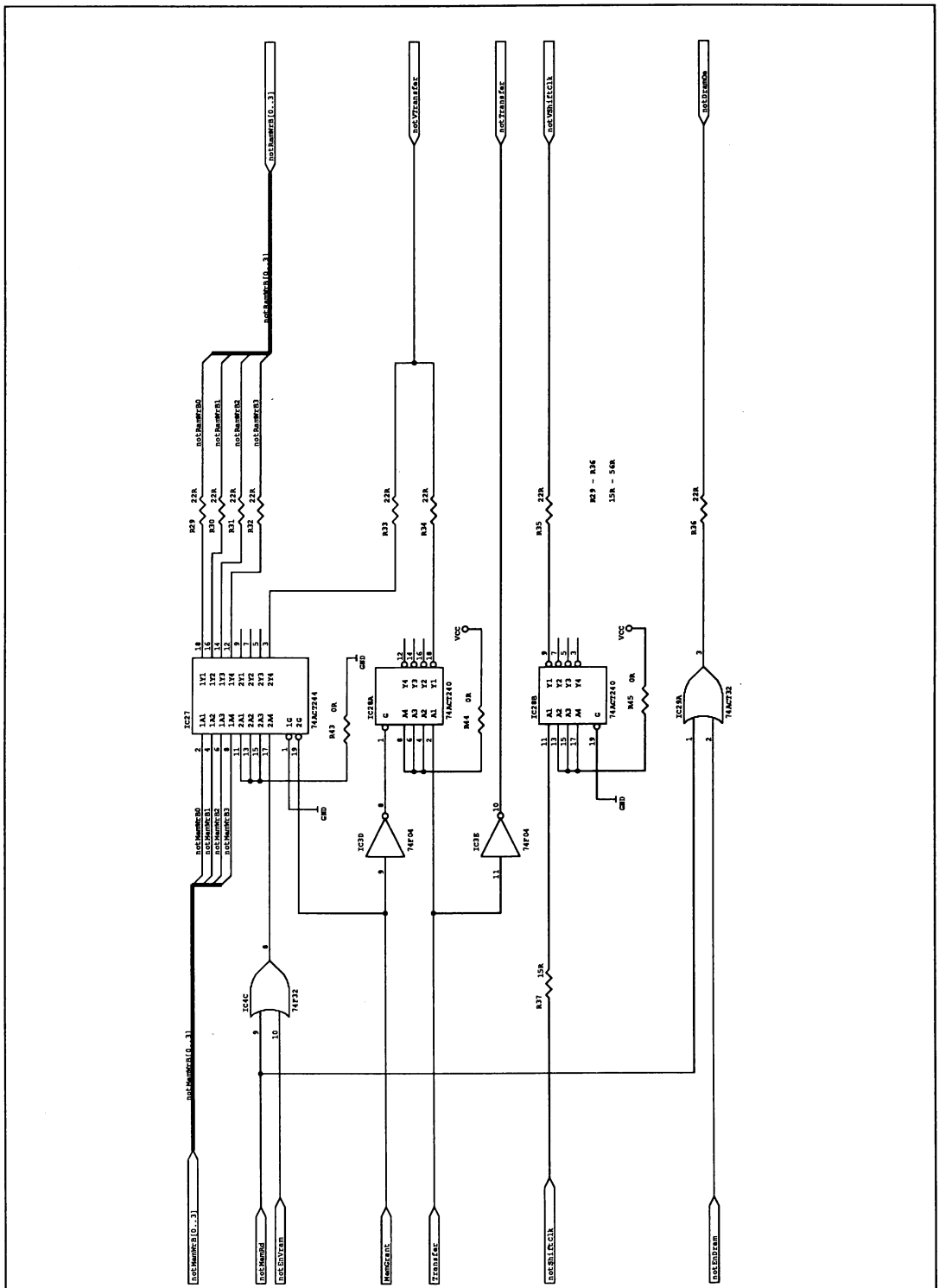

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Figure A.13 Memory strobe buffering

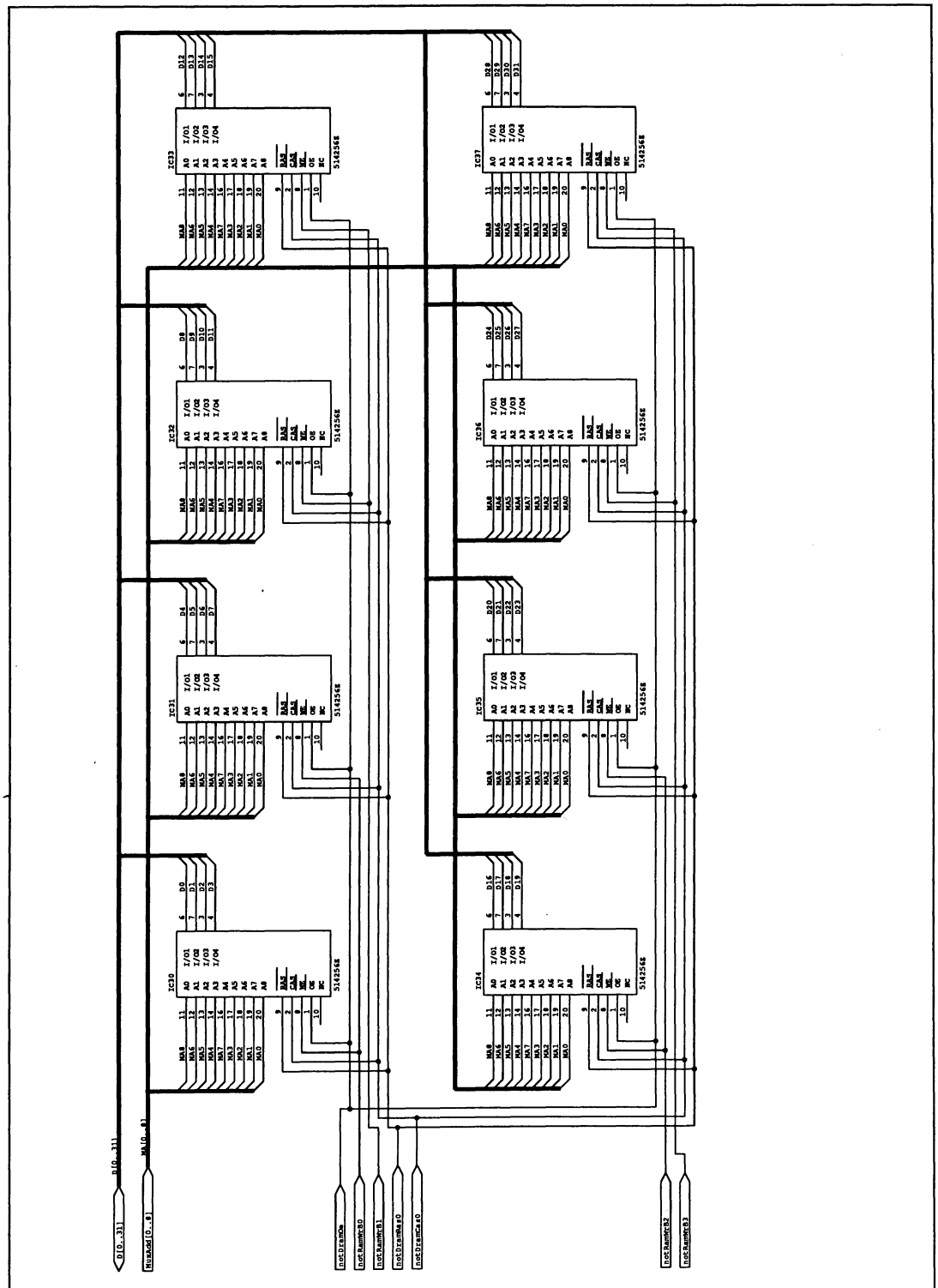


Figure A.14 DRAM bank 0

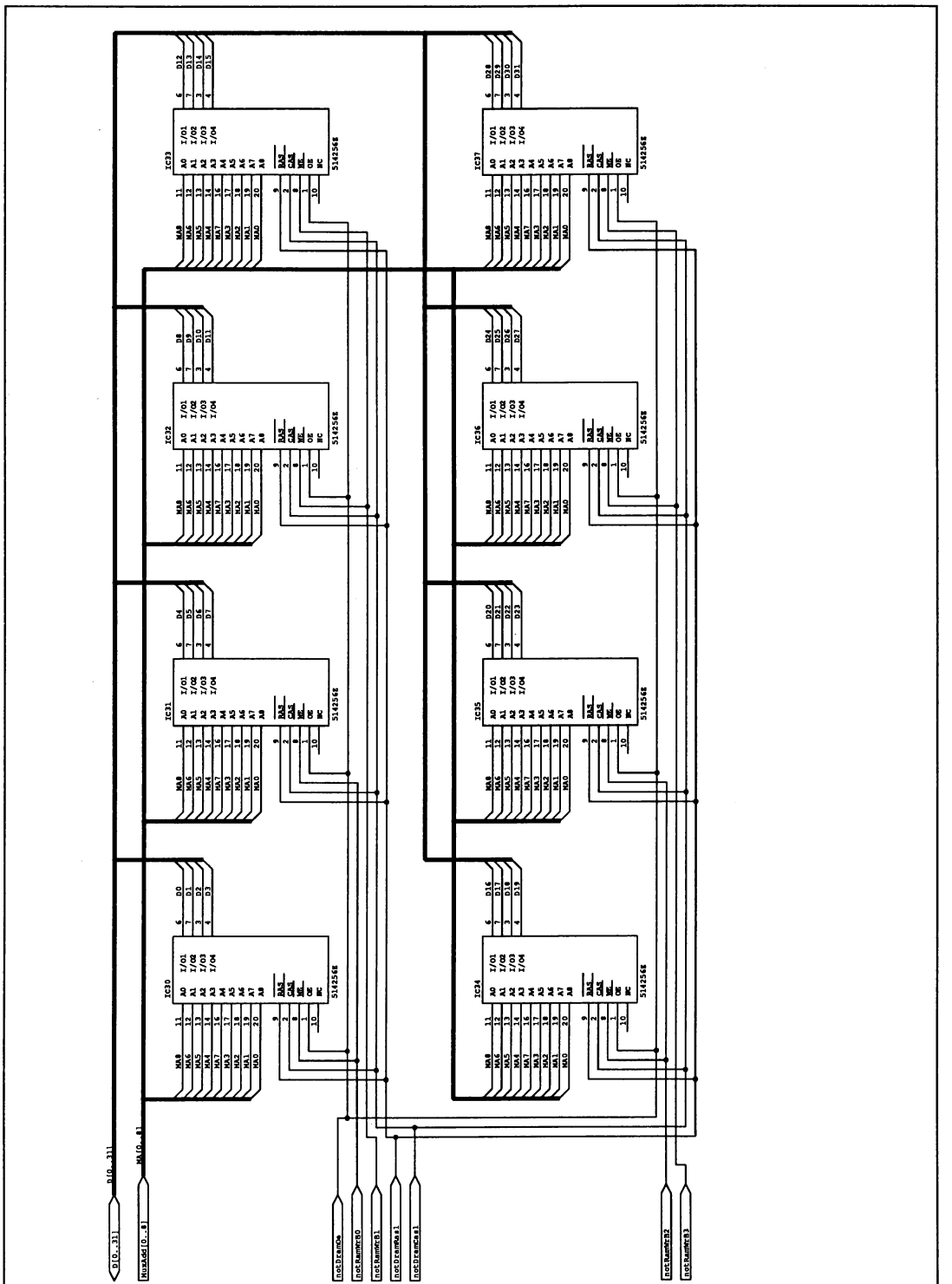


Figure A.15 DRAM bank 1

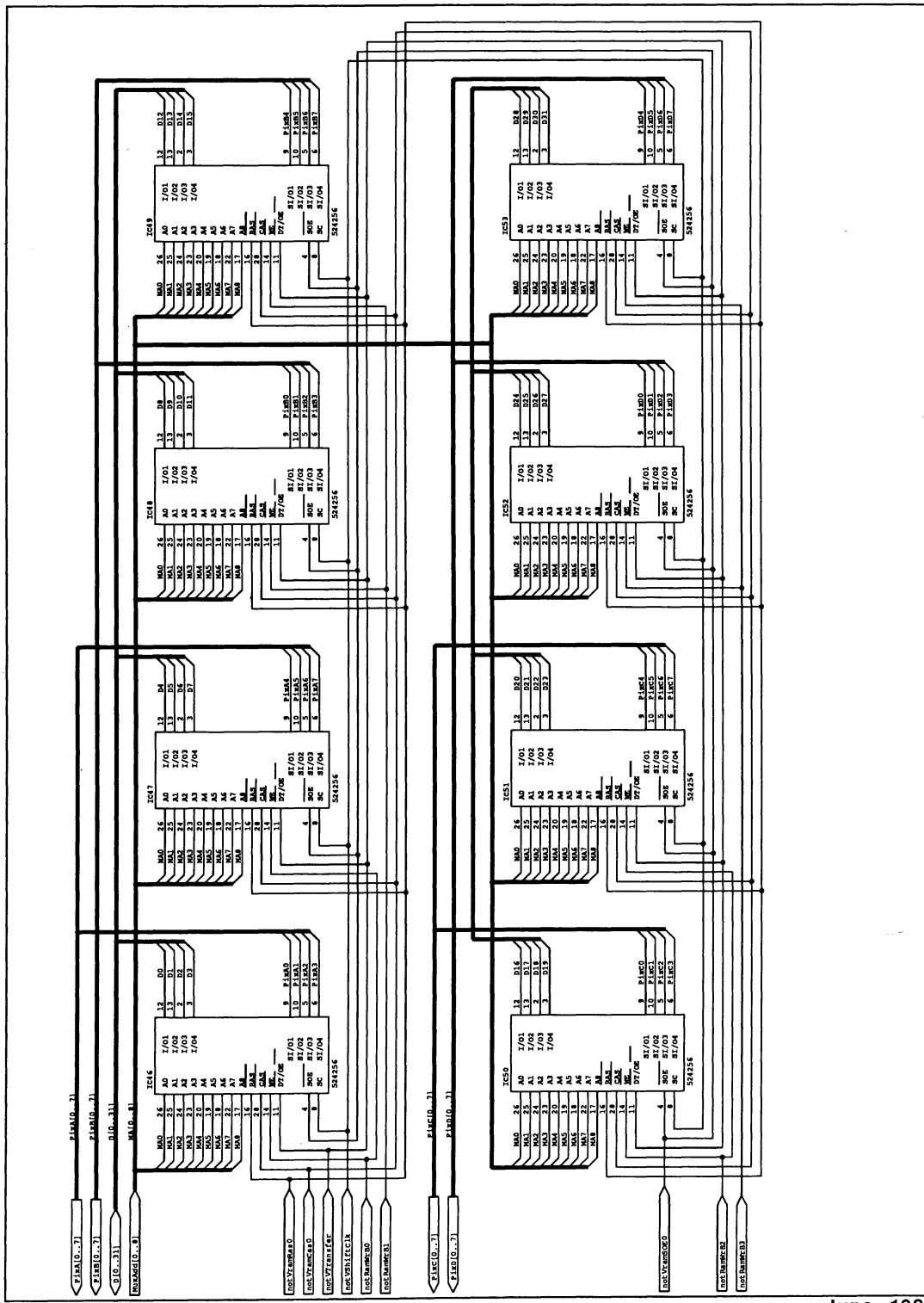


Figure A.16 VRAM bank 0

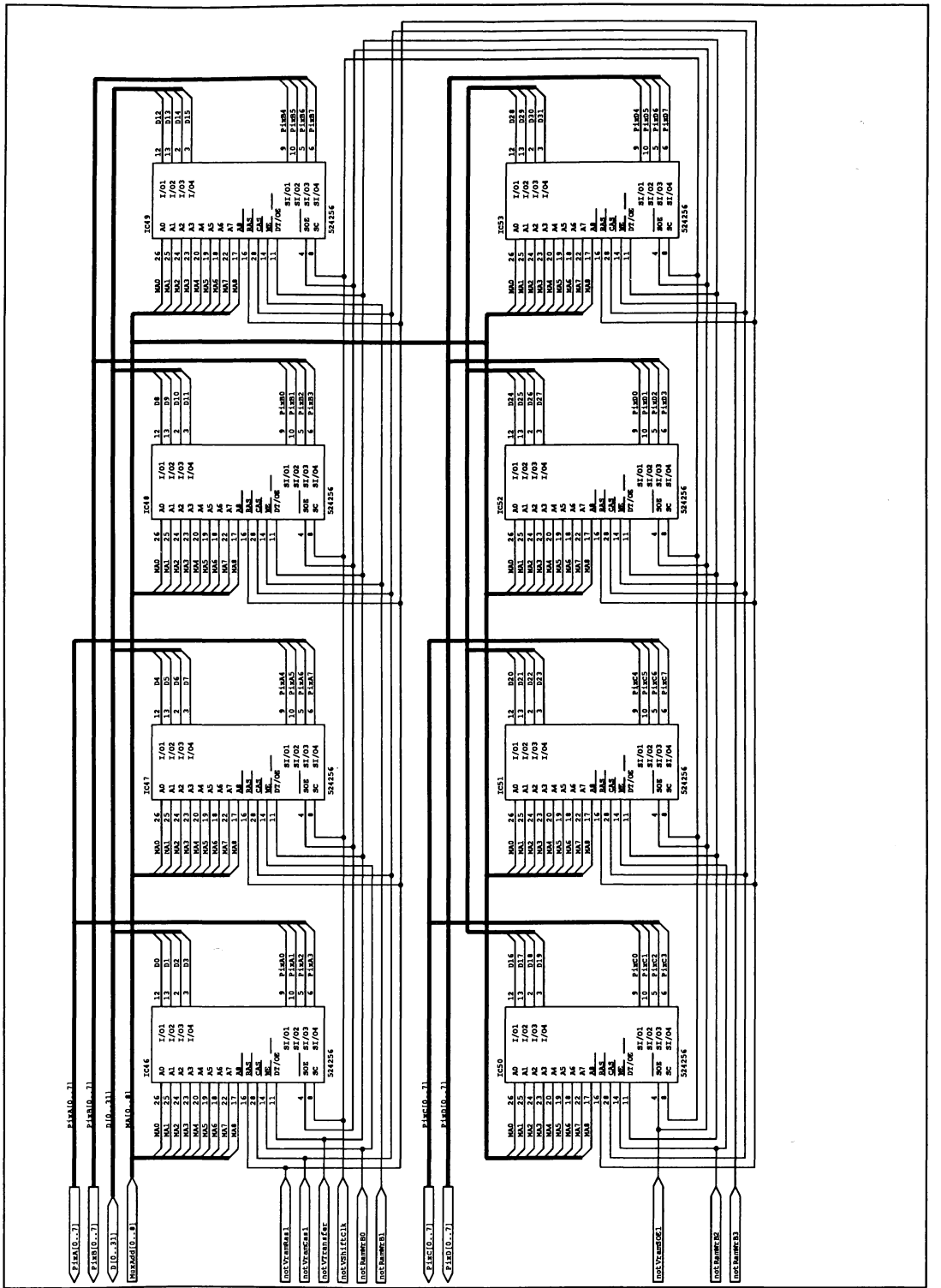


Figure A.17 VRAM bank 1

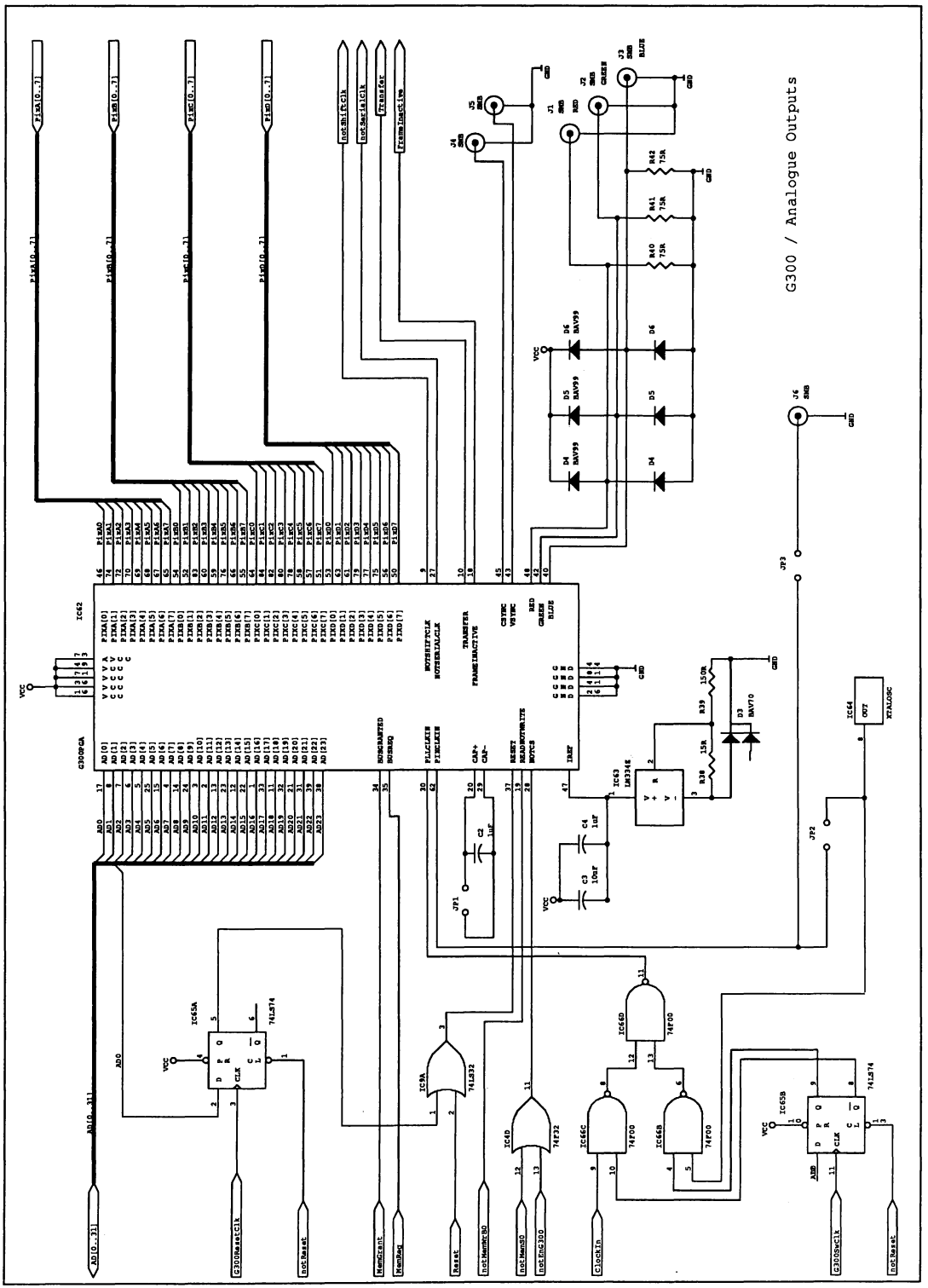


Figure A.18 G300 / analogue outputs

B Further reading

1 *IMS G300A Colour Video Controller* Data sheet, INMOS Limited

2 *Transputer databook*, INMOS Limited 1989

3 occam *2 reference manual*, Prentice Hall 1988

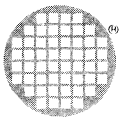
4 *Transputer technical notes*, Prentice Hall 1988 Transputer technical notes

5 *Notes on graphics support and performance improvements on the IMS T800*, Technical note 26, INMOS Limited

6 *A transputer based distributed graphics display*, Technical note 46, INMOS Limited

7 *Graphics databook*, INMOS Limited 1989

8 *Applications of a multi-port video RAM No. 6*, Hitachi Semiconductor



INMOS Limited
1000 Aztec West
Almondsbury
Bristol BS12 4SQ
UK
Telephone (0454) 616616
Telex 444723

INMOS Corporation
PO Box 16000
Colorado Springs
CO 80935
USA
Telephone (719) 630 4000
Telex (Easy Link) 62944936

INMOS GmbH
Danziger Strasse 2
8057 Eching
Munich
West Germany
Telephone (089) 319 10 28
Telex 522645

INMOS Japan K.K.
4th Floor No 1 Kowa Bldg
11—41 Akasaka 1-chome
Minato-ku
Tokyo 107
Japan
Telephone 03-505-2840
Telex J29507 TEI JPN
Fax 03-505 2844

INMOS SARL
Immeuble Monaco
7 rue Le Corbusier
SILIC 219
94518 Rungis Cedex
France
Telephone (1) 46.87.22.01
Telex 201222

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