·O·U·G·

occam® user group · newsletter

No 7 Summer 1987

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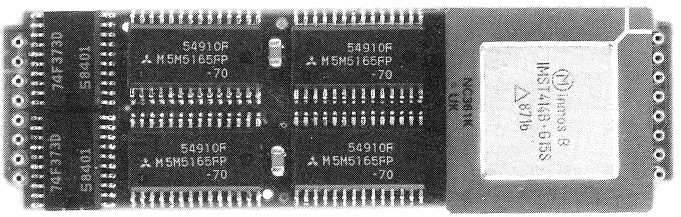

One of the forthcoming transputer modules from INMOS, the IMS B401, see p 12

NEWS

From the Editors

Once again, we have an issue of the Newsletter which reflects the growing activity within the occam community. However, we would welcome readers' views on the style and purpose of this document. For example, should it contain papers of substantial length (or should they be submitted in future to OUG Meetings, given that Proceedings of those meetings will be published from now on)? What should be the relationship between this newsletter and the Electronic Grapevine mentioned below?

Perhaps before the deadline for the next issue (early January 1988) members would like to express their views on these matters, either through the Grapevine or by post to us (address is at the back).

Short, newsy items for inclusion in the Newsletter are welcome, either through electronic mail (JANET: Paddon@uk.ac.aucc), or on PC floppy in unformatted ASCII or WORD format.

Derek Paddon, Mike Barton

Back Numbers

Copies of Issues 1, 2, 3, 4, 5 and 6 of the Occam User Group Newsletter are available while stocks last on application to the secretary at INMOS.

The bibliography started in issue 1, and the list of members in issue 2. Both have been supplemented in each issue.

Formation of a SIG for occam learning

Sandy Riach

As was announced at the last OUG meeting at Guildford we are setting up a SIG for the learning (and implicitly for the teaching) of parallel processing techniques using occam. We have used the word 'LEARNING' so as to cover the whole range of teaching and training.

Parallel processing, using occam, is a new and exciting area not only for the learners but also for those who will be instructing them. We have a great opportunity to contribute to the development of a teaching and training methodology for an area of computing that is new and challenging. Unlike other areas of computing there is little or no documented work on the common (or for that matter the uncommon) problems that people have when learning to use or program parallel systems (whether in occam or other languages like concurrent Pascal). As the group of people who are, perhaps, most involved in using occam we could ALL CONTRIBUTE to this SIG.

At the next meeting I am hoping to have a number of short talks from experienced teachers of occam discussing their techniques and from a novice to occam discussing the problems that caused most heartache. The intention is to create a basis for discussion on the aims and objectives of this SIG.

If you have any comments on the above, teaching/training materials for others to use or wish to talk at the SIG meeting on a specific subject please contact me at the address below:

Sandy Riach,
ITEC Consultancy Unit,
189 Freston Rd.,
London W10 6TH
U.K.
+44 1 969 4658 (or +44 1 969 7527)

Electronic Grapevines
Geraint Jones (University of Oxford)

If you are an electronic mail user, you may want to know about two electronic mailing lists, carrying discussions on occam and the transputer. These offer you a mechanism rapidly to distribute information, short papers, programs, problems, even gossip about INMOS, to the sort of people who may be interested. You may even want to read this sort of thing. We even have subscribers from INMOS who can be sometimes be goaded into authoritative declarations.

Each list has distribution points both in the UK and the USA. To join the occam mailing list try making contact with either:

occam-request@UK.AC.OXFORD.PRG (in the UK)

or

occam-request@SYR-SUTCASE.CSNET (in the USA)

For the transputer list contact:

transputer-request@TCGOULD.TN.CORNELL.EDU (in the USA)

or

transputer-request@UK.AC.OXFORD.PRG (in the UK)

In case of (extreme) difficulty, resort to

Geraint Jones
Programming Research Group
11 Keble Road
Oxford
OX1 3QD

7th technical meeting of the Occam User Group

This meeting will be held at the National Polytechnical Institute of Grenoble, France on 14th-16th September 1987.

All enquiries should be addressed to Mme Clotilde Chaland, US Systemes Integres, INPG, 46 Avenue Felix Viallet, 38000 Grenoble, France.

Telephone +33 76 87 60 68 or +33 76 47 98 55 Ext 619.

Travel arrangements from U.K.:
There are a number of charter and scheduled daily flights into Lyon and Geneva. Charter flights cost about £100, and scheduled flights about £130. This option would leave a journey of a further two hours or so, by train or coach, to Grenoble. Your usual travel agent will advise you or ring Conference Department, Spectrum Worldwide Travel on 0272 420789.

Spectrum Worldwide Travel have arranged a coach for those wishing to take the inexpensive route. "Club Occam" travel can be booked by using the form enclosed or ring the above Bristol number. Availability is on a "first come first served" basis so do not delay.

IFIP Conference on Distributed Processing

Amsterdam, 5-7 October 1987

Registration and programme details are available from SIC, Paulus Potterstraat 40, 1071 DB Amsterdam, The Netherlands. Telephone +31 20 620681; Telex 10761 Omega NL. Registration fee Dfl. 595 rising to Dfl. 695 after 1 September.

Bristol Transputer Centre

On 6 July, the Bristol Transputer Centre, located at Bristol Polytechnic, was formally opened by Iann Barron. The £0.5M Centre, which was set up with support from (inter alia) the Department of Trade and Industry, offers consultancy and training in the use of occam and transputers; it has a well-furnished laboratory containing a substantial number of development stations. For further details, phone Dr Jon Mortimer at Bristol Polytechnic: (0272) 656261.

MEETING REPORTS

Occam User Group Sixth Technical Meeting

Andrew Dixon (University of Bristol)

This meeting was held at the University of Surrey from Monday 13th to Wednesday 15th April 1987. It was organised by Roger Peel.

The number of SIGs had grown to include a hardware group and an introductory group for newcomers.

The speech at the conference dinner (on Monday evening) was given by Dr C J Elliott of Smith Associates.

ParSiFal: Hardware for mapping arbitrary occam networks onto Transputers

Peter J Jinks (University of Manchester)

This talk looked at the feasibility of mapping efficiently an arbitrary Occam program (with a network of channels) onto a Transputer Network, such that the hardware could be reconfigured for each application.

Four networking strategies were compared. A patchboard was dismissed as taking too long to reconfigure. A standard network with message passing would be fast to reconfigure, but would slow down all programs running on the network. A bus would be a possible solution, but it would limit expansion by its size. A switching network was therefore proposed as the best solution. This is constrained by hardware and software controlled.

Transputer networks of between 100 and 1000 transputers were considered. A full crossbar switch for all four links would require 4Nx4N switches. By always linking link 0 to link 2

and link 1 to link 3, the number of switches is reduced without loss of generality. It was then shown that if a Hamiltonian Cycle exists (almost always) then only 2xNxN switches are needed.

The T-rack using transputers and C004s was then described.

Flexible Interconnection of Processors using an Omega Switch
Dr Tony Fisher (University of York)

An alternative switching algorithm was then outlined. The major expense in a crossbar is the need for NxN switches, Bell Labs have conducted much research to reduce this. A Benes network is capable of any crossbar result with only 2NlogN-1 switches. This is more powerful than most people require, especially as one-to-many connections are not allowed in transputer networks. A cut-down version called the Omega Switch, consisting of perfect shuffles, costs NlogN and acheives virtually all one-to-one mappings.

An amusing look at stationary packet rings, implementing this design, was then recounted. A challenge was made to Inmos to match the 40 Gigabyte/sec link transfer rate.

The Design of Programs for Transputer Networks
Dr P Kilpatrick (Queen's University, Belfast)

A need for programming methodology for parallel programs was advocated in this talk. Efficient modifications rely on the ability to isolate processes. Programs should be sliced longitudinally rather than pipelined, when extra parallelism is sought. A compiler was taken as a case study, where the code generator was sliced to add parallelism, an efficiency of up to 150% was achieved.

Looking for Parallelism in Fortran
Derek Jones (Knowledge Software Ltd)

Many people are not prepared to rewrite their major investment in Fortran programs. The ability to recompile Fortran code to run on a network of computers is enticing. ParLoc analyses Fortran code to indicate where potential parallelism exists. The results indicate whether sufficient parallelism exists to warrant new hardware, and which areas of code are worth rewriting or reconfiguring.

Real-Time Control Using Transputers
Peter R Croll (Sheffield University)

External devices attached to computers often require servicing within a finite time of signalling a request. A Transputer time-slicing several processes may fail to respond in time. Even if the servicer receives a block of data from the external device, it must still be capable of passing that block (possibly buffered) on before the next service request. This talk looked at the use of the scheduler and high and low priority processes to try to overcome this potential problem. Hardware to implement a real-time controller was also described.

The Design of Fault-Tolerant Concurrent Processes using Occam
Dr David J Holding (Aston University)

If it is not possible to prevent a fault occurring (be it a software bug or a hardware fault), then tolerance is important in certain applications. This talk looked at the concepts and practicalities of error detection and recovery, damage assessment and fault repair.

With inter-process communication, the effect of an error in one process being passed onto others must also be considered. The standard sequential approach using backtracking after an error has been detected is complicated by the conversations which have been affected by the erroneous data.

PARFES - A Parallel Finite Element System
Dimitris Zois (Imperial College & University of Patras, Greece)

This speaker talked about the use of shared memory to implement his design for a parallel finite element system. A network interconnection box was used to link blocks of processor + memory to each other.

A detailed explanation of finite element theory was then mapped out, showing how MIMD was appropriate to this problem.

Configuration Tools for C004
John Nixon (Quintek Ltd)

Given an Occam program and a network of transputers linked by C004 switches, it is not always clear how one should be described on the other. This speaker talked about a descriptor language which enables the programmer to place nodes onto transputers and map channels onto links routing them through link switches where necessary. This descriptor language then converted it into instructions for the C004s and the transputer configurer.

TRANSIM - A Computer Simulator
Edmund R Hart (Polytechnic of Central London)

This simulator is capable of providing statistics on the performance of a transputer, or network of transputers, given an Occam program.

TRANSIM produces an overall run time, an average suspended time, the percentage of processor utilization and link traffic, and an event list for each processor. A distiction was made between a simulator which does not know which path to choose for conditional jumps, and an emulator which executes the code as if it were a transputer. Simulators can be used at a pre-coding stage (using shaved occam), a post-coding stage (to optimize, verify and debug) and even when coding is not intended (for research purposes).

Recent Advances in Polyprocessor Architectures
Dr P Milligan (Queen's University, Belfast)

This speaker suggested that no-one knows how to develop systems on polyprocessor architectures. He then looked at the different types of linking available. B004s have four free links, B003s are loosely coupled processors with some fixed and some free links. The Intel iPSC, however, has a rigid architecture. It was advocated that sequential programs should be converted automatically to run in parallel on these systems.

Latin is used to decompose Fortran, in order for it to be split between processes.

The Inmos T800 Architecture
Roger Shepherd (Inmos Ltd)

The floating point transputer can sustain 2.25 Mflops. Its design relied on the reuse of the T414 design and formal techniques for the FPU to minimize on development time and on

risk. A Behavioural Descriptor Language (occam) was used to determine its expectations and a Hardware Descriptor Language was used to describe the VLSI which implements that design. Mathematics was used to show that the BDL design and the HDL design were equivalent.

User Experiences with the T800
Charles Askew (Southampton University)

Southampton University was pleased to be able to boast that it had already received a much coveted T800. It had benchtested it against the T414, a VAX 11-750, a Micro-VAX II and a Ridge 3200.

	Monopoles	Lanizos	Laplace	3x3 matrix	Livermore
B004	1	1	1	1	1
T414b	2.5	2.3	2.3	2.6	2.1
T800a	15.5	12.1	12.5	35.1	23.2
VAX 11-750	6.6			6.0	
Micro VAX II				7.1	
Ridge 3200				35.1	

A maximum of 1.33 Mflops was obtained, which is a factor of 6 over the T414. The T800 is cheap per Mflop.

INMOS Product Update
Steven Brain (Inmos Ltd)

Inmos used this opportunity to plug its new products, especially the T800 (available July) and the Beta 2 version of Occam 2 (May 87).

Exploring Transputer Networks
Neil Miller (Inmos Ltd)

Roger the Worm was described as a simple way of exploring multiple transputer arrays. It can be used for checking and comparing networks, debugging and testing systems, and loading large unknown networks.

The SERC Transputer Initiative
Dr M R Jane (SERC)

The SERC has set up a transputer initiative to supply Higher Education Establishments with hardware, software and support on a pump-priming and short term loan basis. Enquiries should be sent to Dr Jane at Rutherford Labs.

Implementing Forth on the Transputer
Leon Heller (Concurrent Technology)

This speaker attempted to sell a product which has not yet been produced. He failed to give any details of how the language would be implemented on the Transputer.

The Pursuit of Deadlock Freedom
Naiem Dathi

The use of CSP and formal techniques may be used to investigate interactions between pairs of processes to reduce the likelihood of deadlock.

An Image Processing System with Optimising Performance
Dr David W Downing & Ian B Bennett (Gwent College of Higher Education)

This talk looked at methodologies for vision systems. A tree structure was advocated. A convolution image transformation was based on a 3 x 3 pixel multiplication to obtain a new central pixel. The system proved very effective at identifying coffee mugs.

Guildford meeting of the Transputer Hardware SIG
Tony Gore (Inmos Ltd)

The first meeting of the Transputer Hardware special interest group belonging to the Occam User Group was held as part of the sixth OUG meeting at the University of Surrey, Guildford on the 13th. April 1987.

The chairman opened by briefly laying out some ideas for objectives and organisation for the SIG before there were a number of presentations on relevant subjects to give the attendees food for thought.

Techniques for debugging transputers and transputer systems from the hardware point of view were covered by the SIG chairman as a means of introducing a relevant topic to this group. This information was given out at the time; the software mentioned has been placed into the OUG library.

An example of interfacing with a link adapter was given and demonstrated by the chairman and then Tim Normanton of Smiths Industries detailed his experiences of interfacing an FPS array processor to a B002 via a link adapter. John Nixon of Quintek briefly outlined his computer assisted transputer board design programme.

Discussion was then opened on the subject of objectives and organisation for the SIG. The **objectives of the SIG** were perceived as follows:-

Hardware Interfaces
(Various offers were made of this information - RSRE have a mouse to link adapter interface they are willing to detail)

Tools and Techniques
Device Drivers (although this may interface with operating systems)

Set hardware standards
Act as a pressure group for future hardware developments

Produce a list of companies and hardware products

Produce a list of bugs

The first two items were put to a show of hands for the level of support - greater than 90 percent.

SIG organisation was much harder to define; however it can be summarised thus:-

Meet with the OUG every six months.

Have a bulletin board / mailing list on something such as JANET.

Put together some information regarding geographic distribution of members.

Aim to do a trial run of a local SIG meeting before the next OUG to see how it goes. The area likely for this is probably to be centred on Sheffield, with Peter Croll as one of the organisers.

There was one later suggestion that the SIG might put together a collection of hardware notes, perhaps in book-form for sale - a sort of transputer cookbook.

Guildford meeting of the Formal Techniques SIG

Bob Gustafson (609 W Stratford Pl.,Chicago, IL 60657, USA)

The meeting was convened by Bob Stallard (D.M. England and Partners Ltd, Lytham Court, Woodley, Berks, RG5 3PQ)

There was a long discussion on the usefulness of Formal Techniques (FT). It was mentioned that FT were used extensively in the design of the T800. The motivation was to bring the floating point Transputer to market quickly and cheaply. The alternative - hack up a design and test - was not feasible because even with abbreviated test vectors, the testing time would stretch on into the next century. The design team for the T800 consisted of 8 people including a mathematician (Boolean proofs). Total calendar time was less than 1 year. The FP spec was the trick. The IEEE standards were faulted for using English. It was agreed <even though the conference was in England> that English is not a good language to describe or express specs if one expects a number of different companies to implement the spec.

There were 30 to 50 points of unclearness. These had been communicated to Kahan's standards group at Berkeley.

There is an Oxford monograph available from INMOS describing the work on the Floating Point Specification.

A Higher Order Language/Formal Techniques methodology was used to design some sort of ECL lashup at Cambridge. Subsequent deadlock of the system was traced to specifications which were faithfully reproduced by FT in hardware. Other languages (?) mentioned besides occam were ML, Estelle, Pangloss...

Other successes of FT were mentioned - they were used to keep track of OSI communication protocols within ICL.

Oxford PRG is considering doing a short course on Formal Techniques. Timing might be synchronized with the Sept OUG meeting in Grenoble (either before or after). Contact

Michael Goldsmith for more information, (Michael @ SEVAX.PRG.OXFORD.AC.UK). Send suggestions / <proposed syllabus>. The sooner suggestions arrive, the higher the probability they will be taken into account.

Guildford meeting of the Operating Sytems SIG
Bob Gustafson (609 W Stratford Pl.,Chicago, IL 60657, USA)

Operating systems mentioned in conjunction with occam/Transputers were PC-DOS, MS-DOS, TDS-Stride, TDS-(VAX-(VMS,Unix),Sun Unix), Megatool (ParSyTec), MDS (Meiko).

INMOS developments - file stores were seen to be moving from nameless system to named stores (?), Beta2 occam2 TDS ('Product' release in 2 months) includes fully enhanced protocol checking, a library with a large collection of T8 application programs (sines, cosines, FFT, etc), examples of how to use & get access to DOS filing system. Usage checker, inline assembly code were mentioned (but the exact context is hard to determine from my notes!) Lattice Logic has Pascal Compiler (?).

Panel session at Guildford OUG meeting
Bob Gustafson (609 W Stratford Pl.,Chicago, IL 60657, USA)

The members of the panel were: (from left to right):

Judy Bishop - c/o Dept of Physics, Univ of Southampton, Hants S09 5NH

Duane Call - CSA, 950 University Ave, Provo, Utah 84604 USA

David May - INMOS Ltd, 1000 Aztec West, Almondsbury, BRISTOL, BS12 4SQ

Gordon Harp - RSRE, St. Andrews Road, Great Malvern, Worcs, WR14 3PS

Peter Welch - Computing Lab, University of Kent, Canterbury, Kent CT2 7NF **(Chairman)**

Allan Burns - Computer Science, Univ of Bradford, West Yorkshire, BD7 1DP

Allan Burns responded to the first question: 'What is major need of occam community?' by saying "lack of good books" (he has a book coming out in Sept). Answers from others to same question: Unbundling of occam, library compilation, sympathetic C or FORTRAN, Transputer Workstations.

The discussion drifted to ADA, with Judy Bishop answering most of the questions. It was mentioned that UK defense has chosen ADA (this statement was later hedged). The ADA model of concurrency leans toward closely coupled, shared memory systems. There are fundamental problems in adapting ADA to loosely coupled machines. Sequential implementation seems ok. One glowing hope of ADA is the Programming Environment. Until PEs are implemented, ADA will be just another compiler. ADA may have to change in 1989 to address some of these issues. 25% of use is commercial rather than defense in U.S.

Need to use Transputers for monitoring. Meiko supervisor bus is a valid approach - too bad it was implemented as a bus.

Problems getting in and out of Tedius (ah - TDS).

Occam needs to be taught by example. People need to be happy with the language. A person who has been maintaining a 500,000 line FORTRAN program is considered permanently brain damaged and unsuitable for reprogramming to occam. Many programmers have been ground into a sequential rut. Hardware engineers with no previous programming experience

do better at occam than Software types. Experience with parallel, concurrent happenings seems to make a difference. Occam is useful for teaching logic design.

David mentioned that the original T414 design was limited by available silicon area, but subsequent designs have faced a "sea of silicon". The floating point T800 is one use of that area. INMOS is continually looking for market direction, but the constraint is to come up with a balanced chip design that will have a long production run. David suggested that 16 T on one chip would be a possibility.

One question from the floor asked WHEN this chip, with an integral C004, would be available. No comment.

Provision of Output Guards was discussed as something that David May should incorporate into occam. He responded by saying (paraphrased) that the best way to implement output guards would result in a slowing of link throughput and increase in complication of link hardware for ALL communication. Experience has shown that in all cases (so far), output guards can be avoided by clever occam software.

Second International Conference on Supercomputing
Derek Paddon (University of Bristol)

This conference was held at the Santa Clara Convention Centre, California, USA during the period 3 to 8 May, 1987.

The conference was very well supported by industry, governments and academia, with delegates drawn from the ranks of: USA senators, government officials from Europe, Japan and the USA; industrial and government research laboratories; and of course, universities from most continents.

The industrial show, associated with the conference, namely the "first world supercomputer exhibition" lived up to its title. Most major supercomputer manufacturers exhibited, often with lavish presentations of their latest equipment. Notable exceptions were the absence of CRAY and the new DAP company Active Memory Technology (who were represented by a management team).

Most of the exhibitors were reasonably well informed on the principles of parallel computation, but obviously partisan. Even so, a degree of naivity was present. This naivity was often displayed by representatives of companies marketing vecterising supercomputers. Some still believe "you never need to look at your algorithm" as their latest whiz bang compiler will "spot the parallelism".

Representatives of Thinking Machines had heard of the DAP (at last) and thought there may be a relevant literature (mostly based in the UK) which was worth looking at, and they would soon. This more enlightened view indicates that parallel computation is perhaps coming of age, with a true international community.

The transputer was featured on three stands at the exhibition: Inmos, CSA and Floating Point Systems. FPS had an abundance of literature available on the T-series and created some interest. The personnel on the Inmos stand vigorously advanced the cause of the transputer. Pete Wilson, Martin Booth and their support staff explained the principles to numerous interested but often unbelieving Americans. This disbelief turned to dumbfounded astonishment when they visited the neighbouring stand of CSA, where the ever smiling Duane Call demonstrated the only live IMS T800 in the USA. CSA's banner "The World's only supercomputer kit" brought a continuous stream of delegates to view the power of the T800 ray tracing demonstration.

Among the five day programme, in five parallel sessions, lurked a small number of papers on occam and/or the transputer. Jeffrey Fox from the CALTECH hypercube project made frequent mention of transputer systems, but the main contributions were papers given by Gordon Harp, who gave an excellent paper on the supernode project, and Anirlan Basu who also gave an excellent paper on an adaptable pipeline.

A large number of papers described MIMD systems, sometimes based on totally unsuitable processor architectures. This again showed the opportunity we have to exploit the transputer in a multitude of system architectures, where its versitility gives an enormous advantage as a research tool.

The papers describing parallel computation were the most varied in quality that I have heard at a conference. In particular, papers describing scientific computation were often of a quality that should have been difficult to have had accepted even ten years ago. Many contributors seemed to have recently 'discovered' parallel computation and as a result were 'doing their thing' without much knowledge of the vast literature in this field. Perhaps there are lessons here for the occam users group. We must not fall into the trap of repeating old work with a new language and computer architecture and pretend it is research, when in reality it may only be evaluation.

NEW PRODUCTS AND SERVICES

Product news from INMOS

David McCusker (Inmos Ltd)

The INMOS transputer family continues to expand with new parts, packages and board products. Many new transputer products are coming on to the market, and transputer production facilities have been ramped up to cope with the demand.

The IMS T800 will be shipped in quantity by the end of the third quarter and already the backlog is sufficient that it will take several months to satisfy the initial demand. The 30 MHz speed option will be available in the first quarter of 1988 with military (883C) qualified parts available at the end of that year.

IMS T414s will also be available to military 883C qualification at the end of 1987 and plastic leaded chip carrier packaged parts will also be available in the same timeframe. The 16 bit T212 will also be produced to military specification in the fourth quarter of 1987.

The board family is being expanded to include a range of motherboards and modules. The motherboards will be designed to accept many different standard transputer modules, and INMOS will produce different modules to build up the system that matches the customer's needs.

The motherboards will be available for various host environments, but the first two that will be produced will be for the IBM PC XT or AT (the IMS B008) and the INMOS ITEM rack in double extended eurocard format (the IMS B012). In the future motherboards are planned for the new IBM PC's and the Sun workstations (VME format).

INMOS will be producing a range of modules which will fit on to the motherboards. All the modules will fit on to any of the motherboards. The first three modules released will be the following :

IMS B401-1 &IMS T414B-G15S plus 32 K Bytes of SRAM.

IMS B402-1 &IMS T212A-G20S plus 8 K Bytes of SRAM.

IMS B403-1 &IMS T414B-G15S plus 1 M Byte of DRAM.

In the future the modules available from INMOS will have 2, 8 and 16 M Bytes of memory as well as modules with IMS M212's, RS232 and Ethernet links, and graphics facilities.

Both modular and fixed boards will be supported long term by INMOS.

Occam 2 transputer development systems are being released in Beta format and all customers will be upgraded to full occam 2 product when it is available. Compilers for C, Fortran and Pascal are also available in pre-production releases and product should be available in the third quarter of 1987.

Full details and pricing can be obtained from INMOS' distributors. In the UK these are:

Access Electronics Components Ltd. Tel No. 0462 682333

Hawke Electronics Ltd. 01 979 7799

Rapid Recall Ltd. 0494 26271

Outside the UK:

Austria.	Othmar Lackner (43) 0222 75 26 18
Belgium.	Diode Belgium (02) 216 21 00
Denmark.	Peter Petersen A/S (45) 6 83 62 11
Finland.	Field Oy (0) 692 25 77
France.	Tekelec (1)534 75 35
France.	Scaib (1) 687 23 13
Ireland.	Micro Marketing Ltd. (0001)856288
Israel.	R.D.T. (03) 49 21 90
Italy.	Celdis (02)612 00 41
Netherlands.	Techmation (041) 89 22 22
Norway.	O.T.E. (02)26 99 55
Portugal.	Teleprinta
Spain.	Diode Espana (01)455 36 86
Sweden.	AB Gosta Backstrom (08) 53 12 51
Switzerland.	Datacomp (01) 730 21 65
West Germany.	Astek (04106) 710 84/86
West Germany.	E2000 (089) 42 0010

Product news from Transtech

Transtech has continued to increase its range of transputer based systems. The imminent arrival of the IMS T800 floating point transputer is catered for as an optional upgrade for most of the Transtech systems. Details on educational discounts are available from Transtech.

TSB04-2 PC add-on:

This is an add-on board for the IBM PC, XT or AT (or compatibles) and provides a 32-bit transputer with 2 Mbytes of DRAM as an introductory system. It may be used as a single transputer evaluation system or as a host to a transputer network. It is available in two versions:

2 Mbytes of DRAM + T414-20 at £1440 ~~$627.84~~

4 Mbytes of DRAM + T414-20 at £1950 ~~$850~~

TSB44-4 four transputer board

This add-on board for the IBM PC, XT or AT (or compatibles) provides four 32-bit transputers, each with 1 Mbyte of DRAM. The system can be upgraded for T800 floating point transputers.

The basic system is priced as follows: ~~$1918.40~~

4 X T414-20 + 4 X 1 Mbyte of DRAM at £4400.

The full specification and upgrade cost is available from Transtech.

Transputer Development kit

A kit comprising an IBM AT, an add-on board (T414-20 + 2 Mbytes of DRAM) and OCCAM 2 software is available at £4395. ~~$1916~~

TSB174-4 PC add on fully configurable network

This is the most exciting prospect to date in cost effective systems for the parallel processing engineer or scientist, offering 25 Mflop power for less than £20000. This system is supplied with 17 transputers and 4 Mbytes of DRAM. The 16 slave transputers are configured by program via the 2 Inmos C004 link crossbar switches, eliminating the need for connecting links by hand, thus increasing the flexibility of a system that needs to be frequently configured.

The present version of the system uses the T414-20 transputer, upgradable to the T800 floating point transputer.

The system is supplied with the Inmos TDS for Occam programing; C Pascal and FORTRAN compilers are available as optional extras. Price £14750.

~~$6431~~

Transputer modules
Transputer modules are available as follows:

Double Eurocard mother board (with sites for 16 transputer modules) TSMB-16 at £750

Module TSM 42-25 with T414-20 and 256 Kbyte of DRAM at £645

Module TSM 42-1 with T414-20 and 1 Mbyte of DRAM at £895

Module TSM 42-4 with T414-20 and 4 Mbyte of DRAM at £1945

IMS T800 module system prices are to be announced.

TSMB-16 reconfigurable module network
This system combines the flexibility of the transputer modules with the reconfigurable system previously described. The TSMB-16 consists of a double Eurocard mother board with 16 transputer module sites, two sockets for the IMS C004 crossbar switch and two RS232 ports. The board can be populated with the transputer modules described above.

The system can be initiated with just one module and added to as pocket or need requires. Multiple mother boards can be rack mounted to give very powerful systems while retaining the reconfigurability allowed by the C004 cross bar switches.

Cost and full specifications are available from:

Transtech Devices Ltd, Unit 3, St. John's Estate, Penn, Bucks HP10 8HR. tel: (0494 81)6681

Product news from Concurrent Techniques

TM2 1 Mbyte transputer module
Concurrent Techniques (formerly Concurrent Technology) now has available a 1 Mbyte transputer module. It's the same size as the earlier 256K TM1 module (75mm by 95mm), and sells for £650 with a T414-15 and 120 ns RAMs. The TM1 costs £450.

XLISP on the transputer
Leon Heller writes: "I recently purchased the Inmos/Lattice Logic C compiler, and tested it by compiling the source code for David Betz's public domain XLISP object-oriented LISP interpreter. Apart from a couple of statements, the whole thing compiled without any problems, and runs quite happily on my 256K and 1 Mbyte modules. If anyone wants a copy, it's available free, if they send me a formatted 5 1/4" DOS disk."

Further details are available from:

Leon Heller, Concurrent Techniques, 30 Baldslow Road, Hastings, East Sussex, TN34 2EY. tel: (0424) 714790.

Occam2 and the Meiko Computing Surface
University of Edinburgh
Department of Physics

A series of courses is being planned, the first of which will be held in Edinburgh from 2nd to 4th September 1987.

This course offers an introduction to the occam2 programming language, to techniques for exploiting concurrent computers and to the MEIKO computing surface, in particular.

There is a substantial component of practical work using transputer-based workstations, VAX-based occam2 environment and the Concurrent Supercomputer built by MEIKO. This last system currently comprises a processor farm for code development, and an electronically reconfigurable 40-transputer array and four high-performance graphics systems.

The full course is limited to 16 participants and the fee for the course is £300 + VAT exclusive of accommodation costs. Staff and students of other universities may attend lectures and receive course material for a reduced fee of £50 + VAT but will not have access to the Computing Surface during the course.

For further information contact:

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ARTICLES

Interfacing a Link Adapter to a Z80 PIO

A E Lawrence (MicroProcessor Unit, Oxford University)

A number of people in the hardware SIG at the recnet OUG meeting at the University of Surrey expressed interest in the circuit.

It interfaces a C003 link adapter to an elderly Z80 system. The link is buffered onto 93 ohm coaxial cable. We have run the link over a complete reel of at least 100 metres, and have not recorded a single error.

The interface does not include any provision to prevent ground loops. The connection may be interrupt driven, or polled. It uses an existing Z80A PIO chip clocked at 4MHz. The link itself would have been buffered with a 74F3037 (Signetics and possibly others), had that chip been available at the time. Instead two F420 gates were employed. In order to control skew, terminating the driving F420 with 93 ohms was considered. This does not seem to be necessary in practice.

The circuit is straightforward. the C003 is much faster than the PIO, so few latches are required. Copies of the circuit can be obtained from the editors.

Sorting in Occam

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Sorting can be defined as the process of rearranging a sequence of values in ascending or descending order. Because of both their practical importance and theoretical interest sorting algorithms have been studied extensively.

We demonstrate, how sorting algorithms can be implemented in Occam on a transputer architecture. Both parallelized algorithms and pure parallel algorithms are considered in a full version of this article.

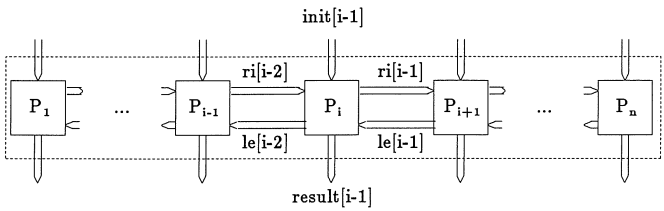
As basis for our discussion here we show a parallel version of the serial odd-even transposition sort algorithm. The serial odd-even transposition sort algorithm *[Knuth 73]* sorts n values $(x_1,x_2,...,x_n)$ in n phases, alternatively an odd and an even phase. During an odd phase, odd elements must be compared with their right adjacent neighbours, during an even phase, even elements are to compare with their right adjacent neighbours.
The following example demonstrates this sorting process:

	x_1	x_2	x_3	x_4	x_5	x_6
	5	4	1	3	6	2
odd phase	4	5	1	3	2	6
even phase	4	1	5	2	3	6
odd phase	1	4	2	5	3	6
even phase	1	2	4	3	5	6
odd phase	1	2	3	4	5	6

In general, n phases are nessecary to sort n values, each phase requires n/2 comparisons, that is sorting can be done in $O(n^2)$.

A parallel version of this algorithm is introduced in *[BauSte 78]*. Let us suppose we have n lineary connectet processors $P_1,P_2,...P_n$ and initially x_i resides in P_i. To sort the sequence $(x_1,x_2,...,x_n)$ in parallel, during an odd phase $P_1,P_3,P_5,...$ must be active, $P_2,P_4,P_6,...$ are active during an even phase. All prosessors work in parallel. Thus the parallel odd-even transposition sort algorithms sorts n values with n processors in n comparisions and 2n transfers, that is sorting can be done in $O(n)$ and it is easy to prove that this is optimal for the architecture shown below.

Now we are prepared to specify the parallel version in Occam. The architecture of the resulting sort-machine illustrates the following picture:



We assume that the sequence $(x_1,x_2,...,x_n)$ to be sorted is available at channels init[0],init[1],...,init[n-1]. The sorted sequence may be outputed at channels result[0],result[1],...result[n-1]. To describe the sorting process, we consider one process P_i. Let us suppose P_i is in an odd phase. The activities P_i has to execute depend on i:

If i is odd, then P_i performs the following actions (active role):

a) consulting P_{i+1}

b) comparising x_i and x_{i+1}

c) outputing the maximum of x_i and x_{i+1} to P_{i+1}

d) setting x_i to the minimum of x_i and x_{i+1}

If i is even, then P_i is passive:

e) outputing x_i to P_{i-1}

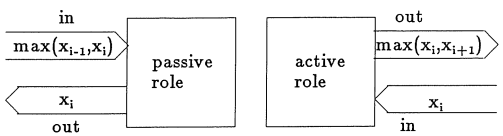
f) inputing the maximum of x_i and x_{i-1} from P_{i-1}

If P_i is in an even phase active role and passive role are to be defined analogically (i is odd implies pasive role, i is even implies active role).

Now we can specify active and passive role in Occam:

```
PROC active.role(CHAN in,out,VAR xi,xiplus1)=
  SEQ
    in ? xiplus1 -- a)
    IF -- b)
      xi < xiplus1
        out ! xiplus1 -- c)
      TRUE
        SEQ
          out ! x1 -- c)
          xi := xiplus1: -- d)


PROC passive.role(CHAN in,out,VAR xi)=
  SEQ
    out ! xi -- e)
    in ? xi: -- f)
```

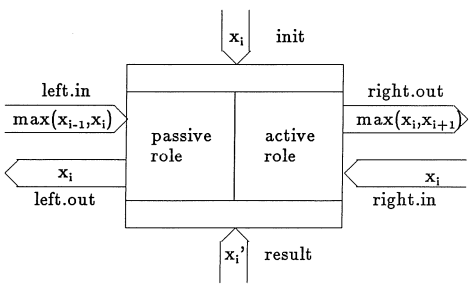


The processor P_i executes the following sequence of actions, depending on i:

i is odd		i is even
active.role		passive.role
passive.role		active.role
:	n/2 times	:
active.role		passive.role
passive.role		active.role

Thus, we can formulate P_i as Occam process:

```
PROC P(CHAN right.in,right.out,left.in,left.out,init,result,VALUE i,n)=
  PROC active.role ...
  PROC passive.role ...
  VAR xi,xiplus1:
  SEQ
    init ? xi -- inputing xi
    IF
      i\2 = 1 -- P is odd process
        SEQ j=[1 FOR n/2]
          SEQ
            active.role(right.in,right.out,xi,xiplus1)
            IF
              i<>1
                passive.rolle(left.in,left.out,xi)
      TRUE -- P is even process
        SEQ j=[1 FOR n/2]
          SEQ
            passive.role(left.in,left.out,xi)
            IF
              i<>n
                active.role(right.in,right.out,xi,xiplus1)
    result ! xi : -- outputing result
```



To complete the Occam programm, we state that n P-processes can work in parallel, thus we obtain the following Occam code.

```
DEF n=8: -- n must be an even number
CHAN ri[n-1],le[n-1],init[n-1],result[n-1],dummy1,dummy2:
PROC P ...
PAR
  P(le[0],ri[0],dummy1,dummy2,init[0],result[0],1,n)
  -- call P1
  PAR i=[2 FOR n-1]
    P(le[i-1],ri[i-1],ri[i-2],le[i-2],init[i-1],result[i-1],i,n)
    -- call Pi 1¡i¡n
  P(dummy1,dummy2,ri[n-1],le[n-1],init[i-1],result[i-1],n,n)
  -- call Pn
```

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