·O·U·G·

occam™ user group · newsletter

No 6 February 1987

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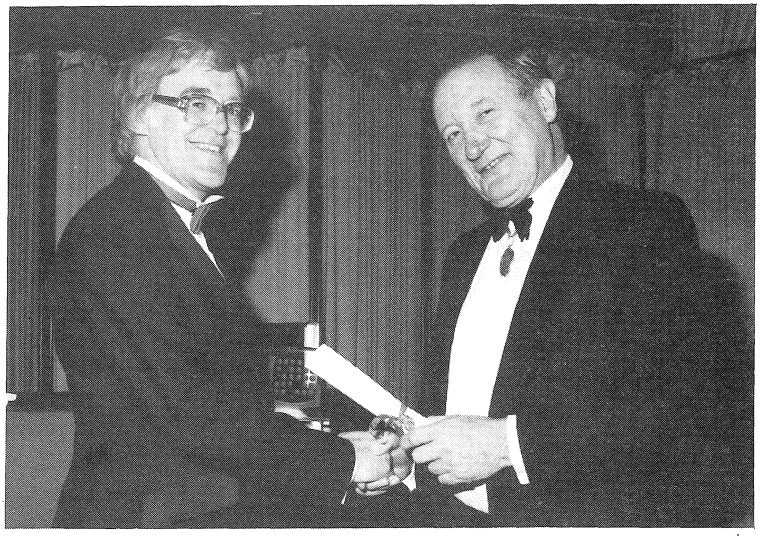

Iann Barron receiving a BCS award (technicl category) for the transputer from Sir Francis Tombs, Chairman of the Engineering Council.

OUG NEWS

From the editors

This sixth newsletter contains news that we are sure the members will find interesting, but is thin on articles. We appeal to members to submit articles, particularly material related to occam experience based on multi-transputer systems.

To ease secretarial duties, unformatted text on 5.25 inch floppy disc or electronic mail will be appreciated.
(JANET: Paddon @ uk.ac.aucc)

Derek Paddon, Mike Barton.

From the chair

The OUG is now into its 4th year and has grown from the 20 founder members in 1984 to over 1000 in the first 3 years. Such a rapid growth raises the question of whether the present organisation is meeting the members' requirements and, in particular, if the present committee structure is adequate.

The committee currently consists of chairman, secretary, librarian and news letter editor, plus 7 ordinary members. The practice up to now has been to co-opt an additional member to organise each technical meeting with the result that the committee has now grown to 11 members and could continue to grow to an unmanageable number. The committee are also aware that none of the members are elected and we are all here by default as it were. We hope that we have the right balance between academia and industry and that we reflect the members' views and represent them adequately but we would like confirmation. We therefore plan to seek the views of members at the next technical meeting to be held at Guildford on 13, 14 and 15 April. We shall ask the members to decide if they wish the organisation to be on a more formal basis with an elected committee. If the vote is for an elected committee then we have several further options:

1. To decide the composition of the committee. Note that we rely on financial and secretarial support from Inmos and currently Inmos nominate the secretary.

2. Should the new officers be appointed by the committee or should they be elected?

3. How often should elections be held and where?

The present committee are all happy to continue but if changes are decided on then our recommendations are for a committee of 7 members consisting of one member nominated by Inmos, the other six to be elected annually and with the officers being appointed by the committee. I urge all members to consider these issues and be prepared to vote at the next technical meeting.

At the Loughborough meeting there were several controversial issues raised:

1. There was concern over support for large projects being developed in occam, with many programmers and software modules to be coordinated.

2. There is a general requirement to access data which is stored on host machines but not written into occam folds.

3. There were queries over the stability of occam2 and concern about how much and how quickly it will change in the future.

Peter Cavill, Inmos Director of Microcomputer products has responded with the following comments:

"1. We share your concern over the problems of support for large projects. Inmos do not have the resources to develop this level of software themselves but would be willing to cooperate with vendors of IPSE's who wish to include support for transputer-based targets."

"2. Access to host data files is an essential part of alien language support and will also be made available to occam programs when alien languages are included in the development system."

"3. When we release an occam 2 product we shall support a well-defined version of the occam language. We reserve the right to extend the language further at a later date. Such an extension would create a new language, probably called occam 3, but we would undertake to provide a means whereby occam2 programs would continue to be valid."

Plans for 1987 are now in an advanced state; details of the 6th Technical meeting to be held in Guildford are on page 4, with the 7th meeting being planned for Grenoble, France, in September 1987.

Finally, Martin Bolton, who has so successfully edited the news letter over the last 3 years is moving into new research activities and is relinquishing the post of editor. I'm sure all members will join me in wishing him every success for the future. Derek Paddon and Mike Barton of Bristol University have agreed to jointly edit future issues. We make the usual plea for news items, contributions, etc.

Gordon Harp

Back numbers

Copies of Issues 1, 2, 3, 4 and 5 of the Occam User Group Newsletter are available while stocks last on application to the secretary at INMOS.

The bibliography started in issue 1, and the list of members in issue 2. Both have been supplemented in each issue.

Formation of a Special Interest Group for Hardware

Tony Gore, INMOS

Following comments made at the recent Occam Users Group meeting, there now seems to be a need for a special interest group concentrating on "hardware", where "hardware" is defined as the systems that occam is run on. It is expected that this will be mainly, but not exclusively, transputers. The plan is for this group to be a forum for the exchange and dissemination of ideas, as there has been no co-ordination of this in the past.

All comments and articles will be most welcome, to myself, Tony Gore, at:
Inmos (1000 Aztec West, Almondsbury, Bristol, BS12 4SQ, England). Articles will normally be published in the OUG newsletter.

I believe that some people who are active in the area of hardware may wish to get together more locally on occasions (this need has been expressed by those outside the UK in particular), and the group can help in co-ordinating this. So, send in the articles, however big or small!

Hardware Special Interest Group

Tony Gore, INMOS

To start the ball rolling in this new special interest group, I have gathered together some of the common errors that are made when building transputer systems from scratch.

There have been a number of simple things that can cause problems with self build transputer systems; the usual manifestation is that the system fails to boot properly. The following points should be borne in mind:-

1) The loop time constant capacitor for the transputer is 1.0 microfarad for the revision B silicon; a non-polarised ceramic is preferred, particularly if upgrading, as the CapPlus and CapMinus pins were interchanged between revisions A and B. If the original value of 10.0 microfarad is used, then there may be too much jitter on the links for correct communication.

2) All unused links should have their inputs taken to ground through a 10k resistor. On booting from link, the transputer monitors all links and replies to the one that it sees activity on; floating links will waggle up and down, confusing it, so that it may reply to the wrong link and thus fail to boot.

3) The PCB tracks to the PLL decoupling capacitor should be wide and short to minimise inductance, capacitance and resistance. The length of these should not exceed 25mm, and they should avoid other signals that can cross-couple noise, etc. onto them. These two connections are the most important after good power supply connections.

4) The "worm" program supplied with occam 1 is greater than the 2k of internal memory, and so will not find processors that do not have working or connected external memory. For occam 2, there is a "skinny worm" that will work in internal memory only, and this can be used to check that the connectivity and functionality of transputers connected to a B004.

Sixth Technical Meeting

The Sixth Technical Meeting of the Occam User Group will be held at the University of Surrey, Guildford, on Monday 13th to Wednesday 15th April, 1987.

Registration and Special Interest Group sessions will be held on Monday morning, followed by lectures and a panel discussion on Monday afternoon, Tuesday and Wednesday. The conference dinner is planned for Monday evening.

Accommodation is available for all delegates on the Monday and Tuesday evenings, with a lesser number of places also planned on the evening of Sunday 12th April for those travelling long distances.

Registration details are enclosed with this newsleter.

Requests for further details or to fill exhibition space may be discussed with:

Roger M.A. Peel,
Department of Electronic and Electrical Engineering,
University of Surrey,
Guildford,
Surrey GU2 5XH.

Phone: (0483) 571281 ext 2278
JANET: roger @ uk.ac.surrey.syse
UUCP: ...mcvax!ukc!reading!uoseev!roger

Advance notice of Technical Meeting No 7.

The seventh technical meeting of the occam user group will be held at the University of Grenoble, France from 14th to 16th September 1987. This will be our first venture out of England and members are invited to help make this a success.

Members on the continent of Europe are particularly invited to offer to speak or demonstrate at this meeting which will be conducted in English. British contributors will also be welcome.

Please make your offers either to Dr Triain Muntean,
IMAG, Lab de Genie Informatique, BP 68,
38402 St Martin d'Heres,
Grenoble, FRANCE (Tel 76 514600 x5217)
or to Gordon Harp, (OUG Chairman) at RSRE, St Andrews Road,
Great Malvern, Worcs, WR14 3PS, UK.
(Tel 06845 2733 x2824)

MEETING REPORTS

Fifth Technical meeting of the occam user group
Nigel Kingswood, University of Bristol.

The last technical meeting of the user group took place at Loughborough University of Technology and was spread over two and a half days from the evening of Sunday 21st September to the afternoon of Tuesday 23rd September. Following the trends of previous meetings the number of people attending increased and the there was a significant number of people from overseas including some of the speakers.

The main part of the meeting was spread over 4 sessions on the Monday and Tuesday. The whole of the Sunday evening was reserved for the special interest group meetings. As well as presentations, there were also several companies demonstrating their products.

The conference started with the meetings of the special interest groups. To allow people to attend more than one group meeting they were organised as three sessions each of which had two meetings going on in parallel. The six special interest groups were: Formal Techniques, Networks, Artificial Intelligence, Operating Systems, UNIX, and Graphics. Some of these groups were still developing and had not decided on their final form.

The first session on Monday morning was chaired by Chris Jesshope from Southampton University.

-- The Opening address by Dan Simpson of the Alvey Directorate covered the work done by the Directorate to foster IT and software engineering. He speculated on what might happen after the Alvey program had finished and how occam was being used in some Alvey projects.

-- Michael Poole of Inmos then outlined the features of occam 2, the new version of occam. After noting the differences between occam 2 and proto occam, he described a tool to ease the translation from proto occam to occam 2.

-- John Oldfield expounded the work of his group at Syracuse University, New York. They were working on the the use of content addressable memories to accelerate logic programming systems. He outlined the use of such content addressable memories in a co-processor to support PROLOG running on a transputer based host.

-- Alan Culloch from Lattice Logic described his work to allow the use of alien languages on the transputer. This would allow conventional language segments such as C, Fortran and Pascal to be bound together in an occam 'harness' which would describe any parallelism.

The second session on Monday afternoon was chaired by John Oldfield of Syracuse University, New York.

-- Chris Jesshope described his work at Southampton University to construct an adaptable array processor known as the RPA. He outlined it use as an intelligent memory system for the transputer and put forward some performance figures for the system.

-- Ron Schiffman of CSA Corporation (USA) has worked on the FPS T series computers and he outlined the ways he had change his approach to writing device drivers, queue managers etc., in using occam as a system programming language. He also gave his impressions on using occam for these tasks.

-- Chris Followell of Inmos gave an overview of Inmos transputer product available now or in the near future. These included evaluation boards containing one or more transputers. He also described the floating point transputer and evaluation boards for the disk transputer and the A100 signal processing chip. -- Bob Moore from Advanced System Architectures proposed the use of Auto-G as a tool for the overall design of transputer systems. This product uses graphics to outline the functioning of a system.

-- Donna Bergmark gave a presentation on the work done at Cornell University, USA, to convert a high level language such as concurrent Pascal into occam.

-- The session was rounded off with a panel discussion.

The conference dinner was held on Monday evening. The speaker at this dinner was D.J. Evans from Loughborough University.

The third session on Tuesday morning was chaired by Peter Welch from Kent University.

-- The session began with a talk from Andy Bakkers from Twente University, Netherlands on the the work he had done in using occam to write an control algorithm for a robot.

-- Colin Stirling from Edinburgh University described some of the problems in extending Hoare logic to include terminating concurrent programs; in particular a generalised channel CSP.

-- John Brierley from Sension Limited talked about some of the products available from his company. These included evaluation systems, high speed data acquisition and graphics subsystems.

-- Duncan Roweth described the work being done at Edinburgh University, in particular the computational physics group using a Meiko computing surface.

-- The session was concluded by the occam user group business. This was mainly concerned with the format of future meetings. Suggestions were made as to the length of future meetings and the possibility of parallel sessions to allow more presentations. The timing of the special interest groups in the meeting was also debated.

The final session on Tuesday afternoon was chaired by Gordon Harp of RSRE.

-- Julian Wilson from Inmos started the session with a description of how errors in the execution of occam programs on arrays of transputers could be analysed using features of the Inmos evaluation boards.

-- Graham Megson of Loughborough University outlined his work in using occam for simulating systolic arrays. An occam program described a virtual machine which allowed different systolic architectures to be studied.

-- M.A. Stinchcombe of British Aerospace described the use of electromagnetic environment simulators for testing defense systems. He outlined the possible use of transputers in such a simulator.

-- David Tanqueray of Floating Point Systems finished the final session with a talk on the T series computers produced by his company. These all use transputers as control units.

The conference was very capably organised by R. Stallard from Loughborough University.

Report of the presentation given by Sension Ltd
to The Fifth Technical Meeting of the Occam User Group
John Brierly,
Manager - Transputer Products Division.

Sension Ltd, part of the Northwich based Sension Group, described their range of transputer products, in particular the Transputer Evaluation System developed in conjunction with Sheffield University and the Megaframe transputer systems manufactured in West Germany by Parsytec GmbH.

The Transputer Evaluation System has been designed to provide true parallel processing on a desk top. The initial versions of the product are aimed specifically at Nimbus and IBM PC users who want "hands-on" experience of using the latest version of occam (occam-2), either with a single transputer or several transputers linked together to form a network.

The latest version of the Parsytec Megaframe was described, together with details of the range of plug-in modules. These included two new VME bus bridges, a versatile Transputer Front End module, a High Speed Data Acquisition Interface and a High Resolution Graphics Sub-System.

Sension indicated that its role will be to use its technical and commercial resources to explore and develop new products incorporating transputer technology. The company intends to design its own transputer based products and to enter into collaborative development arrangements with other organisations where this would be mutually beneficial.

Demonstrations of the Transputer Evaluation system and Parsytec Products took place throughout the meeting.

Report on Software Engineering, occam and Research
Dan Simpson
The Alvey Directorate and Sheffield City Polytechnic

The aim of this talk was to introduce some of the current government initiatives in UK R&D in software engineering and relate them to current and proposed work in occam.

Following an overview of the Acard Report on Software, the work of the IT86 committee, SERC, the STARTS initiative and other current government concerns, the presentation concentrated on the Alvey view of software engineering. The importance of the IPSE view was stressed with particular emphasis on the need to interface occam development tools to other tools to support project management. Delegates' attention was drawn to PCTE as an emerging de facto European standard for such an interface.

The presentation concluded with an overview of the Alvey projects which include occam and the transputer. The Forsite project was proposed as one system to which occam development tools could be interfaced. The longer term suggestion was that a formal specification in Z and CSP could be developed using the Forsite system, such a specification could then be transformed smoothly and currectly into an occam implementation.

The conclusions drawn were that there is much research currently under way which could be of benefit to the occam community; by using the results of such work research in the occam arena can gain much and progress quickly. This should allow high quality occam and transputer based systems to be brought to the market in quite a short timescale.

Report on UNIX SIG meeting

Peter Welch,
University of Kent.

As with the other SIGs, a very large number of people (>100) attended. No formal 'mini-presentations' were made, but a more-or-less controlled discussion took place from which emerged a few facts and several concerns.

Initially, we tried to find out the ways in which UNIX was of 'special interest' to us. There seemed to be three categories: using existing UNIX systems to host occam/Transputer application development (i.e. the TDS); using Transputer networks to host UNIX; using UNIX to provide the run-time system on each node of a Transputer target network(!).

The last category had been included because of the apparent intention of a large American university reported in a recent publication of good repute. Happily, representatives of that institution who were present were able to deny any such masochism and this category was deleted.

The chairman distributed his paper on the current state of occam systems under UNIX (further copies for updated contributions to him please) and, in particular, the latest version of the VAX/UNIX OPS 2.0 compiler/run- time system.

Colin Whitby-Strevens, Manager, Microcomputer Support at INMOS, was spotted at the back of the room and "volunteered" to report on the current INMOS policy for non-Transputer based hosts. Because of manpower problems, it seems that INMOS will not be able to maintain support for its existing software tools (i.e. the TDS) executing on non- Transputer targets (i.e. the 8086 (PC), the 68000 (Stride) or the VAX. Future products (like alien languages, new releases of occam 2, ...) will only be targeted to the Transputer. Non-Transputer hosts will only be used as dumb peripheral controllers (for terminals/file-stores) on behalf of tightly-coupled (i.e. high bandwidth connection) Transputer cards on which the real development will take place. Such cards are available for PCs and will become available for VAXes and SUNs. Similar cards for other UNIX workstations (together with similar host file- server software) may also become available from sources other than INMOS. Colin apologised for the disquiet that his announcement raised and bravely stayed in the hot seat to face the audience. He noted that, as he had been away from INMOS in the U.S. for a few days, the whole policy may have shifted! Hopefully, there will be a statement of the current INMOS position on these matters elsewhere in this newsletter.*

The implications of this policy seem to be these. A single user working on a SUN, or a VAX, will be better off (having probably invested in a Transputer board in any case) and will certainly get better response from it running the TDS.

Multiple users have a problem. Whereas before they could just log in to their existing investment of, say, a large VAX cluster and start working, now they will have to queue up to gain exclusive use of a Transputer card. Colin was asked about multi-user versions of the TDS. He said this was being considered but that there are problems of robustness. If two users were developing software on the same Transputer and one divided by zero, both would be zapped. Multiple users require separate Transputer sub-networks. For the same reason, systems software (e.g. for routing data to/from a file server) requires dedicated Transputer "highways" distinct from the user from multiple- user development systems based on

*The Inmos position on the matter is still under review and no statement is yet available.

parallel, software re-configurable Transputer arrays. The cost/benefit ratio ought to be impressive compared with a conventional multi-user VAX ... but when will it be available?

Moving the TDS exclusively to a Transputer environment may accentuate another serious problem. Under "mature" systems like UNIX, a great number of software tools have been accumulated to help develop (or manage the development of (large systems. Indeed, pressures are being applied by large customers on systems developers to force/encourage the use of such tools (e.g. the STARTS programme). Future environments (e.g. the Alvey IPSEs) are hosted on traditional (UNIX) workstations or mainframes. How are the TDS users going to be able to exploit these 'mainstream' developments? They seem to be very well insulated from them!

An elegant solution to the problem of integrating the TDS within an IPSE (or even UNIX) needs to be found. Maybe this will have to await the multi-user re-configurable Transputer network, so that the IPSE (or UNIX) can follow the TDS on to the same hardware. Maybe the C/Transputer compiler will help. Is anybody out there doing this and willing to talk? How urgent are these problems? Please would all interested organisations send me their views (and news) so that we can get an overall picture. Let's discuss this more fully at the next SIG meeting (at the Surrey OUG conference). Has anyone (e.g. Industry/Alvey/ESPRIT/SERC...) got any money left? If not, do we just forget about these matters? My address is on the back page of this newsletter.

NEW PRODUCTS AND SERVICES

Occam and Transputer products from INMOS.

Dave McCusker, INMOS

The continuing expansion of the transputer family from INMOS confirms its commitment to be a leader in parallel processing technology. In addition to the T414 32 bit processor and the 16 bit T212, the M212 disk processor and the T800 Floating Point Transputer are being introduced.

The IMS T414 32 bit processor has been available for over a year and has been accepted as a major step in the development of parallel processing. It offers the user 10 MIPS processing power with memory and communication capability, all on a single CMOS chip in a 84 pin package. It has 2 KBytes of high speed (50ns) on-chip RAM and 4 gigabytes of linear address space with a 25 MByte/sec memory interface. The four links on each T414 have full duplex DMA transfer and are capable of up to 20 MBits/sec.

The 16 bit transputer, the IMS T212, was released soon after the T414 and like it offers 10 MIPS processing power with 2K memory and 4 inter- transputer links, each with full duplex DMA transfer at 20 Mbits/sec.

The IMS T800 is the latest addition to the transputer family and is expected to be the world's fastest 32 bit microprocessor, capable of sustaining well over one million floating point operations per second. The T800 is pin compatible with and retains all the capabilities of the established T414 transputer. In addition, it incorporates an on-chip floating point unit, novel instructions to support graphics and 4 KBytes of on-chip RAM i.e. double that of the T414. The T800 also has double the data transfer rate of the T414 on the communication links thus enhancing system performance. Shipments will begin in 1987.

The IMS M212 disk processor is a 16 bit transputer capable of 10 MIPS with 2 KByte of on-chip SRAM, an external memory interface, two INMOS serial links and a fully programmable disk controller providing industry standard A400/ST506 interfaces. It controls up to four disk drives (either floppy or winchester) and provides data buffering either in internal or external RAM. The M212 is a 68 pin CMOS chip and is the only controller that can be programmed in a high level language and has compatibility at both program and

interface level with all other transputer products. Samples are available now with full production scheduled for February 1987.

There are now also an increasing number of boards available for evaluation of the transputer products. These boards are available in one of two formats: double eurocard and IBM PC compatible boards. The IBM boards can be run individually on a PC (XT or AT compatible) or can be used to control a number of other boards attached to the system. The IBM PC boards are the IMS B004 and the IMS B009, the B004 having one transputer plus memory whereas the B009 has options of 16 or 32 bit transputers with four IMS A100 digital signal processing chips.

The other boards include the B003 which has 4 T414s, the B005 which includes the M212, the B006 having options or one or nine 16 bit transputers and the B007 which has the G170 INMOS colour look-up table on board.

Both IBM boards can be supplied with the necessary software (IMS D701, Transputer development System) to compile and run occam programs on the transputer. Compilers will soon be available to allow the user to run sequential parts of the programs in C, Fortran and Pascal all within an occam harness. INMOS are also developing a version of the Transputer Development System which will allow users to work with occam in the VAX/VMS environment. These will allow programs developed under VMS to be downloaded to transputer boards.

For your general information INMOS have recently moved to new offices in the north of Bristol. The new address is :

INMOS Ltd,
1000 Aztec West,
Almondsbury,
Bristol,
BS12 4SQ.

Overview of the IMS T800-20 / IMS T800-30* transputer

FEATURES

Integral hardware 64 bit floating point unit
ANSI-IEEE 754-1985 Floating Point Representation
1.5(2.25*) Sustained MegaFlops/sec
Full 32 bit transputer architecture
Pin compatible with the IMS T414-20 transputer
4 Kbytes RAM on chip for 80(120*) Mbytes/sec data rate
32 bit configurable memory interface
External memory bandwidth 26.6(40*) Mbytes/sec
High performance Graphics support
Single 5 MHz clock input
Power dissipation less than 1 Watt
DRAM refresh control
Four 10/20 Mbits/sec INMOS serial links
External event interrupt
Internal timers
Support for run-time error diagnostics
Boot from ROM or link

APPLICATIONS

Scientific and mathematical applications
High speed multi processor systems

High performance graphics processing
Supercomputers
Workstation clusters
Digital signal processing
Accelerator processors
Distributed databases
Simulation
Telecommunications
Robotics
Fault tolerant systems
Image processing
Molecular modelling
Pattern recognition
Artificial intelligence

Programming the IMS T800

The IMS T800 transputer can be programmed in several languages including occam, C, Fortran and Pascal.

The transputer provides direct support for the occam model of concurrency and communication. It has a scheduler which enables any number of concurrent processes to be executed together, sharing the processing time. The number of registers which hold the process context is small and this, combined with fast on-chip RAM, provides a sub-microsecond process switch time.

IMS T800 floating-point transputer

The IMS T800 is a 64-bit floating point member of a family of transputers, all of which are consistent with the INMOS transputer architecture, described in the transputer reference manual.

The IMS T800 integrates a 32-bit microprocessor, a 64-bit floating point unit, four standard transputer communications links, 4K bytes of on-chip RAM, a memory interface and peripheral interfacing on a single chip, using a 1.5 micron CMOS process.

The Central Processor

The design achieves compact programs, efficient high level language implementation, and provides direct support for the occam model of concurrency. Procedure calls, process switching and interrupt latency are all sub-microsecond. The processor shares its time between any number of concurrent processes. A process waiting for communication or a timer does not consume any processor time. Two levels of process priority enable fast interrupt response to be achieved.

Floating point unit

The 64-bit floating point unit provides single length and double length operation according to the ANSI-IEEE 754-1985 standard for floating point arithmetic and is able to perform floating point arithmetic operations concurrently with the processor; sustaining in excess of 1.5 Mega Flops.

Links

The IMS T800 uses a DMA block transfer mechanism to transfer messages between memory and another transputer product via the INMOS links. The link interfaces and the processor all operate concurrently, allowing processing to continue while data is being transferred on all of the links.

The four standard INMOS serial links on the IMS T800 give a unidirectional transmitted data rate of 1.7 Mbytes/sec and a combined (bidirectional) data rate per link of 2.3 Mbytes/sec, at a link speed of 20 Mbits/sec. Link speeds of 10 Mbits/sec and 5 Mbits/sec are also available

on the IMS T800 making the device compatible with all other INMOS transputer products. The significant improvement in link performance has been made possible allowing the acknowledge packets to be sent before the data packet has been fully received. The presence of overlapped acknowledges is fully compatible with all other INMOS transputer products.

Memory system

The 4K bytes of on chip static RAM provide a maximum data rate of 80(120*) MBytes/sec with access for both the processor and links. The IMS T800 can directly access a linear address space up to 4 Gbytes. The 32 bit wide external memory interface uses multiplexed data and address lines and provides a data rate of up to 40* MBytes/sec. A configurable memory controller provides all timing, control and DRAM refresh signals for a wide variety of memory systems. Internal and external memory appear as a single contiguous address space.

Peripheral interface

The memory controller supports memory mapped peripherals, which may use DMA. Links may be interfaced to peripherals via an INMOS link adaptor. A peripheral can request attention via the event pin.

Time

The processor includes timers for both high and low priority processes.

Error handling

High-level language execution is made secure with array bounds checking, arithmetic overflow detection etc. A flag is set when an error is detected. The error can be handled internally by software or externally by sensing the error pin. System state is preserved for subsequent analysis.

Package

The IMS T800 will be available in an 84 pin grid array.

Floating point performance

The operation times of the IMS T800 are shown below

	T800-30		T800-20	
	single length	double length	single length	double length
operation				
add	233 nS	233 nS	350 nS	350 nS
subtract	233 nS	233 nS	350 nS	350 nS
multiply	433 nS	700 nS	650 nS	1050 nS
divide	633 nS	1133 nS	950 nS	1700 nS

The operation time is not a reliable measure of performance on real numerical programs. For this reason, floating point performance is often measured by the Whetstone benchmark. The Whetstone benchmark provides a good mix of floating point operations, and also includes procedure calls, array indexing and transcendental functions. It is, in some sense, a 'typical' scientific program.

The performance of the IMS T414 and IMS T800 compared with other processors as measured by the Whetstone benchmark is shown below:

processor		Whetstones/second single length
Intel 80286/80287	8 MHz	300K
IMS T414-20	20 MHz	663K
NS 32332-32081	15 MHz	728K
MC 68020/68881	16/12 MHz	755K
ATT 32000/32100		1000K
Fairchild Clipper	33 MHz	2220K
IMS T800-20	20 MHz	4000K
IMS T800-30	30 MHz	6000K

This table shows that although the IMS T414 has an operation time three times slower than the MC68881 co-processor it performs only 20 % worse than the MC68020 + MC68881 co-processor (as measured by the Whetstone benchmark). This is because the speed of evaluating a floating point expression depends on two factors; the speed at which operands are transferred to and from the floating point unit and the speed of the unit itself. By careful balancing of these the single chip IMS T800-20 achieves more than five times the Whetstone performance of the MC68020/MC68881 combination.

Another important measure is the performance obtained from a given area of silicon. For example, four IMS T800-30 chips occupy an area similar to the i80386 together with the Weitek 1167 chip set, and on single length floating point will deliver 6 times the performance in any concurrent application. In terms of circuit board area, the effect is even more dramatic; the IMS T800 requires negligible support circuitry and can even be used without external memory.

IMS T800 graphics capability

The IMS T800 has a microcoded graphics capability; three new instructions have been added to increase the speed of operation when block transfering two dimensional arrays of bytes. Block moves operate at the speed of memory.

The two dimensional block move instructions provide for contiguous block move as well as both transparent and inverse transparent modes of operation. These transparent modes allow either only non-zero, or only zero bytes of data to be block copied respectively.

The two dimensional block move instructions can be used to provide graphics operations such as text manipulation, windowing, panning, scrolling and screen updating.

Bit counting instruction

The IMS T800 provides an instruction which counts the number of bits set in a word; particularly useful in a number of digital signal processing applications, especially pattern recognition.

Cyclic Redundancy Checking

Two instructions have been included in the IMS T800 to provide the ability to perform Cyclic Redundancy Checks (CRC) on serial data streams of arbitrary length. Cyclic redundancy checks are used to provide error detection in situations where data integrity is critical.

Configurable Memory Interface

The IMS T800 has a configurable memory interface designed to allow easy interfacing of a variety of external memory types with minimal extra components. The interface can directly support DRAMs, SRAMs, ROMs and memory mapped peripherals. The IMS T800 has a 32 bit mulitplexed data and address bus with a linear address space of 4 Gbytes. There are 4

byte write strobes, a read strobe, a refresh strobe, 5 configurable strobes, a wait input, a memory configuration input, a bus request input and bus grant output. With this flexible arrangement, a variety of memory timing controls can be obtained with little external hardware.

Refresh

The IMS T800 has an on-chip refresh controller and 10 bit refresh address counter and can, therefore, refresh DRAMs of up to 1Mbit by 1 bit capacity without requiring the counter to be extended externally.

Setting the Memory Interface Configuration

Despite the high speed of the IMS T800 processor, the memory interface is fully configurable and capable of supporting low speed dynamic RAMs. A memory interface configuration is specified by a 36 bit word and is set at reset time. The IMS T800 has a selection of 13 pre-programmed configurations. If none of these is suitable, the user may supply a configuration word to the IMS T800 MemConfig input immediately following reset. Using a pre-programmed configuration has the advantage of requiring no external components; only a connection from MemConfig to the appropriate data line.

The Memory Interface Program

The INMOS Transputer Development System includes an interactive program which assists in the task of memory interface design.

IMS T800 pinout

The IMS T800-20 is pin compatible with the IMS T414-20 transputer.

IMS T800 Internal speed selection

Two package pins are available on the IMS T800 to allow the internal clock frequency of the processing unit to be determined by the user; up to the maximum rated clock frequency for the device. These pins are called ProcSpeedSelect0 and ProcSpeedSelect1. They are both HoldToGND inputs on the IMS T414 which therefore makes the T800 compatible with an IMS T414-20 part (20 MHz).

Designation	Processor clock speed	Processor cycle time	Input clock frequency
IMS T800-20	20.0 MHz	50.0 ns	5 MHz
IMS T800-30	30.0 MHz	33.3 ns	5 MHz

Inmos documentation

The following documentation is available, from David McCusker at INMOS:

Document title	Availablity
Transputer Ref Man (Oct 86)	Available
IMS T800 Product Preview	Available
IMS T414 Engineering Datasheet	Available
IMS C004 Datasheet	Available
IMS T800 Product data	Available
IMS M212 Product data	February
Occam 2 Tutorial DP+Occam 2 DEF	Available
Occam 2 Ref Man	February
Compiler Writers Guide	February

Technical Notes :

0 Transputer based navigation system	Available
1 Extraordinary use of links	Available
2 Testing embedded systems	Available
3 Getting started with the TDS	Available
4 TDS EPROM programming	Available
5 Program design for concurrent systems	Available
6 IMS T800 Architecture	Available
7 Exploiting concurrency; a ray tracing example	Available
10 IMS B003 design of multi-transputer board	Available
11 IMS B004 IBM PC add-in board	Available
12 IMS B007 A transputer based graphics board	Available
13 Transputer networks using the IMS B003	Available
14 IMS B006 A single board computer using T212	Available
15 IMS B005 Design of a disk controller board	Available

Notes on the boil and likely to be available before March :

8 IMS B010 NEC add-in board
9 Designing with the T414 T800 memory interface
16 Developing occam programs for the transputer
20 Communicating processes and occam
21 The transputer implementation of occam
22 Communicating process computers
23 Compiling occam into silicon
24 Exploring multiple transputer arrays
25 Occam 2: aspects of the language and its development
The Philosophy of occam
Guide to configuration
Maximising performance

The following Oxford PRG monographs are also available :

The laws of occam programming
Exploiting parallelism in the graphics pipeline
The pursuit of deadlock freedom
Formal methods applied to a Floating Point number system

TDS for Sun Workstations

Paul Bently, Logica Cambridge ltd.

The Sun TDS is based upon the INMOS portable TDS release 2 and runs on a Sun Workstation under Sun UNIX 4.2 release 3. The Sun TDS functionally resembles versions available on the Sage, Stride and IBM PC, and includes the following notable features:

occam 2 compilers for the Sun and Transputer;
programs (ie both user programs and the TDS itself) may be executed on either the Sun, or on a Transputer with the Sun acting as a terminal/file server;
two means of communication with remote Transputer hardware are supported: RS232 and VME/link adaptor; sufficient source code is provided to allow incorporation of alternative communication mechanisms;
an extra utility set allows importing/exporting of folds from/to the UNIX file system;
the terminal handler exploits the Termcap facilities in order to achieve terminal independence.

The VME/link adaptor board referred to above was developed by INMOS and RSRE. The board plugs directly into the VMEbus and provides a single INMOS serial link together with Reset, Analyse and Error signals and is suitable for use with the INMOS evaluation boards.

The Sun TDS will be passed back to INMOS for further development, but can be obtained as an unsupported development release directly from Logica. The price for a single machine is £750 (£400 for academic institutions). The pricing for multiple machines is based on the number of executing hosts in a network, ie processors on which the TDS is run rather than file servers or workstations. The release consists of:

Sun cartridge tape containing the TDS
brief installation guide
IMS D100 B / D200 B user documentation
occam 2 product description

Further information on pricing and licencing is available from:

Paul Bentley
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Betjeman House
104 Hills Road
Cambridge CB2 1LQ
UK

Telephone 01 637 9111 or 0223 66343
Telex 27200
Facsimile 0223 322315
Electronic mail pcba@uk.alvey
Telecom Gold 83:LUK085

Low cost transputer module

Concurrent Technology has produced a low-cost Transputer module, containing an IMS T414-15 Transputer, with 256K of DRAM, on a small four-layer PCB approximately 75 mm by 595 mm. The price (1 to 5) will be £600.00.

Further details from:

Leon Heller,
Concurrent Technology,
30 Baldslow Road,
Hastings,
E. Sussex. TN34 2EY
Tel: (0424) 714790

Transputer network capability

Sension Ltd launched their entry-level transputer evaluation systems during August 1986. These systems are cased, powered and ready to go; they contain from one to four transputers and support the occam-2 language environment. The first systems was available from August for use with Nimbus machines, and will allow a potential transputer user to evaluate occam and small transputer networks. An IBM PC version was available from September.

Further information from John Brierley or Andy Graham at Sension Ltd, Denton Drive, Manchester Road, Northwich, Cheshire, CW9 7LU (Northwich 0606 - 44321).

UNIX is a trade mark of Bell Laboratories.

Occam and transputer engineering
Computing Laboratory, University of Kent at Canterbury

Course Objectives:

To acquire technical knowledge, insight and practical experience of parallel system design using occam and Transputer networks. Software engineering principles, real-time applications, load-balancing techniques and super-computing issues will be covered.

Course Members:

Engineers with some experience of a traditional "high-level" language. (Note: we have found that hardware engineers, with only a modest knowledge of software, find the occam concepts for parallelism particularly easy to master.)

Course Methods:

Informal lectures with a large proportion of "hands-on" experience being provided through practical exercises and a "mini-project". Practical work will be on one of the University's mainframe computers and will be supervised at the ratio of one tutor for every six attendees. The course size is limited to eighteen attendees. The MEiKO* Computing Surface* - an infinitely expandable, user configurable Transputer network - will be demonstrated.

Length & Cost:

Four days & £270 per person (inclusive of lunches, coffee, tea and biscuits).

Dates:

Course No. 2: 18-19, 25-26 March 1987
Course No. 3: 31 March - 3 April 1987

Contact:

For a full syllabus, application forms, special arrangements and accommodation, please contact Dr. P. H. Welch, Computing Laboratory, The University, Canterbury, Kent, CT2 7NF (Tel: 0227-66822 ext. 3629) (JANET: phw@uk.ac.ukc).

ARTICLES

Two Dimensional Block Move Instructions on the T800
Guy Harriman,
Inmos Ltd.

1.1 Introduction

In addition to the support for floating point arithmetic the T800 transputer has special instructions for two-dimensional block moves.

Three new instructions of this kind have have been provided. The instructions differ in how the source and destination data are combined. Their function may best be described by occam PROCs.

*MEiKO and the Computing Surface and trademarks of Meiko Limited.

1.1 Two-Dimensional Block Moves Of All Bytes

```
PROC Move2D (VAL[][]BYTE Source, VAL INT sx, sy,
             [][]BYTE Dest, VAL INT dx, dy,
             width, length)
 SEQ y = 0 FOR length
  [Dest[y+dy] FROM dx FOR width] :=
   [Source[y+sy] FROM sx FOR width]
:
```

This moves a block of size (width, length) which starts at byte `Source[sy][sx]` to the block starting at byte `Dest[dy][dx]`.

The Move2D procedure is implemented by the instruction Move2DAll.

1.2 Two-Dimensional Block Move Of Non-Zero Bytes

```
PROC Draw2D (VAL[][]BYTE Source, VAL INT sx, sy,
             [][]BYTE Dest, VAL INT dx, dy,
             width, length)
 BYTE temp:
 SEQ line = 0 FOR length
  SEQ point = 0 FOR width
   SEQ
    temp := Source[line+sy][point+sx]
    IF
     temp = (BYTE 0)
      SKIP
     TRUE
      Dest[line+dy][point+dx] := temp
:
```

This moves a block of size (width, length) which starts at byte `Source[sy][sx]` to the block starting at byte `Dest[dy][dx]`. However for every byte transferred a check is made to see if it is zero. If this is the case then that byte is not copied, and the destination remains unaltered.

The Draw2D procedure is implemented by the instruction Move2DNonZero.

1.3 Two-Dimensional Block Move Of Zero Bytes

```
PROC Clip2D (VAL[][]BYTE Source, VAL INT sx, sy,
             [][]BYTE Dest, VAL INT dx, dy,
             width, length)
 BYTE temp:
 SEQ line = 0 FOR length
  SEQ point = 0 FOR width
   SEQ
    temp := Source[line+sy][point+sx]
    IF
     temp = (BYTE 0)
      Dest[line+dy][point+dx] := temp
     TRUE
      SKIP
:
```

This moves a block of size (width, length) which starts at byte `Source[sy][sx]` to the block starting at byte `Dest[dy][dx]`. However for every byte transferred a check is made to see if it is zero. If this is the case then that byte is copied.

The Clip2D procedure is implemented by the instruction Move2DZero.

1.4 Use Of Two-Dimensional Block Move

Draw2D and Clip2D are complementary. Draw2D is used for the copying of irregular shapes onto the screen. Clip2D is used in the creation of templates, where non-rectangular shapes are masked out from a picture. Complex shapes can be formed easily by multiple use of Draw2D and Clip2D to form images, before copying the shape with Move2D to a video frame buffer for display.

1.5 Passing Parameters To The Instructions

Six parameters are required to perform two-dimensional block moves. They are :

1 The address of the least significant byte to be copied from (the first source byte) 2 The address of the least significant byte to be copied to (the first destination byte)
3 The width or number of bytes in each row to be copied
4 The length or number of rows to be copied
5 The stride or number of bytes in each row of the source array
6 The stride or number of bytes in each row of the destination array

The instruction Move2DInit sets up three of these parameters in the reserved workspace in internal memory between #80000048 (above the interrupt save space) and #80000070 (MemStart). Three words of the reserved workspace are used for low priority two-dimensional block moves, and three other words of the reserved workspace are used for high priority two-dimensional block moves. On entry to Move2DInit the stride of the source array is in the C register, the stride of the destination array is in the B register, and the length is in the A register.

The three instructions Move2DAll, Move2DNonZero, and Move2DZero contain on entry the address of the first source byte in the C register, the address of the first destination byte in the B register, and the width in the A register.

2 Relative Performance on the T800

The occam procedures and the equivalent instructions were executed with code and data in external memory for a range of array sizes on one of the first T800s packaged. This T800 was put on an Inmos B004 evaluation board having four cycle external memory, and operated at 20 MHz processor cycle frequency. All the benchmarking was done at high priority, in order to prevent the screen and keyboard handling from timeslicing the execution of the program.

The size of the destination array was 1024 by 1024. The source arrays were not initialised, and so contained an arbitrary number of zero value bytes. Therefore it is not relevant to compare the times taken for Clip2D and Draw2D for any array size. However, the relative performance for each array for the procedure and the equivalent instructions for Clip2D and Draw2D are based on identical initial conditions, and these may be meaningfully compared.

The following results were obtained :

Source Array Size	Type of Move	Time For Procedure	Time For Instruction
512 * 512	Move2D	30318 uSec	27015 uSec
512 * 512	Draw2D	1595661 uSec	18262 uSec
512 * 512	Clip2D	2359623 uSec	26227 uSec
256 * 256	Move2D	8502 uSec	6839 uSec
256 * 256	Draw2D	399061 uSec	4702 uSec
256 * 256	Clip2D	590293 uSec	6551 uSec
8 * 8	Move2D	72 uSec	14 uSec
8 * 8	Draw2D	442 uSec	14 uSec
8 * 8	Clip2D	579 uSec	14 uSec
1 * 1	Move2D	16 uSec	4 uSec
1 * 1	Draw2D	20 uSec	3 uSec
1 * 1	Clip2D	16 uSec	4 uSec

It can be seen that the overhead of doing one-dimensional block moves and a replicated SEQ in Move2D falls from 500% for an 8*8 array to 12% for a 512*512 array.

It can also be seen that the overhead of detecting zero value bytes and conditionally storing them one a time in Draw2D and Clip2D increases from a factor of 30 for an 8*8 array to a factor of 90 for a 512*512 array.

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The group now has more than a thousand members on its mailing list!

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