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M U L T I C L U S T E R Series

Hardware Documentation

TPM-4

Transputer Processor Module

Technical Documentation

Version 1.0

July 1987

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Contents:

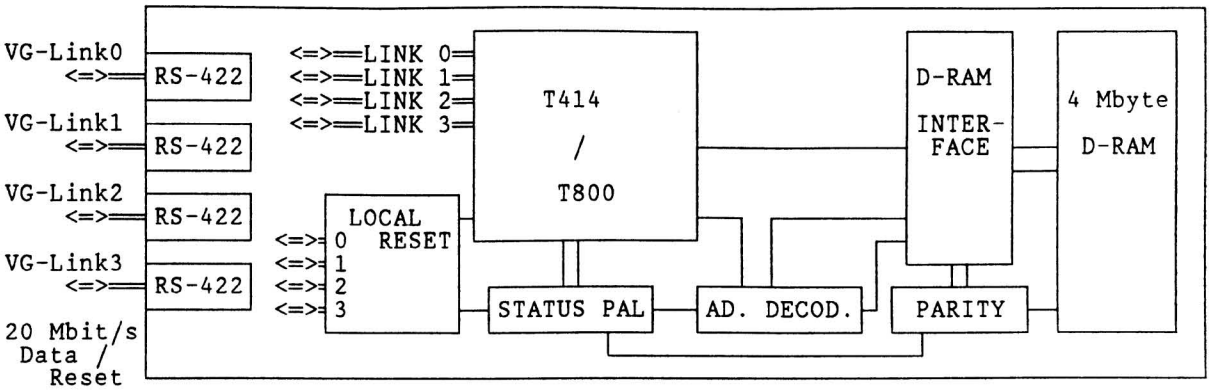


Fig. 1: Block diagram of the TPM-4

The TPM-4 32 bit transputer module has 4 Mbyte of parity protected dynamic RAM (120 ns). The basic version has a 20 MHz T414 (optional T800 floating point transputer).

A status register latches error conditions and can be read at any time. One bit indicates a transputer error, another an address error and four more, parity errors. On any error analyse is asserted which shuts down all active processes. Another transputer may then reset the system via one of its links and analyse the status latch to determine the source of the error.

The 4 transputer links are RS-422 buffered and brought out to the DIN connector. At 20 Mbit/s the maximum distance is 10 m using the PARSYTEC link cable. For greater distances the links can be jumpered to operate at 10 or 5 Mbit/s.

Parallel to each link there is a software controlled bidirectional reset line. Using this, each transputer in a network is able to control by software the activity of the four next neighbours and on an error to reset, analyse and reload them.

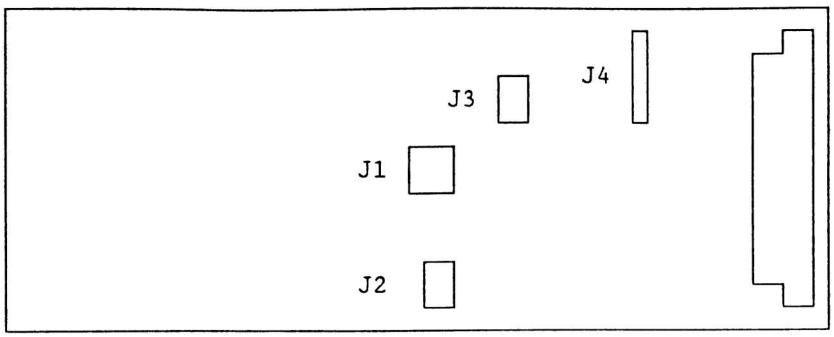


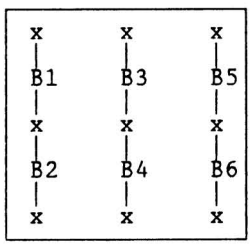
Fig. 2: Jumper Positions

1) Jumper setting

J1: Processor clock T414 (T800)
J2: Memory access
J3: External Error: Analyse, Event, Error
J4: Link speeds

The jumpers within each jumper are numbered beginning with B1 :

J1: Processor clock T414 (T800)

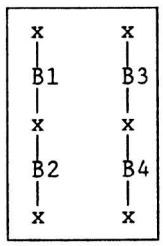


For 20 MHz transputers :

B1, B3, B5 set

Same settings for other frequencies until final definition.

J2: Memory access

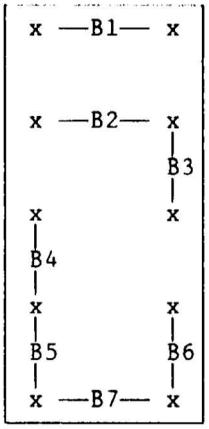


20 MHz transputer, 120 ns RAM: B3 set

20 MHz transputer, 100 ns RAM: B4 set

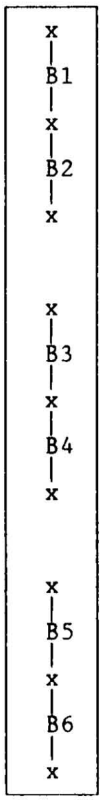
30 MHz transputer, 100 ns RAM: B3 set

J3: External Error



ignore	:	B2, B4, B6	set
Analyse	:	B1, B2, B4, B6	set
Event	:	B2, B5, B6	set
ErrorIn	:	B2, B7, B4	set

J4: Link speeds



The following combinations of link speeds are possible :

all links at 20 MBit/s:	B1, B3, B5
all Links at 10 MBit/s:	B2, B4, B6
all Links at 5 MBit/s:	B2, B3, B5
Link 0 at 20 MBit/s, Link 1-3 at 10 MBit/s:	B1, B3, B6
Link 0 at 10 MBit/s, Link 1-3 at 20 MBit/s:	B1, B4, B5
Link 0 at 10 MBit/s, Link 1-3 at 5 MBit/s:	B2, B4, B5
Link 0 at 5 MBit/s, Link 1-3 at 10 MBit/s:	B2, B3, B6

3) Hardware Addresses

Address space of the T414 (T800)

Hardware address		addresses in current OCCAM 2 implementation PLACEment as word address
0000 00C0	Reset	#2000 0030
0000 0080	Status	#2000 0020
0000 0000	Identification PAL (optional)	#2000 0000
803F FFFF		#000F FFFF
...	4 Mbyte RAM	...
8000 0000		#0000 0000

The identification PAL enables each board to be given a unique 8 byte identity code. These bytes appear in the least significant byte of the following occam addresses:

#20000000	Byte 1
#20000001	Byte 2
#20000002	Byte 3
#20000003	Byte 4
#20000004	Byte 5
#20000005	Byte 6
#20000006	Byte 7
#20000007	Byte 8

4) Software Addresses of the links

After declaring the channel names the following PLACE statements assign the logical channels to the physical links :

```
PLACE Link0.Output AT #0 :
PLACE Link1.Output AT #1 :
PLACE Link2.Output AT #2 :
PLACE Link3.Output AT #3 :
PLACE Link0.Input  AT #4 :
PLACE Link1.Input  AT #5 :
PLACE Link2.Input  AT #6 :
PLACE Link3.Input  AT #7 :
```

5) Bootstrap

The TPM is configured by default to BootFromLink, i.e. after each reset the processor expects the program as a data stream from a link. In this state all 4 links are equal. The first message received on one of the links is interpreted as the boot program and executed.

6) Error and Analyse

There are three sources of error : program, addressing and parity fail. Program errors such as division by 0, integer overflow or array boundary violation are trapped by the transputer and generate an error signal that is latched by the status PAL. The address space is fully decoded and any illegal memory access causes an error bit in the status PAL to be set. Four more bits record any parity errors. When any of these bits are set the PAL asserts analyse wich causes the transputer to shut down all processes. After reset from a link the transputer can be analysed and restarted. The PAL information is preserved until it is read, which clears the PAL and activates error monitoring.

The status PAL address in mentioned above. When set bits 0 to 5 indicate the following errors (active low) :

```
Bit 0 = 0 :  Transputer error
Bit 1 = 0 :  Address error
Bit 2 = 0 :  Parity fail byte 0
Bit 3 = 0 :  Parity fail byte 1
Bit 4 = 0 :  Parity fail byte 2
Bit 5 = 0 :  Parity fail byte 3
```

7) Software controlled Reset

Parallel to each output link is a reset line that is controlled by software and may be used to reset and boot the connected transputer. The following program demonstrates the sequence needed to generate a reset via a link.

```
PROC reset ( VAL INT link )
  --  reset channel 0: link = 1
  --  reset channel 1: link = 2
  --  reset channel 2: link = 4
  --  reset channel 3: link = 8
  INT addr.reset :
  PLACE addr.reset AT #20000030 :  -- reset PAL address
  TIMER clock :
  VAL INT wait IS 2 :              -- 2 times 64 microseconds
  SEQ
    addr.reset := 0                -- this sequence unlocks
    addr.reset := 1                -- the reset PAL
    addr.reset := 2                --
    addr.reset := 3                --
    addr.reset := link             -- number of link to be reset
    clock ? time                   --
    clock ? AFTER time PLUS wait   -- wait 128 microseconds
    addr.reset := 0                -- clear reset
:
```

8) DIN Connector Pinout

c		a
Reset 0 out +	1	Reset 0 out -
Link 0 out +	2	Link 0 out -
GND	3	GND
Link 0 in -	4	Link 0 in +
Reset 0 in -	5	Reset 0 in +
GND	6	GND
Reset 1 out +	7	Reset 1 out -
Link 1 out +	8	Link 1 out -
GND	9	GND
Link 1 in -	10	Link 1 in +
Reset 1 in -	11	Reset 1 in +
GND	12	GND
Reset 2 out +	13	Reset 2 out -
Link 2 out +	14	Link 2 out -
GND	15	GND
Link 2 in -	16	Link 2 in +
Reset 2 in -	17	Reset 2 in +
GND	18	GND
Reset 3 out +	19	Reset 3 out -
Link 3 out +	20	Link 3 out -
GND	21	GND
Link 3 in -	22	Link 3 in +
Reset 3 in -	23	Reset 3 in +
GND	24	Master Reset
	25	
	26	
+ 5	27	+ 5
+ 5	28	+ 5
+ 5	29	+ 5
GND	30	GND
GND	31	GND
GND	32	GND