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M E G A F R A M E Series

Hardware Documentation

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MTM-2 Multi Transputer Module

Technical Documentation

Version 1.3

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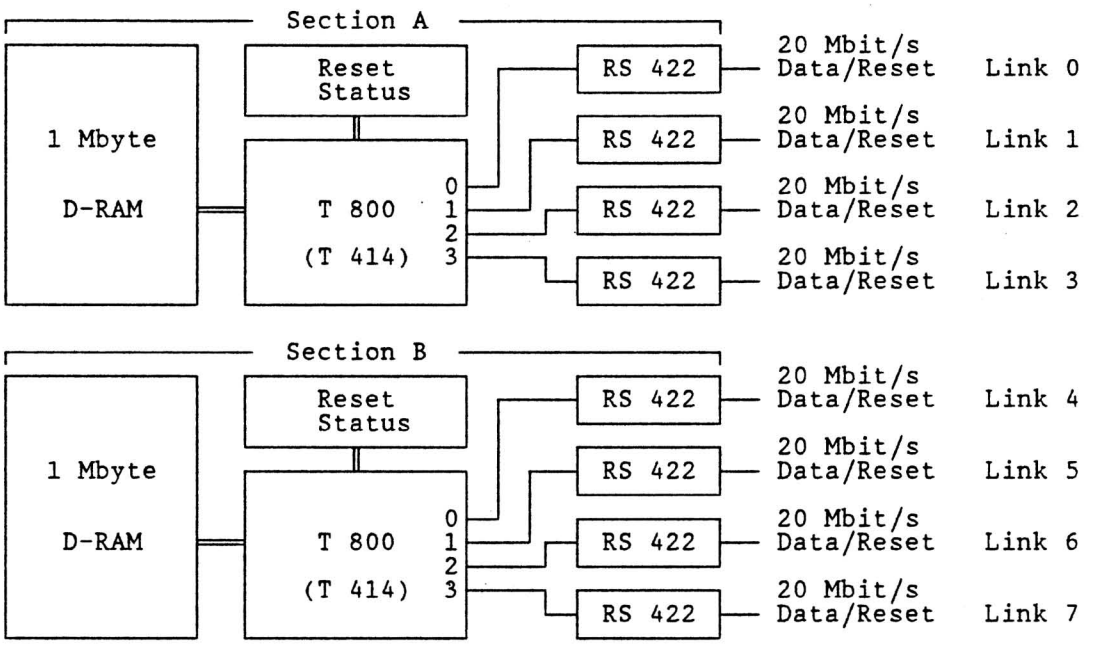


Figure 1: Block Diagram of the MTM-2

The MTM-2 is a 2-transputer module with a processing-capacity of up to 20 MIPS. Every transputer node consists of a T800 (T414) 32 bit transputer with 20 MHz system clock and 1 Mbyte dynamic RAM with an access time of 100 or 120 ns.

The 4 transputer links can be adjusted to 20, 10, or 5 Mbit/s. Two links of each transputer are RS-422 buffered and taken to the VG connector. The remaining 4 links can be switched as desired with each other on the board or buffered and taken to the DIN connectors.

The internal link-cabling of the boards with each other is done by the user via plugable flat-cable-connections on the backplane. Shielded twisted-pair cables connect the links in distributed transputer systems. At a transmission rate of 20 Mbit/s up to 10 m can be covered. For longer distances the links can be tuned to 10 or 5 Mbit/s via jumper.

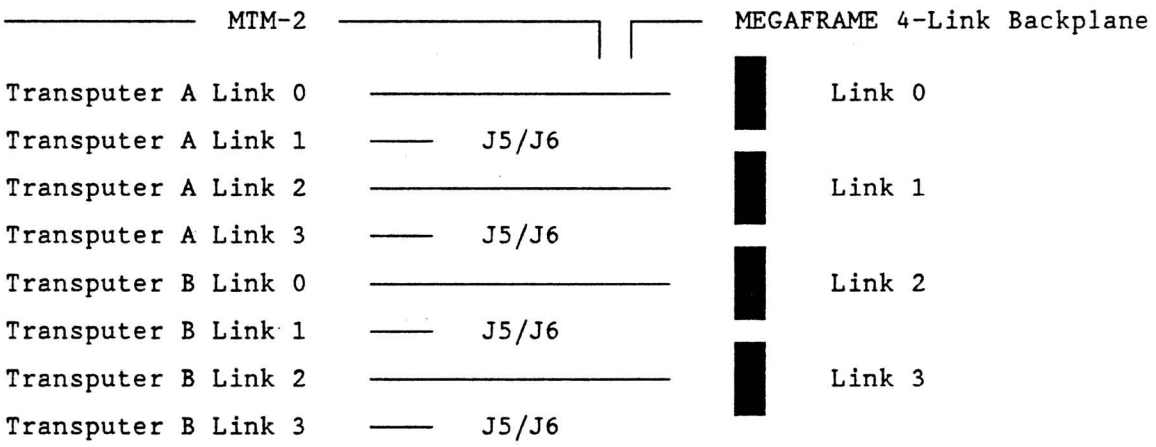
Working concurrently with every link is the possibility of a program controlled bi-directional reset facility. This enables each transputer in a network to control the activation of its 4 neighbours and in the event of an error to reset them and start anew.

A status register holds the transputer error which can be read-out at any required time. One bit each is provided for transputer- and address-errors. According to the jumper selection either the analyse condition is indicated, an interrupt or an external error is generated in the event of an error occurring.

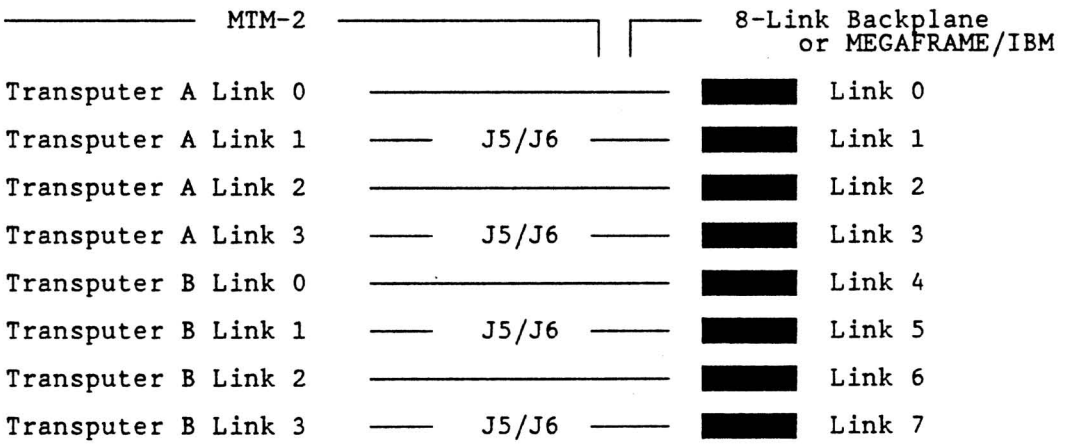
2) The Links

Link 0 and link 2 of each transputer are taken via the RSS-422 buffers directly on to the VG connector, whilst links 1 and 3 are wired optionally on the board or RS-422 buffered and taken to the DIN-connector (jumper J5, J6).

MEGAFRAME 4-Link Backplane



MEGAFRAME 8-Link Backplane and MEGAFRAME/IBM



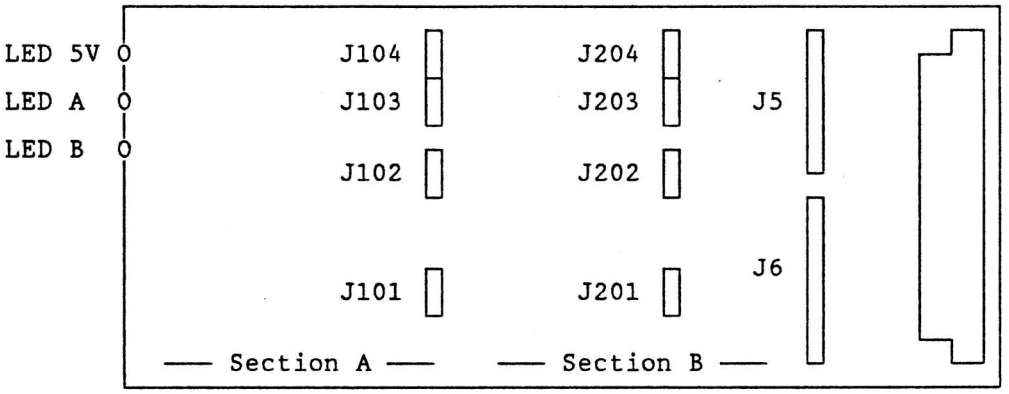


Figure 2: Jumperpositions

3) Jumper Allocations

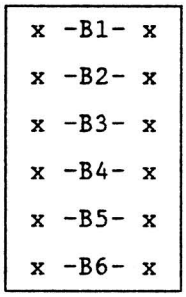
J101/201 Memory access
J102/202 Link speed
J103/203 Clock frequency T800-Processor (T414)
J104/204 External Error: Analysis, Event, Error
J5/6 Link-Configuration

The jumper numbering J1xx describes jumper of transputersection 'A',
the jumper numbering J2xx describes jumper of transputersection 'B'.

J101/201 : Memory access

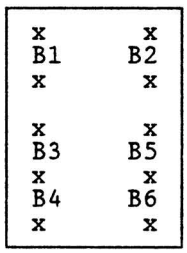
x -B1- x	20 MHz Transputer, 120 ns RAM:	B2 jumpered
x -B2- x	20 MHz Transputer, 100 ns RAM:	B3 jumpered
x -B3- x	30 MHz Transputer, 120 ns RAM:	B1 jumpered
x -B4- x	30 MHz Transputer, 100 ns RAM:	B2 jumpered

J102/202 : Link speed



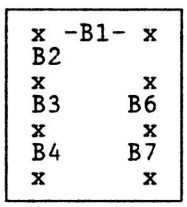
all links at 20 Mbit/s:	B1, B3, B5
all links at 10 Mbit/s:	B2, B4, B6
all links at 5 Mbit/s:	B2, B3, B5
Link 0 at 20 Mbit/s, Link 1-3 at 10 Mbit/s:	B1, B4, B5
Link 0 at 10 Mbit/s, Link 1-3 at 20 Mbit/s:	B1, B3, B6
Link 0 at 10 Mbit/s, Link 1-3 at 5 Mbit/s:	B2, B3, B6
Link 0 at 5 Mbit/s, Link 1-3 at 10 Mbit/s:	B2, B4, B5

J103/203 : Clockfrequency T800 (T414)



For 20 MHz Transputer: B2, B3, B5 jumpered
All other frequencies the same until the final definition.

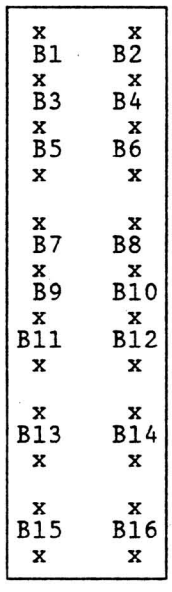
J104/204 : External Error



Analysis	: B1, B4, B7 jumpered
Event	: B1, B3, B6 jumpered
ErrorIn	: B2, B4, B6 jumpered
ignore	: B1, B4, B6 jumpered

J5/6 : Link-Configuration

The jumpers must be plugged-in identically at J5 and J6 !!



Possible Link-Connections :

TP-Section 'A' Link 1 -	TP-Section 'B' Link 1:	B9, B10
TP-Section 'A' Link 1 -	TP-Section 'B' Link 3:	B13, B14
TP-Section 'A' Link 3 -	TP-Section 'B' Link 1:	B15, B16
TP-Section 'A' Link 3 -	TP-Section 'B' Link 3:	B3, B4
TP-Section 'A' Link 1 -	Back-Plane Link 1:	B11, B12
TP-Section 'A' Link 3 -	Back-Plane Link 3:	B5, B6
TP-Section 'B' Link 1 -	Back-Plane Link 5:	B7, B8
TP-Section 'B' Link 3 -	Back-Plane Link 7:	B1, B2

Make only one connection per link !!

4) Hardware Addresses

Address space of the T800 (T414)

Hardware Addresses		Addresses in present OCCAM-2-Implementation PLACEment as word addresse
0000 00C0	Reset	#2000 0030
0000 0080	Status	#2000 0020
0000 0040		#2000 0010
0000 0000	Identification-PAL (optional)	#2000 0000
800F FFFF		#0003 FFFF
...	1 Mbyte working memory	...
8000 0000		#0000 0000

The identification-PAL makes it possible for the user to give every board an identification up to 8 bytes long. These bytes appear in the least significant byte of the foolowing occam addresses :

#20000000	Byte 1
#20000001	Byte 2
#20000002	Byte 3
#20000003	Byte 4
#20000004	Byte 5
#20000005	Byte 6
#20000006	Byte 7
#20000007	Byte 8

5) Software - Link Addresses

After deklaration of the channels the following address assignment for the 4 links of the T800 (T414) are valid:

```
PLACE Link0.Output AT #0 :
PLACE Link1.Output AT #1 :
PLACE Link2.Output AT #2 :
PLACE Link3.Output AT #3 :
PLACE Link0.Input  AT #4 :
PLACE Link1.Input  AT #5 :
PLACE Link2.Input  AT #6 :
PLACE Link3.Input  AT #7 :
```

6) Bootstrap

Each processor of the MTM-2 is configured by default to BootFromLink, i.e. after each reset the processor exspects the program as a data stream from a link. In this state all 4 links have equal priorities. The first message that comes via one of those links is interpreted as a boot program and executed accordingly.

7) Error and Analysis

In the event of errors, the MTM-2 offers the possibility of a systematic shut-down of all processes. In principle, only two types of errors can occur: Program- and address errors. Program errors, such as a division by 0, integer overflow or array boundary violation are signalled by the transputer with setting of the error flag. An external address decoding identifies the exceeding of the on board RAM and sets a bit in status PAL.

According to the jumper selection an error condition will initiate either an analyse condition, an interrupt, generate an external error or do nothing. The analyse condition starts a controlled shut-down of all active processes and the system can be externally analysed after reset and loaded anew. The error condition can also be read-out and analysed. The interrupt activates a service routine in which the user can determine the further process. The external error input of the T800 (T414) has the same effect during activation as an internal transputer error.

The addresses of the status-PAL are listed above. The bits 0 and 1 have the following meaning when set (active low):

Bit 0 = 0 : Transputer error
Bit 1 = 0 : Address error

8) Software controlled Reset

A reset line is lead parallel to every link which sets the addressed transputer in boot-condition. That provides the possibility to supervise the activities of the next four neighbouring transputers and executes a systematic reset in the event of an error. Afterwards they can be provided with a new program code via the links and can be started anew.
The following program example shows the necessary command-sequence for the reset.

```
PROC reset ( VAL INT link)
  --  reset channel 0: link = 1
  --  reset channel 1: link = 2
  --  reset channel 2: link = 4
  --  reset channel 3: link = 8
  INT addr.reset :
  PLACE addr.reset AT #20000030 :  -- address of reset PAL
  TIMER clock :
  VAL INT wait IS 2 :              -- 2 times 64 microseconds
  SEQ
    addr.reset := 0                -- this sequence unlocks
    addr.reset := 1                -- the reset PAL
    addr.reset := 2                --
    addr.reset := 3                --
    addr.reset := link             -- number of link to be reset
    clock ? time                   --
    clock ? AFTER time PLUS wait   -- wait 128 microseconds
    addr.reset := 0                -- clear reset
:
```

Pin-out of 96-way DIN connector (27. 2. 1987)

MTM-2 Rev. 1.1, MTM-4 Rev. 1.1 and GDS Rev 1.0

	c	b	a
1	Reset 0 out +	Reset 1 out +	Reset 0 out -
2	Link 0 out +	Reset 1 out -	Link 0 out -
3	GND	Link 1 out +	GND
4	Link 0 in -	Link 1 out -	Link 0 in +
5	Reset 0 in -	Link 1 in -	Reset 0 in +
6	Link 1 in +	Reset 1 in -	Reset 1 in +
7	Reset 2 out +	Reset 3 out +	Reset 2 out -
8	Link 2 out +	Reset 3 out -	Link 2 out -
9	GND	Link 3 out +	GND
10	Link 2 in -	Link 3 out -	Link 2 in +
11	Reset 2 in -	Link 3 in -	Reset 2 in +
12	Link 3 in +	Reset 3 in -	Reset 3 in +
13	Reset 4 out +	Reset 5 out +	Reset 4 out -
14	Link 4 out +	Reset 5 out -	Link 4 out -
15	GND	Link 5 out +	GND
16	Link 4 in -	Link 5 out -	Link 4 in +
17	Reset 4 in -	Link 5 in -	Reset 4 in +
18	Link 5 in +	Reset 5 in -	Reset 5 in +
19	Reset 6 out +	Reset 7 out +	Reset 6 out -
20	Link 6 out +	Reset 7 out -	Link 6 out -
21	GND	Link 7 out +	GND
22	Link 6 in -	Link 7 out -	Link 6 in +
23	Reset 6 in -	Link 7 in -	Reset 6 in +
24	Link 7 in +	Reset 7 in +	Master Reset
25		Reset 7 in -	
26			
27	+ 5	+ 5	+ 5
28	+ 5	+ 5	+ 5
29	+ 5	+ 5	+ 5
30	GND	GND	GND
31	GND	GND	GND
32	GND	GND	GND