MTM-2-11/12/13

Multi-Transputer Module

Technical Documentation
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1. Introduction

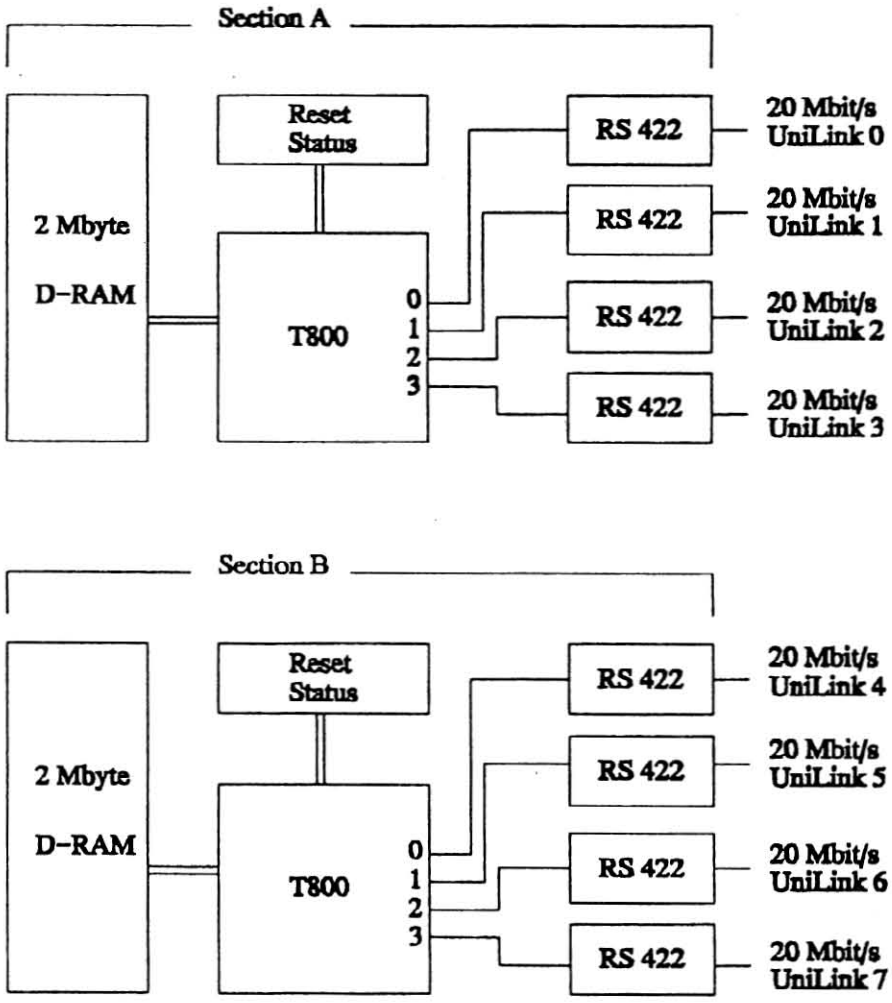
1.1 General Information

The MTM-2-11/12/13 is a module with two T800/805 Transputers and a processing-capacity of up to 20 MIPS. The similar structured boards only differ from the size of dynamik RAM. Available are:

2 MByte DRAM	→	MTM-2-11
4 MByte DRAM	→	MTM-2-12
8 MByte DRAM	→	MTM-2-13

All 8 transputer links are RS-422 buffered and brought out to the rear DIN connector as UniLinks. They can be adjusted to 20, 10, or 5 Mbit/s.

Fig. 1-1: *Block Diagram of the MTM-2-11*



The internal link-cabling of the boards with each other is done by the user via plugable flat-cable-connections either on the backplane of the MultiCluster or on the BBK-PC.

Shielded twisted-pair cables connect the links in distributed transputer systems. At a transmission rate of 20 Mbit/s up to 10 m can be covered. For longer distances the links can be tuned to 10 or 5 Mbit/s via jumper.

Each link is combined with a reset connection, wich supports program controlled resetting of neighbour transputers in both directions. This enables each transputer to reset and reboot its neighbours, e.g. after a software malfunction has been detected.

A status register holds the transputer error which can be read-out at any required time. One bit each is provided for transputer- and address-errors. According to the jumper selection either the analyse condition is indicated, an interrupt or an external error is generated in the event of an error occurring.

For more detailed information please refer to the following chapters.

1.2 Using the board

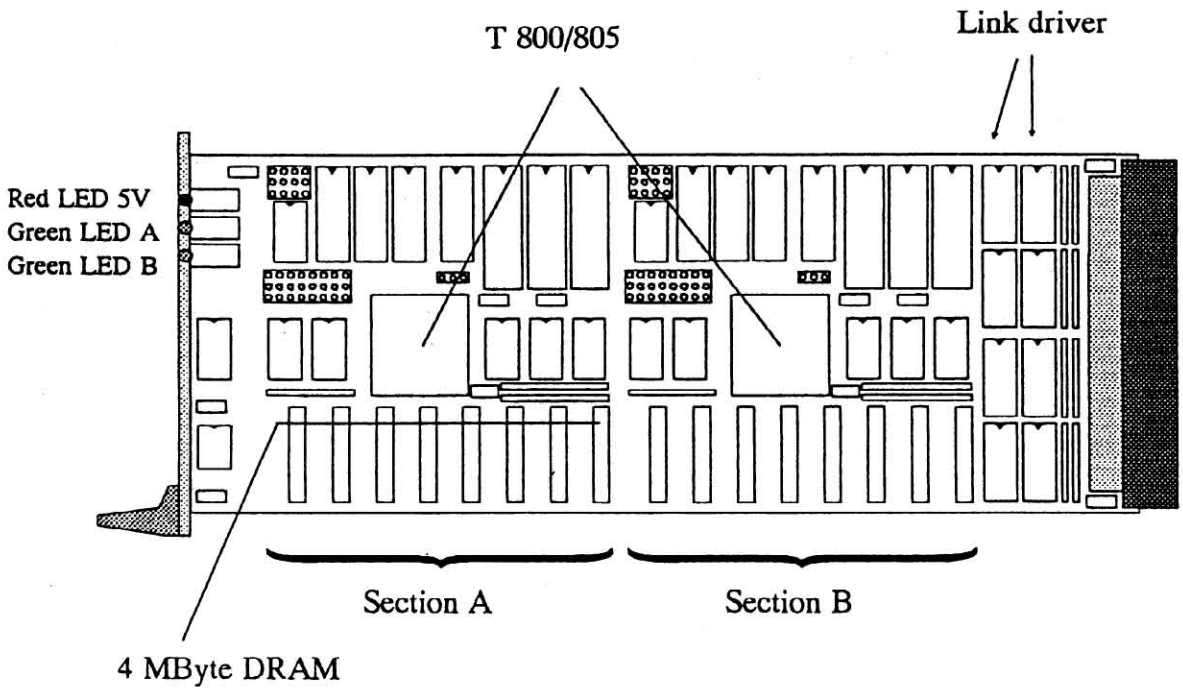
A major application is the MultiCluster-2 which comprises three functional units: the processing subsystem, the I/O subsystem and the configuration control subsystem. For the processing subsystem the MC-2 provides 16 slots for modules such as the MTM-2-11/12/13 board. Which specific board of the MTM-2 series you should use only depends on the dynamik RAM needed by the application running, e.g. Realtime systems such as Image Processing or Number Crunching such as Computational Fluid Dynamics or engineering simulations. Furthermore the processors on the board can be used as host processors in a SuperCluster with a direct link to the host system e.g. PC, Sun Workstation, Apple MacIntosh. You can run for example Helios or Toolset on it.

2. Hardware Description

2.1 Overview

The MTM-2 board has the extended Eurocard form factor of 220 mm * 100 mm and needs one slot to plug into e.g. a MultiCluster or SuperCluster. It is built up of two identical transputer sections and some additional electronics e.g. power supply, I/O functions, etc.. The heart of each transputer section is a INMOS T800/805 with adjustable processor speed between 17.5 MHz and 30 MHz. Furthermore each section has 2 MByte DRAM (MTM-2-11), 4 MByte DRAM (MTM-2-12) or 8 MByte DRAM (MTM-2-13).

Fig. 2-1: *Layout of the MTM-2-12*



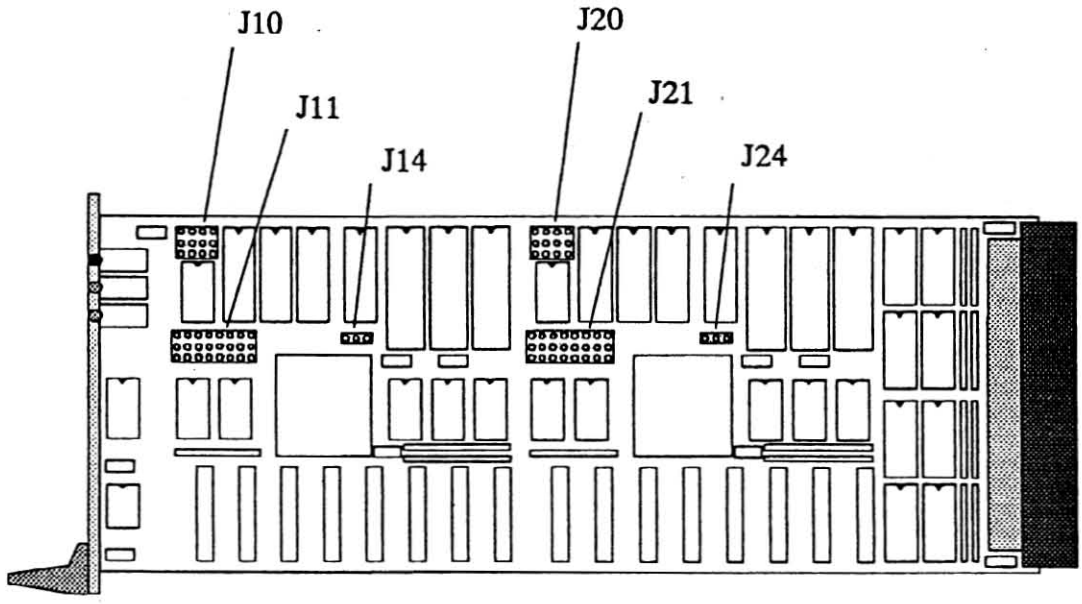
2.2 Jumper

For each transputer section there are two jumper settings which could be changed. The jumpers J10 and J20 are supposed to set the Event Handling respectively the Analyse Handling. With the jumpers J11 and J21 you can adjust the speed control of the board. For more detailed information please refer to chapters 2.2.2 and 2.2.3.

2.2.1 Jumper Allocations

The allocations of the jumpers are indicated in the picture below.

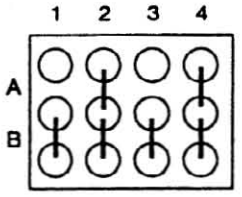
Fig. 2-2: *Jumper positions on a MTM-2-12*



2.2.2 J10, J20: Exeption Handling

Note: These jumpers should not be changed unless you want none Event or Analyse generation.

Scheme :



Details :

- J10, J20 column 1 : internal use

jumper setting	function
1A	**do not jumper!**
1B	standard setting

- J10, J20 column 2 : Event Handling

jumper setting	function
2A	Event on address error
2B	none Event generation

- J10, J20 column 3 : internal use

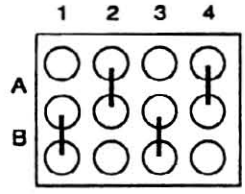
jumper setting	function
3A	**do not jumper!**
3B	standard setting

- J10, J20 column 4 : Analyse Handling

jumper setting	function
4A	Analyse generation for all incoming reset signals via links.
4B	none Analyse generation

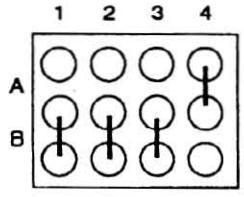
✗ **example setting :**

Event on address error
Analyse on all resets via link :



➪ **default setting :**

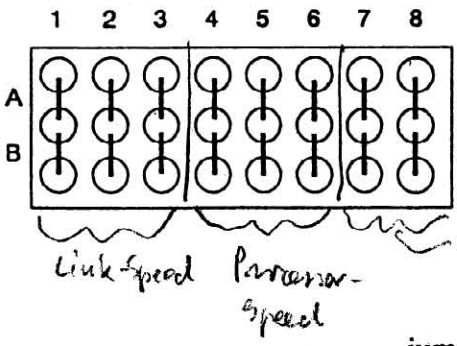
Analyse on all resets via link :



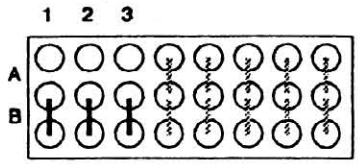
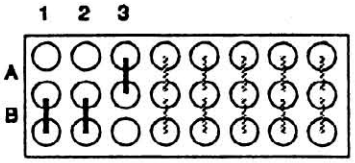
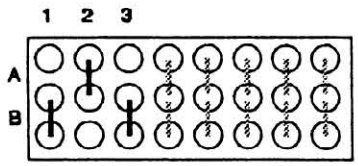
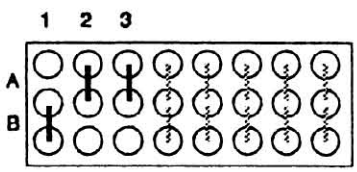
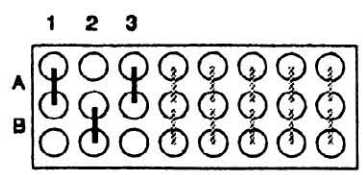
2.2.3 J11, J21 : Speed control

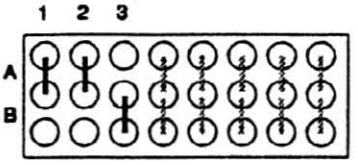
This jumper serves multiple purposes. First of all, you can choose different link speed settings, therefore the first three columns of the jumperbank are reserved. The T800/805 links support the standard operating speed of 10 Mbit/s, but also operate at 5 or 20 Mbit/s. The definite jumper settings are listed below. Secondly the columns 4, 5 and 6 are used to determine the processor speed via the transputer clock. For exact jumper settings see next page. Last of all the memory access time is also adjustable. Please see next page.

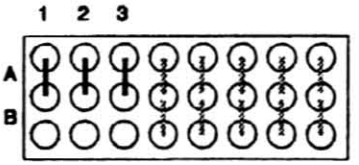
Scheme :

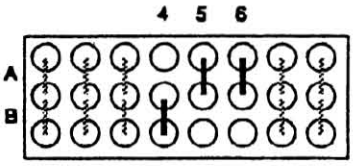
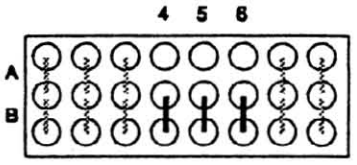
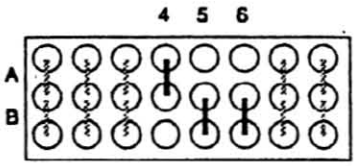
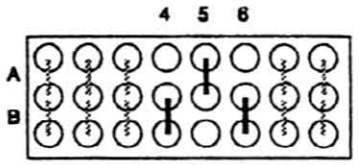
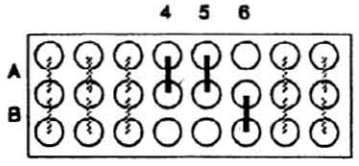
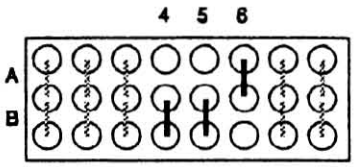


Details :

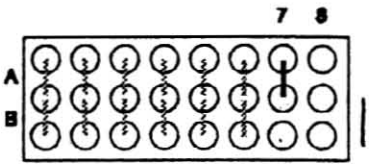
Link speed		jumpers set	
Link 0 Link 1, 2, 3	10 Mbit/s 10 Mbit/s	1B, 2B, 3B	
Link 0 Link 1, 2, 3	10 Mbit/s 5 Mbit/s	1B, 2B, 3A	
Link 0 Link 1, 2, 3	5 Mbit/s 10 Mbit/s	1B, 2A, 3B	
Link 0 Link 1, 2, 3	5 Mbit/s 5 Mbit/s	1B, 2A, 3A	
Link 0 Link 1, 2, 3	10 Mbit/s 20 Mbit/s	1A, 2B, 3A	

Link 0	20 Mbit/s	1A, 2A, 3B	
Link 1, 2, 3	10 Mbit/s		

Link 0	20 Mbit/s	1A, 2A, 3A	
Link 1, 2, 3	20 Mbit/s		

Transputer clock		jumpers set	
T800	17.5 MHz	4B, 5A, 6A	
T800	20 MHz	4B, 5B, 6B	
T800	22.5 MHz	4A, 5B, 6B	
T800	25 MHz	4B, 5A, 6B	
T800	30 MHz	4A, 5A, 6B	
T800	35 MHz	4B, 5B, 6A	

Transputer clock	Memory access time	jumpers set
17.5 MHz	80 ns	7A
17.5 MHz	100 ns	7B
20 MHz	80 ns	7A
20 MHz	100 ns	7B
25 MHZ	60 ns	7A
25 MHz	80 ns	7B
25 MHz	100 ns	8A
30 MHz	70 ns	7B ✓
30 MHz	80 ns	8A
30 MHz	100 ns	8B



7B ✓

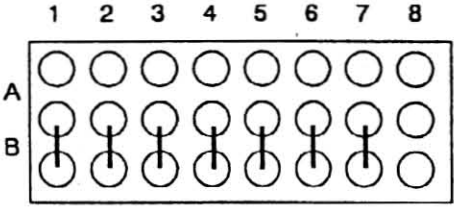
/

30MHz ⊕ 70ns Mem. ✓

✗ **example setting :**

- speed of 10 Mbit/s on links 0 to 3

- T800 20 MHz, 100ns memory access time



2.2.4 J14, J24 : Internal use

Note: This jumper is for internal use only.

Do not change the setting!

2.3 Hardware Addresses

Address space of the T800

Hardware Addresses		Addresses in present OCCAM-2-Implementation PLACEment as word address
0000 00C0	Reset	#2000 0030
0000 0080	Status	#2000 0020
0000 0040		#2000 0010
0000 0000	Identification-PAL (optional)	#2000 0000
807F FFFF	8 MByte memory	#001F FFFF
803F FFFF	4 MByte memory	#000F FFFF
801F FFFF		#0007 FFFF
...	2 MByte main memory	...
8000 0000		#0000 0000

The identification-PAL makes it possible for the user to give every board an identification up to 7 bytes long. These bytes appear in the least significant byte of the following occam addresses :

#20000000	Byte 1
#20000001	Byte 2
#20000002	Byte 3
#20000003	Byte 4
#20000004	Byte 5
#20000005	Byte 6
#20000006	Byte 7

2.4 Allocation of the DIN Connector

Pin-out of 96-way DIN connector:

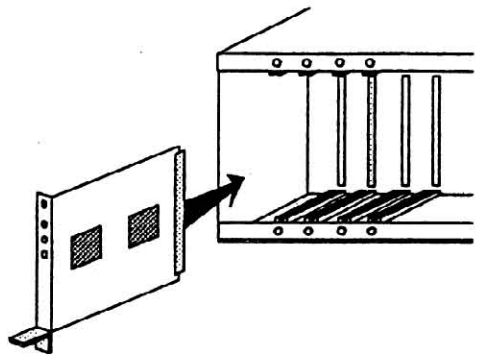
	a	b	c
1	Reset 0 out +	Reset 1 out +	Reset 0 out -
2	Link 0 out +	Reset 1 out -	Link 0 out -
3	GND	Link 1 out +	GND
4	Link 0 in -	Link 1 out -	Link 0 in +
5	Reset 0 in -	Link 1 in -	Reset 0 in +
6	Link 1 in +	Reset 1 in -	Reset 1 in +
7	Reset 2 out +	Reset 3 out +	Reset 2 out -
8	Link 2 out +	Reset 3 out -	Link 2 out -
9	GND	Link 3 out +	GND
10	Link 2 in -	Link 3 out -	Link 2 in +
11	Reset 2 in -	Link 3 in -	Reset 2 in +
12	Link 3 in +	Reset 3 in -	Reset 3 in +
13	Reset 4 out +	Reset 5 out +	Reset 4 out -
14	Link 4 out +	Reset 5 out -	Link 4 out -
15	GND	Link 5 out +	GND
16	Link 4 in -	Link 5 out -	Link 4 in +
17	Reset 4 in -	Link 5 in -	Reset 4 in +
18	Link 5 in +	Reset 5 in -	Reset 5 in +
19	Reset 6 out +	Reset 7 out +	Reset 6 out -
20	Link 6 out +	Reset 7 out -	Link 6 out -
21	GND	Link 7 out +	GND
22	Link 6 in -	Link 7 out -	Link 6 in +
23	Reset 6 in -	Link 7 in -	Reset 6 in +
24	Link 7 in +	Reset 7 in +	Master Reset
25		Reset 7 in -	
26			
27	+ 5V	+ 5V	+ 5V
28	+ 5V	+ 5V	+ 5V
29	+ 5V	+ 5V	+ 5V
30	GND	GND	GND
31	GND	GND	GND
32	GND	GND	GND

2.5 Installation of the board

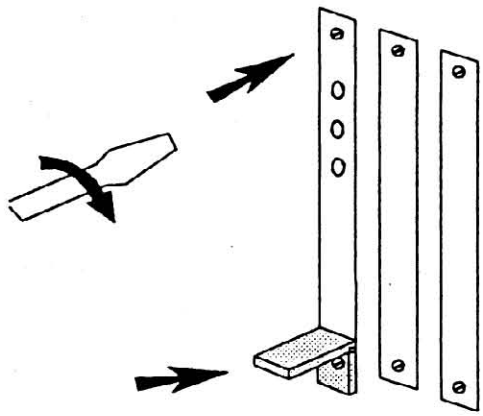
The installation of the MTM-2-11/12/13 is very easy as shown in the figure below. You can plug it into a MultiCluster 1,2,3 or SuperCluster or a PC (only in connection with a BBK-PC)

Fig. 2-3: *Installation*

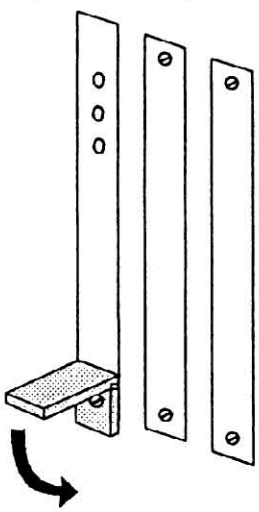
- ❑ Push the board into the case
  until the backplane connectors snap in.



- ❑ For a firm hold fix the screws
  with a screwdriver.



- ❑ To eject the board
  use the bottom ejector.



3. Links

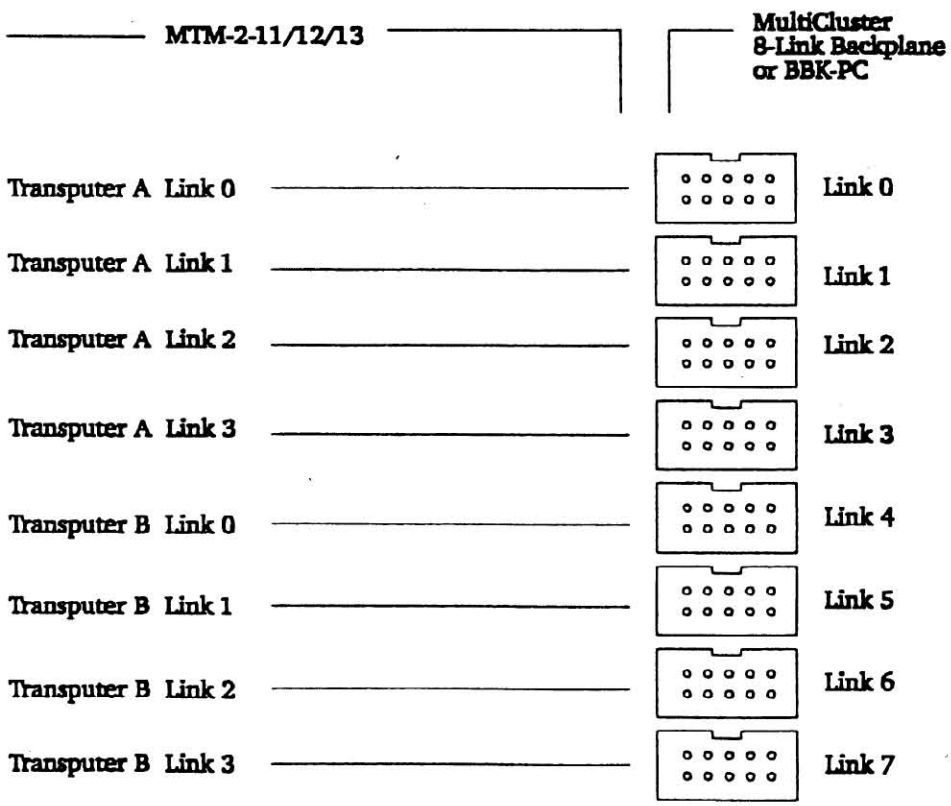
Four identical bi-directional serial links provide synchronized communication between processors and with the rest of the world. Each link comprises an input channel and output channel. A link between two transputers is implemented by connecting a link interface on one transputer to a link interface on the other transputer. Every byte of data sent on a link is acknowledged on the input of the same link, thus each signal line carries both data and control information.

Link 0 to link 3 of each transputer are taken via the RS-422 buffers directly on to the VG connector. They can be adjusted to 20, 10 or 5 Mbit/s depending on the distance of the connection. Please refer to chapter 2.2.3.

Each link offers a reset connection facility, which supports program controlled resetting of neighbour transputers in both directions. This enables each transputer to reset and reboot its neighbours, e.g. after a software malfunction has been detected.

In the figure below you can see the link connectors of the two transputer sections as they are in a MultiCluster 8-Link-Backplane or a BBK-PC (boards connected via the 96-way DIN connector).

Fig 3-1: *MultiCluster 8-Link Backplane and BBK-PC*



4. Software Description

4.1 Error and Analyse

In the event of errors, the MTM-2-11/12/13 offers the possibility of a systematic shut-down of all processes. In principle, only two types of errors can occur: Program- and address errors. Program errors, such as a division by 0, integer overflow or array boundary violation are signalled by the transputer with setting of the error flag. An external address decoding identifies the exceeding of the on board RAM and sets a bit in status PAL.

According to the jumper selection an error condition will initiate either an interrupt, or do nothing. The analyse condition starts a controlled shut-down of all active processes and the system can be externally analysed after reset and loaded anew. The error condition can also be read-out and analysed. The interrupt activates a service routine in which the user can determine the further process.

The addresses of the status-PAL are listed above. The bits 0 and 1 have the following meaning when set (active low):

Bit 0 = 0 : Transputer error

Bit 1 = 0 : Address error

4.2 Software Controlled Reset

A reset line is lead parallel to every link which sets the addressed transputer in boot-condition. That provides the possibility to supervise the activities of the next four neighbouring transputers and executes a systematic reset in the event of an error. Afterwards they can be provided with a new program code via the links and can be started anew.

The following occam program demonstrates the required sequence, to generate a reset from one Transputer to its connected neighbour via a UniLink:

```
PROC reset (VAL INT link.number)
    INT addr.reset, time :
    PLACE addr.reset AT #20000030 :     -- reset PAL address for T4/T8
    --PLACE addr.reset AT #7FFF    :     -- reset PAL address for T2
    TIMER clock :
    VAL INT wait IS 2 :                 -- 2 times 64 microseconds
    SEQ
      addr.reset := 0                   -- sequence to unlock the
      addr.reset := 1                   -- reset logic
      addr.reset := 2
      addr.reset := 3
      addr.reset := (1 << link.number) -- code for link to be reset
      clock ? time
      clock ? AFTER time PLUS wait      -- wait 128 microseconds
      addr.reset := 0                   -- deassert reset signal
:
```

Written in C a reset procedure looks like:

```
void reset (int link)
 {
   int *reset_addr = (int *)0x000000C0;/* T8 address of reset PAL */
   /*int *reset_addr = (int *)0x7FFE;*//* T2 address of reset PAL */
   *reset_addr = 0;                    /* sequence to unlock the
   *reset_addr = 1;                    /* reset PAL */
   *reset_addr = 2;
   *reset_addr = 3;
   *reset_addr = (1<<link);            /* assert reset signal */
   delay (128);                        /* wait 128 us */
   *reset_addr = 0;                    /* deassert reset signal */
 }
```

The following will be performed at the Transputer board connected to the link:

1. Reset comes into the board

2. Analyse-signal is generated by the board logic and given to the Transputer

3. Reset-signal is then guided also to the Transputer

4. Current active process is descheduled

5. Resetting under "Analyse-condition" is initiated

4.3 Bootstrap

A bootstrap is the code sequence used to initialize a processor after a hardware reset.

The program which is executed after reset can either reside in ROM in the transputer's address space or it can be loaded via any one of the links.

Each processor of the MTM-2-11/12/13 is configured by default to BootFromLink, i.e. after reset the processor expects the program as a data stream from a link. In this state all 4 Links have equal priorities.

When a transputer is in a reset state, the first message that comes via one of those links is interpreted as a boot program and executed accordingly. The first byte of the message is the count of the number of bytes of program which follow. The program is loaded into memory starting at a product dependent location MemStart, and then control is transferred to this address.

Messages subsequently arriving on other links are not acknowledged until the transputer processor obeys a process which inputs from them. The loading of a network of transputers is controlled by the transputer development system, which ensures that the first message each transputer receives is the bootstrap program.

5. Board Specifications

Note: This empty chapter is included to obtain an identical structure in all hardware manuals!

6. Technical Data

6.1 Operating Conditions

Power Supply

Voltage:	5V, +/- 5%	
Current:	- operating mode	3,7 A max. peak current
	- non-operating mode	2 A
Power consumption:	15W	

Temperature

Operating mode:		0 to +70 °C
	Gradient	20 °C per hour
Non-operating mode:		-20 to +125 °C
	Gradient	20 °C per hour

Humidity

Operating mode:		20% to 80% RH non-condensing
	Gradient	30% per hour
Non-operating mode:		95% RH non-condensing
	Gradient	30% per hour

Appendix A

Short Reference

This page gives you a short summary of what to do with the board after unpacking it.

The MTM-2 board can be plugged into a MultiCluster-1, -2, -3, a SuperCluster or a PC (the latter is only possible in combination with a BBK-PC).

Please check the correct jumpering before the installation. The only items which can be changed on the board are the following jumper settings:

- Jumpers J10 / J20
  These jumpers control the settings for the Event resp. Analyse generation. The default setting is 2A (Event signal generation on address error) and 4A (Analyse signal generation for all incoming reset signals).
  The other two columns are not to be changed!

- Jumpers J11 / J21
  These jumpers control the different hardware speed settings.
  Use columns 1 to 3 to set the link speed, columns 4 to 6 to set the transputer clock and columns 7 and 8 to set the memory access time. The default setting is 1A, 2A and 3A for the link speed. The other columns have no default because the setting depends on the mounted chips.

- Jumpers J14 / 24
  Do not change!

If you want to change the default settings, refer to chapter 2.2 for detailed information.

Please check if the board has snapped correctly into the backplane connectors. After switching on the power the red LED (+5V) at the board front panel should light up.

Glossary

- *Analyse*
  Signal Input at the Transputer.
  Active Input stops the Transputer normal program access and saves all internal registers.

- *Identification PAL*
  This special logic device implements seven read-only registers to enable software recognition of the specific Transputer Mode.

- *Link*
  Serial communication channel between Transputers.

- *Mips*
  Million instructions per second.

- *OCCAM2*
  Present implementation of the OCCAM programming language for concurrent processing.

- *PAL*
  Programmable Array Logic.

- *Reset*
  A signal to bring logic as well as the Transputer into a well defined state after powering up and better rebooting.

- *Status PAL*
  This specific logic device implements read-only registers to identify the source of an error.

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