parsytec

TIP - MFG

Monochrome Frame Grabber

Technische Dokumentation
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0. Inhaltsverzeichnis

2.   Hardware Beschreibung

Die Hardware des TIP-MFG stellt die visuelle Eingangs-Schnittstelle des Parsytec TIP-Systems zwischen Außenwelt und Rechner-System dar. Um den Anschluß nahezu aller Kamera-Typen am MFG sicherzustellen, ist das MFG mit einer sehr leistungsfähigen und vielfältig einstellbaren Takt- und Video-Timing-Einheit ausgestattet. Alle Parameter in diesem Bereich können mit Software eingestellt werden, eine Jumper-Sektion gibt es nur für den Transputer-Knoten.

Das MFG verfügt auf der Frontplatte über 4 Kamera-Eingänge auf 2 Steckern und 2 TIP-Bus Anschlüssen. Abtastraten bis 18 MHz (8 Bit) werden unterstützt, CCD-Flächen- und Zeilen-Kameras sowie Video-Recorder können angeschlossen werden. Zur Daten-Vorverarbeitung und für die Steuerung der Kameras wird ein Transputer T805 eingesetzt. Er übernimmt gleichzeitig die Initialisierung des TIP-Bus Controllers.

2.1   Funktionsprinzip des MFG

Das TIP-MFG Board gliedert sich in drei Sektionen: die Prozessor-Sektion mit dem T805 und dem Hauptspeicher, die TIP-Bus-Sektion für den schnellen Datentransfer zu anderen TIP Modulen und schließlich die Digitizer-Sektion, die beim MFG für die Aufnahme von Video-Daten verantwortlich ist. 2 MByte Video-RAM sind auf einer Aufsteckplatine untergebracht. [-> Bild Übersicht MFG]

Auf der Frontseite des MFG befinden sich vier flexibel konfigurierbare Video-Anschlüsse, die über einen Multiplexer auf den Flash A/D-Wandler Bt251 geschaltet werden. Optional kann das ausgewählte Video-Signal mit einem Anti-Aliasing-Filter bandbegrenzt werden. Das A/D-Ergebnis adressiert eine Lookup-Table und erlaubt so eine nichtlineare Grauwert-Umsetzung. Die digitalisierten Video-Daten gelangen anschliessend über einen FIFO und einen Umsetzer 8 auf 32 Bit auf den seriellen Eingang des Video-RAMs. Auf das Video-RAM kann außerdem der Transputer und das TIP-Bus Interface zugreifen, sodaß die Video-Daten dem gesamten TIP-System zur Verfügung stehen. Aufgabe des FIFO ist es bis zu 2048 Pixel einer Bildzeile zwischenzuspeichern, falls die höherpriorisierte Buslogik gleichzeitig auf das VRAM zugreift.

Das MFG erlaubt grundsätzlich zwei verschiedene Betriebsmodi. Im Slave-Mode liefert die Videoquelle die Synchronisations-Signale, die Pixelclock wird dabei auf dem MFG erzeugt, kann aber ebenfalls von außen bereitgestellt werden. In diesem Modus ist es zusätzliche Aufgabe des Bt251 aus dem anliegenden Videosignal die Synchronisations-Signale herauszufiltern um sie dem sogenannten 'Sync Stripper' Bt261 zur Verfügung zu stellen.

Im Master-Mode generiert das MFG alle von der Video-Quelle benötigten Signale zur Synchronisation - steuert also die Kamera. Zu diesem Zweck stehen ein Pixelclock Generator (ICS 1394) und ein Video Timing Generator (LM 1882) zur Verfügung. Da beide Bausteine programmierbar sind, sind sowohl die Pixel-Clock als auch die Synchronisations-Signale HSYNC und VSYNC sehr fein justierbar.

Der Baustein Bt261 erzeugt aus den extern oder intern generierten Synchronisations-Signalen und der Pixel-Clock die Steuersignale für den A/D-Wandler Bt251 und die Kontroll-Logik.

Blockschaltbild TIP-MFG
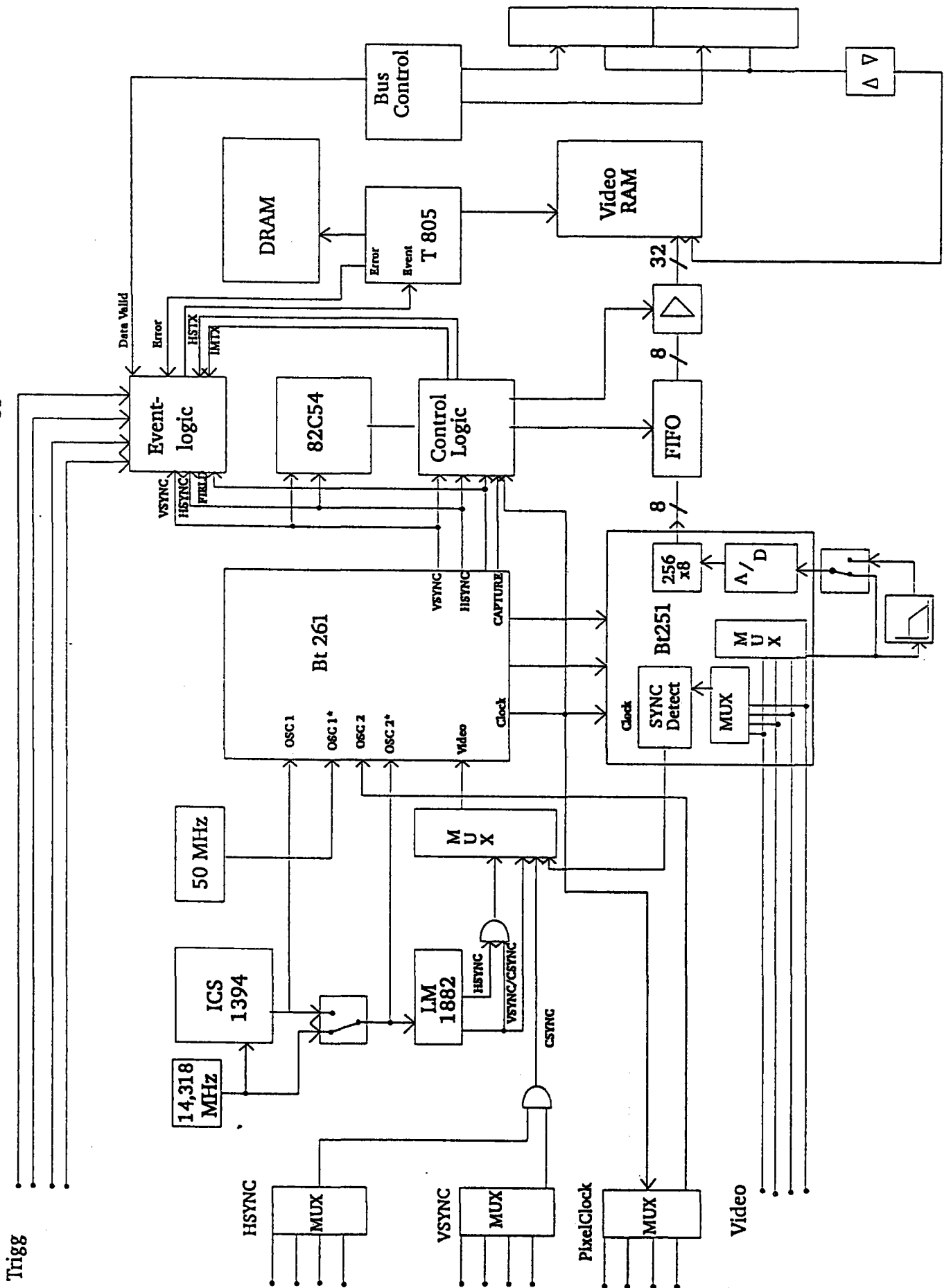
2.2 Transputer Sektion

2.2.1 Der Transputer-Knoten

Die Transputer-Sektion besteht beim TIP-MFG aus einem T805 Transputer, welcher mit 30 MHz getaktet wird. Desweiteren sind 4 MByte dynamischer Arbeitsspeicher (DRAM) vorhanden, sowie weitere 2 MByte Videospeicher (VRAM). Beide RAM-Bereiche, sowie alle Controller auf dem Board sind vom Transputer aus direkt zugreifbar (memory mapped layout).

Zur Einstellung der Taktrate und der Zyklen für den Zugriff auf das DRAM befinden sich einige Jumper auf dem Board.

2.2.2 Transputer Links

Eine Transputer-Link besteht aus Datenleitungen für die Eingangs- und Ausgangsrichtung. Durch Verbinden von jeweils Datenausgang mit Dateneingang lassen sich beliebig große Netzwerke verschalten. In einer Parsytec UniLink Verbindung findet man neben den Datenleitungen auch Reset-Leitungen für beide Richtungen, zudem werden alle Signale differentiell mit RS422-Pegel übertragen.

Diese zusätzlichen Reset-Verbindungen erlauben es, einen Transputer jeweils über einen Link von einem Nachbar-Transputer zurückzusetzen. Dieser Mechanismus kann von jedem Parsytec-Transputermodul über das sogenannte Reset-Register (Adresse $000000C0) ausgelöst werden. Die erforderliche Programmsequenz um den an Link 'link' angeschlossenen Transputer zurückzusetzen, sieht folgendermaßen aus:

```
#define RESET_REGISTER   0x000000C0

ResetLink (int link)              /* valid link numbers are 0...3 */
{
  *RESET_REGISTER = 0;
  *RESET_REGISTER = 1;
  *RESET_REGISTER = 2;
  *RESET_REGISTER = 3;
  *RESET_REGISTER = 1<<link;
  wait(128);                                    /* wait for 128 us */
  *RESET_REGISTER = 0;
}
```

Auf dem MFG werden alle vier Links des T805 Transputers als UniLinks auf die VG-Leiste geführt, daß heißt z.B. über ein Parsytec Backplane-Element läßt sich jeder einzelne Link beliebig mit anderen Transputermodulen zu Netzwerken verbinden. Im Anhang ist die genaue Belegung der VG-Leiste sowie die korrespondierende Belegung der Berg-Stecker bei benutzung der Backplane aufgeführt.

2.2.3 Event-Logik

Jeder Transputer besitzt einen Event-Eingang, der es erlaubt, ähnlich einem Interrupt, auf externe Ereignisse unmittelbar zu reagieren. Auf dem MFG befinden sich insgesamt 13 unterschiedliche Event-Quellen verteilt aufverschiedene Sektionen des Boards. Zu diesen Eventquellen gehören die Trigger-Eingänge der Kamera-Ports, Synchronisations-Signale aus der Digitizer-Sektion, Ablaufsignale aus der Bus-Sektion, sowie die Error-Leitung des Transputers.

Die Verwaltung der möglichen Events, daß heißt zum Beispiel die gezielte Auswahl von Ereignissen, wird über die sogenannte Event-Logik realisiert. Teil dieser Event-Logik ist das Event-Register, über das festgelegt wird, welche Ereignisse ein Event auslösen dürfen, bzw. mit dessen Hilfe ermittelt werden kann, welches Ereignis nun tatsächlich eingetreten ist. Jeder Event-Quelle ist ein Bit im Event-Register zugeordnet.

Mit einem Schreibzugriff auf das Event-Register kann eine beliebige Bit-Maske gesetzt werden. Dabei bedeutet eine logische 1 in der Maske, daß das zugeordnete Ereignis ein Event auslösen darf. Im Falle eines Events kann durch Lesen des Event-Registers die Quelle festgestellt werden, welche zur Auslösung geführt hat.

Die folgende Tabelle zeigt die Zuordnung der Event-Quellen zu den Bits im Event-Register:

Bit	Signal
0	Transputer Error Leitung
1	Real-Time Synchron Channel (RTSC) 0
2	Real-Time Synchron Channel (RTSC) 2
3	Trigger von Kamera-Port 0
4	Trigger von Kamera-Port 1
5	Trigger von Kamera-Port 2
6	Trigger von Kamera-Port 3
7	HSYNC-Ausgang vom Bt261
8	VSYNC-Ausgang vom Bt261
9	Ende einer Bildzeile
10	Ende eines (Halb-)Bildes
11	Field-Bit des Bt261
12	Data Valid Signal vom TIP-Bus

Das Event-Register sowie der Event-Kanal des Transputers befinden sich auf folgenden Wortadressen:

Event-Adresslage		'C' Definition
$000001C0 r/w	MFG-Event Register	EVENT_REGISTER
$80000020	Event-Channel	EVENT *)

*)   Dieses Symbol ist i.A. implementierungabhängig, die angegebene Definition gilt in dieser Form für das Inmos Toolset.

2.3 Digitizer Sektion

In der Digitizer Sektion lassen sich fünf programmierbare Bausteine (Bt251, Bt261, LM1882, ICS1394, 82c54) sowie die vier konfigurierbaren Video-Ports und einige Signal-Multiplexer zusammenfassen. Die nachfolgenden Kapitel stellen diese Komponenten und ihre Programmierung im Einzelnen vor.

2.3.1 Der Flash A/D-Wandler Bt251

2.3.1.1 Funktionsbeschreibung

Der Bt251 von Brooktree hat die Aufgabe, die Video-Daten zu digitalisieren, dabei kann über einen eingebauten Multiplexer einer von vier Video-Kanälen selektiert werden. Die Eingangsimpedanz beträgt in allen Fällen 75 Ohm. Die zweite Aufgabe des Bausteins ist es, aus dem Video-Signal ein Composite-Sync-Signal zu detektieren, um dieses im Slave-Mode dem Bt261 zuzuführen. Der Bt251 kann selbst kein Video-Timing verarbeiten, sondern agiert nur in Abhängigkeit der Pixelclock, Zero- und Clamp-Signale des Bt261.

Die Abtastung des Video-Signals erfolgt mit maximal 18 MSPS bei 8 Bit Auflösung. Das Ergebnis adressiert ein 256*8 Look-Up-Table (LUT), womit eine Echtzeit-Bildmanipulation ermöglicht wird, z.B. Schwellwert-Erkennung, Kontrast-Verstärkung, Bildinvertierung oder nichtlineare Grauwert-Zuordnung. Die zur A/D-Umsetzung benötigten Referenzspannungen REF+ und REF- lassen sich mittels zweier 6-bit DAC's von 0 bis 1,2 Volt in 19 mV-Schritten einstellen (siehe unten). Ein Null-Abgleich (Schwarzwert) kann durchgeführt werden.

Der Bt251 sieht eine Bandbegrenzung des Video-Signales auf den Nutzfrequenzbereich mit einem Antialiasing-Filter vor. Dieses Filter ist bei Auslieferung standardmäßig überbrückt. Um das Filter zu aktivieren, müssen auf der Platine einige Komponenten umgelötet werden. Zum Betrieb des Filters ist eine Versorgungs-Spannung von +/- 12 Volt notwendig.

2.3.1.2 Programmierung

Die Programmierung des Bt251 erfolgt über drei 8-Bit Register (Siehe auch Technische Beschreibung zum Bt251 im Anhang). Es sind sowohl Schreib- als auch Lesezugriffe erlaubt. Die Register befinden sich auf folgenden Wortadressen:

BT 251 Adress-Lage			'C' Definition
$00000580	r/w	Adress-Register	ADDR_REG_251
$00000584	r/w	LUT-RAM Register	RAM_LOC
$00000588	r/w	Kontroll-Register	COMMAND_REG

Bei jedem Zugriff auf die Bt251 Register wird zunächst in das Adress-Register geschrieben, anschliessend kann entweder auf das LUT-RAM Register oder das Kontroll-Register zugegriffen werden. Der Inhalt des Adress-Registers legt somit fest auf welche Position des LUT-RAM (0-255), oder auf welches der folgenden drei Kontrollregister der Zugriff erfolgt:

Adress-Reg.	selektiert wird	'C' Definition
xxxx xx00	Command Register	BT251_COMM_REG
xxxx xx01	IOUT0 Data Register -> REF+	BT251_IOUT0_DATA
xxxx xx10	IOUT1 Data Register -> REF-	BT251_IOUT1_DATA

Das **Command Register** vereinigt grundsätzliche Einstellungen des Bt251 in Bezug auf die Auswahl der Videoeingänge und des Schwellwertes zur Erkennung von Synchronisation-Impulsen. Die folgende Übersicht verdeutlicht die Zusammenhänge:

BT 251 Command Register		'C' Definition
Bit 7,6	legen fest welches der vier Video-Eingangssignale digitalisiert wird.	
00	Video 0	(VID0_SEL)
01	Video 1	(VID1_SEL)
10	Video 2	(VID2_SEL)
11	Video 3	(VID3_SEL)
Bit 5,4	legen fest welches der vier Video-Eingangssignale zur Detektion von Synchron-Impulsen dient.	
00	Video 0	(VID0_SYNC)
01	Video 1	(VID1_SYNC)
10	Video 2	(VID2_SYNC)
11	Video 3	(VID3_SYNC)
Bit 3,2	Festlegung des Schwellwertes für die Erkennung der Synchron-Impulse.	
00	50 mV	(SYNC_LEVEL_0)
01	75 mV	(SYNC_LEVEL_1)
10	100 mV	(SYNC_LEVEL_2)
11	125 mV	(SYNC_LEVEL_3)
Bit 1,0	reserviert (müssen logisch 0 sein!)	

Über zwei Referenzspannungen wird der Arbeitsbereich des A/D-Wandlers festgelegt und damit die erzielbare Dynamik. Die **IOUT-Data-Register** des Bt251 ermöglichen die Kontrolle dieser Referenzspannungen und damit eine den jeweiligen Bedingungen optimal angepaßte A/D-Wandlereinheit. Der Bereich zwischen der unteren (REF-) und der oberen (REF+) Vergleichsspannung wird vom Wandler in 256 Abschnitte unterteilt, sodaß ein direkte 'Einordnung' der Video-Eingangsspannung den Resultatwert liefert. Eingangsspannungen unterhalb der unteren Referenzspannung liefern den Wert $00, Spannungen oberhalb der oberen Referenz liefern $FF.
Die Programmierung der Referenzsspannungen geschieht über die höherwertigen 6 Bit der beiden IOUT Data Register, die beiden unteren Bit müssen logisch 0 sein. Das IOUT0-Register stellt die obere (REF+) Vergleichsspannung ein, IOUT1 die untere (REF-). Den Zusammenhang zwischen dem Inhalt der IOUT Data Register und den Spannungen REF+ und REF-zeigt folgende Tabelle:

BT 251 IOUT Data Register	
IOUT Data	REF+/REF-
0000 0000	0 mV
0000 0100	19 mV
0000 1000	38 mV
:	:
1111 1100	1.2 V

Für eine grobe Einstellung sollte man für die untere Referenzspannung den 250 mV vorgeben und für die obere 1 V.

2.3.2 Der HSYNC Line Lock Controller Bt261

2.3.2.1 Funktionsbeschreibung

Die Aufgabe des Brooktree Bt261 ist die Erzeugung der Steuersignale für den Bt251 und die Kontroll-Logik. Als Basis dient ein Oszillator-Signal für die Pixelclock und das Composite-Sync-Signal, welches vom Bt251 aus dem Videosignal gefiltert oder vom LM1882 generiert wurde. Weiterhin kann auch ein extern angelegtes Composite-Sync-Signal durchgeschaltet werden. Die Auswahl erfolgt über einen vorgeschalteten Multiplexer (CSYNC-Mux).

Zunächst wird das Composite-Sync-Signal zerlegt nach vertikaler und horizontaler Synchron-Information. Das Vertikal-Synchron-Signal (VSYNC) und das Field-Signal (FIELD) gelangen unmittelbar zur nachfolgenden Kontroll-Logik. Das FIELD-Signal liefert im Interlaced-Modus die Information, welches Teilbild gerade digitalisiert wird.

Das Horizontal-Synchron-Signal (HSYNC) gelangt über eine Filterstufe zur Unterdrückung von Zwischenimpulsen (Noise Gate) zur Takterzeugungseinheit und triggert dort den 12-bit Zähler für das horizontale Timing (HCOUNT). In Abhängigkeit dieses Zählers lassen sich alle jeweils eine Bildzeile betreffenden Signale mit 12-bit Genauigkeit einstellen.

Auf dem MFG werden die Oszillator-Eingänge des Bt261 im TTL-Modus betrieben, sodaß insgesamt vier verschiedene Quellen für die Pixelclock zur Verfügung stehen. Dies sind der programmierbare Pixelclock Generator ICS 1394, die 50 MHz Bus-Clock, der 14.318 MHz Quarz-Oszillator oder ein externes Signal auf einem der Pixelclock-Eingängen der Kameraports. Dabei ist zu beachten, daß eine höhere Oszillator-Frequenz einen geringeren Pixelclock-Jitter zur Folge hat, da der Eingangs-Takt die Auflösung vorgibt, nach der die Pixelclock einrasten kann.

2.3.2.2 Programmierung

Der Bt261 verfügt über eine Rechnerschnittstelle, die das Einstellen der Betriebs-Modi, die Auswahl des Eingangs-Oszillators und die komplette Programmierung des Timings erlaubt. Über je ein Adress- und ein Kontroll-Register können vom Prozessor alle Einstellungen vorgenommen werden. Diese Register befinden sich auf folgenden Wortadressen:

BT 261 Adress-Lage			'C' Definition
$000005C0	r/w	Adress-Register	ADDR_REG_261
$000005C4	r/w	Kontroll-Register	CONTROL_REG_261

Über das Adress-Register lassen sich 30 interne 8-bit Register auswählen, von Registernummer 8 an aufwärts bilden jeweils zwei Register zusammengenommen einen 12-bit breiten Wert. Beim Schreibzugriff auf diese Registerpaare is zu beachten, daß Daten erst mit dem Schreibzugriff auf das jeweilige High-Byte Register übernommen werden. Alle Register erlauben sowohl Schreib- als auch Lesezugriffe, Ausnahme ist das Status-Register, welches nur gelesen werden kann.

BT 261 Interne Register		
Nummer	Bedeutung	'C' Definition
$00	Command Register 0	BT261_COMM_REG_0
$01	Command Register 1	BT261_COMM_REG_1
$02	Command Register 2	BT261_COMM_REG_2
$03	Command Register 3	BT261_COMM_REG_3
$04	VSYNC Sample Register	BT261_VSYNC_SAMPLE
$05	OSC Count Low Register	BT261_OSC_COUNT_LOW
$06	OSC Count High Register	BT261_OSC_COUNT_HIGH
$07	Status Register (read only!)	BT261_STATUS
$08,09	HSYNC Start Register [lo/hi]	BT261_HSYNC_START
$0A,0B	HSYNC Stop Register [lo/hi]	BT261_HSYNC_STOP
$0C,0D	CLAMP Start Register [lo/hi]	BT261_CLAMP_START
$0E,0F	CLAMP Stop Register [lo/hi]	BT261_CLAMP_STOP
$10,11	ZERO Start Register [lo/hi]	BT261_ZERO_START
$12,13	ZERO Stop Register [lo/hi]	BT261_ZERO_STOP
$14,15	FIELD Gate Start Reg.[lo/hi]	BT261_FIELD_GATE_START
$16,17	FIELD Gate Stop Reg. [lo/hi]	BT261_FIELD_GATE_STOP
$18,19	NOISE Gate Start Reg.[lo/hi]	BT261_NOISE_GATE_START
$1A,1B	NOISE Gate Stop Reg. [lo/hi]	BT261_NOISE_GATE_STOP
$1C,1D	HCOUNT Register [lo/hi]	BT261_HCOUNT
$1E,1F	reserviert	

An dieser Stelle erfolgt eine knappe Darstellung der Bedeutung einzelner Register, die genaue Funktion aller internen Register ist der Beschreibung des Bt261 im Anhang zu entnehmen.

Command Register 0 legt unter anderem fest, welcher Oszillator-Eingang benutzt wird. Mit Command Register 1 wird zwischen Interlaced und Non-Interlaced Modus unterschieden. Die Quelle für die im Bt261 benutzte Pixelclock wird über Command Register 2 ausgewählt.

Die Register 5 und 6 (OSC Count Low/High Register) legen das Verhältnis fest mit dem der Oszillator-Takt auf die Pixelclock heruntergeteilt wird.

Die HSYNC Start/Stop Register beeinflussen die Dauer von Frontporch/Backporch, legen also u.a. fest, ab wann das eigentliche Video-Information in der Zeile beginnt. Das HCOUNT Register legt die Gesamtzahl von Pixeln in einer Zeile fest.

Die Field Gate Start/Stop Register definieren ein Fenster in einer Videozeile, um den halbzeilig verschoben horizontalen Takt beim Übergang vom zweiten zum ersten Halbbild zu detektieren. Das Field Signal liefert somit die Information, welches Halbbild gerade digitalisiert wird.

In ähnlicher Weise definieren die Noise Gate Start/Stop Register ein Fenster um eventuell vorhandene Ausgleichs-Impulse (Equalization/Serration Pulses) zu unterdrücken.

2.3.3   Der Pixel Clock Generator ICS 1394

Der ICS 1394 ist ein Video Dot Clock Generator, der aus der Grundfrequenz 14.31818 MHz verschiedene Video Pixel Clocks für die Anwendung erzeugen kann. In einem Chip-internen ROM sind 32 Video-Frequenz-Verhältnisse in Bezug auf die Grundfrequenz vorbelegt, die über folgende Adresse selektiert werden können.

ICS 1394 Adress-Lage		'C' Definition
$00000480 /w	I1394 ROM-Tabelle	I1394

Die Auswahl einer bestimmten Frequenz geschieht durch einen Schreibvorgang auf die angegebene Adresse, dabei sind nur die unteren 5 Bit relevant. Es ist nicht möglich das I1394 Register auszulesen. Die einstellbaren Video-Frequenzen (in MHz) sind der folgenden Tabelle zu entnehmen:

ICS 1394-030 ROM-Adress-Belegung							
0	14.318	8	14.318	16	14.318	24	44.900
1	16.257	9	16.257	17	65.028	25	50.344
2	not used	10	not used	18	not used	26	16.257
3	32.514	11	36.000	19	36.000	27	32.514
4	25.175	12	25.175	20	25.175	28	56.644
5	28.332	13	28.332	21	28.332	29	20.000
6	24.000	14	24.000	22	24.000	30	50.000
7	40.000	15	40.000	23	40.000	31	80.000

Anmerkung: Eine höhere Pixel-Clock ergibt im Slave-Modus einen geringeren Bildzeilenjitter für die Bildaufnahme.

2.3.4   Der Video Timing-Generator LM 1882

2.3.4.1   Funktionsbeschreibung

Mit Hilfe des Bausteins LM 1882 auf dem MFG, kann ein komplettes Video Timing (HSYNC, VSYNC, CSYNC) intern erzeugt werden. Entsprechende Signale werden gebraucht falls die angeschlossene Kamera diese Signale nicht liefern kann oder soll. Als Basis dient ein Takt-Signal, welches entweder ein 14.318 MHz Quarz-Oszillator liefert, oder der programmierbare Pixelclock-Generator ICS 1394.

Die Pulsbreiten können vom Anwender programmiert werden, sodaß ein sehr flexibles Video-Timing erzeugt werden kann. Der LM1882 unterstützt Interlaced und non-Interlaced Betriebsmodi. Intern besteht der LM 1882 aus programmierbaren 12 Bit Registern. Aus dem Vergleich zwischen den Register-Inhalten mit Zählern für die horizontalen und vertikalen Bildimpulse wird das Video-Timing generiert. Der genaue Zusammenhang zwischen Register-Inhalten und den Synchronisations-Impulsen zeigen die Abbildungen im Datenblatt des LM 1882 im Anhang.

2.3.4.2   Programmierung

Die folgende Tabelle gibt zunächst einen Überblick über die im LM1882 vorhandenen Register:

LM 1882 Registers	
0	Status Register
Horizontal Interval Registers	
1	Horizontal Front Porch
2	Horizontal Sync Pulse End Time
3	Horizontal Blanking Width
4	Horizontal Interval Width
Vertical Interval Registers	
5	Vertical Front Porch
6	Vertical Sync Pulse End Time
7	Vertical Blanking Width
8	Vertical Interval Width
Equalization and Serration Pulse Specification Registers	
9	Equalization Pulse Width Time
10	Serration Pulse Width Time
11	Equalization/Serration Pulse Vert. Interval Start Time
12	Equalization/Serration Pulse Vert. Interval End Time
Vertical Interrupt Specification Registers	
13	Vertical Interrupt Activate Time
14	Vertical Interrupt Deactivate Time
Cursor Control Register (not used on MFG)	
15	Horizontal Cursor Position Start Time
16	Horizontal Cursor Position End Time
17	Vertical Cursor Position Start Time
18	Vertical Cursor Position End Time

Der LM 1882 besteht intern aus einem Statusregister und 18 Datenregistern, welche einzeln programmiert werden können. Alle Register sind 12-Bit breit. Die gesamte Einstellung des Betriebsmodus wird über die Addresse LM_1882_LOAD (0x00000540) abgewickelt. Zur Programmierung des Chips stehen zwei verschiedene Modi zur Verfügung:

Zum einen der manuelle Modus bei dem die Schreibfolge Registeradresse, Lowbyte, Highbyte lautet, zum anderen der automatische Modus, bei dem die Startadresse und danach nur noch eine Folge von Registerinhalten (jeweils Low-/Highbyte) angegeben wird. Auf diese beiden Modi soll im folgenden noch etwas näher eingegangen werden:

Manueller Modus: Um im manuellen Modus ein Register beschreiben zu können muss zuerst die Adresse des Registers, sodann der Registerinhalt als Low-/Highbyte-Folge angegeben werden:

Die Registernummer wird über die Wortadresse LM_1882_LOAD in den Baustein geschrieben. Bit 8 und 9 dürfen dabei nicht gesetzt sein. Zum Schreiben des Low-Bytes wird dann Bit 8 gesetzt. Das High-Byte läßt sich nun nach Setzen von Bit 8 und Bit 9 schreiben. Zum Schreiben weiterer Adressen des LM 1882 muss die Sequenz wieder von vorne durchlaufen werden. Für die komplette Initialisierung sind somit 57 Schreibzugriffe (3 x 19) erforderlich.

Automatischer Modus: Der Automatische Modus wird speziell dazu benutzt, um mehrere aufeinander folgende Register zu beschreiben. Er bietet sich also insbesondere für eine komplette Initialisierung des Bausteins an. Die Schreibsequenz sieht dabei wie folgt aus:

In diesem Fall wird die Registernummer bei der begonnen werden soll mit gesetztem Bit 9 (Bit 8 muß logisch '0' sein) über die Wortadresse LM_1882_LOAD in den LM 1882 geschrieben. Damit ist der automatische Modus aktiviert und mit darauffolgenden Schreibzugriffen lassen sich nun mehrere 12-Bit Register unmittelbar nacheinander initialisieren. Die Reihenfolge ist jeweils Low-Byte/High-Byte wobei beide Bits (8 und 9) gesetzt sein müssen. Jetzt gilt es noch mit einem abschließenden Schreibzugriff auf LM_1882_LOAD mit gelöschten Bits 8 und 9 den automatischen Modus zu beenden. Danach befindet sich der LM 1882 wieder im manuellen Modus. Die komplette Initialisierung im automatischen Modus braucht somit nur 39 Schreibzugriffe (1 + 2 x 19).

Eine genaue Erklärung für die Einstellung des Timings ist den Seiten 3 und 4 des LM1882 Datenblattes im Anhang zu entnehmen. Ein Beispiel für die Register-Programmierung nach RS 170 Spezifikation ist ebenfalls in diesem Datenblatt zu finden.

2.3.5   Programmierbarer Intervall Zähler 82C54

2.3.5.1   Funktionsbeschreibung

Mit dem Intel 82C54 können aus dem aufgenommenen Bild die interessierenden Bild-Zeilen ausgeschnitten werden. Der 82C54 ist ein programmierbarer Interval Timer, der aus drei 16 Bit Zählern besteht, die unabhängig von einander genutzt werden können. Die gewünschte Verzögerungszeit wird eingestellt, indem die Zähler mit einem Wert vorbesetzt und dann mit einem definierten Takt heruntergezählt werden.

Der 82C54 verfügt über 6 verschiedene Betriebsmodi, der vom MFG verwendete Modus ist der Mode 1, 'Hardware Retriggerable One-Shot'. Über die Rechner-Schnittstelle wird der 82C54 mit einem Wert N geladen. Nach dem Start des Zählers vergehen N Taktzyklen, dann ist der Inhalt des Zählers 0 und der Ausgang springt auf "high". Der Zähler merkt sich die geladenen Werte und mit dem nächsten Triggerimpuls ist der Zähler wieder aktiv.

Vom MFG werden nur die Zähler 0 und 1 benutzt. Als Taktsignale dienen die HSYNC-Impulse aus dem Bt261. Der Zähler 0 dient zur Bestimmung des oberen <u>inaktiven</u> Bildbereiches. Seine Programmierung (N0) legt also die erste aktive Zeile eines Bildes fest. Nachdem die erste aktive Zeile eines Bildes erreicht wurde, - N0 HSYNC-Impulse wurden gezählt - aktiviert Zähler 1 den 'sichtbaren' Bereich des Bildes für N1 Takte. Nach diesen N1 HSYNC-Impulsen werden weitere Daten des A/D-Wandlers wieder ignoriert. Mit jedem VSYNC-Impuls werden die Zähler zurückgesetzt und der Vorgang beginnt von vorne. Mit Hilfe dieser Zähler-Mimik wird Position und Anzahl der Zeilen eines interessierenden Bildbereiches auch, 'Region of Interest' (kurz ROI), bestimmt. Ergänzend dazu kann mit Hilfe des Bt261 der Spaltenbereich eingestellt werden, der von Interesse ist. Die Programmierung hierfür ist der Beschreibung des Bt261 im Anhang zu entnehmen.

2.3.5.2   Programmierung

Über vier Wortadressen lassen sich die 8-bit Register des 82c54 vom Transputer ansprechen.

82c54 Adress-Lage			'C'Definition
$00000500 r/w	Counter	Register 0	COUNTER_0
$00000504 r/w	Counter	Register 1	COUNTER_1
$00000508 r/w	Counter	Register 2	COUNTER_2
$0000050C /w	Control	Register	CONTROL_WORD

Um einen Zähler zu laden sind drei Schreibzugriffe notwendig: Zunächst wird das Control-Register beschrieben, dessen Wert legt fest dann fest wie ein Zähler gesetzt wird. Es ist möglich High-Byte und Low-Byte der Zähler getrennt zu setzen oder beide direkt nacheinander (erst die unteren 8 Bit, dann die oberen 8 Bit). Die folgende Tabelle zeigt wie die verschiedenen Modi über das Control-Register selektiert werden:

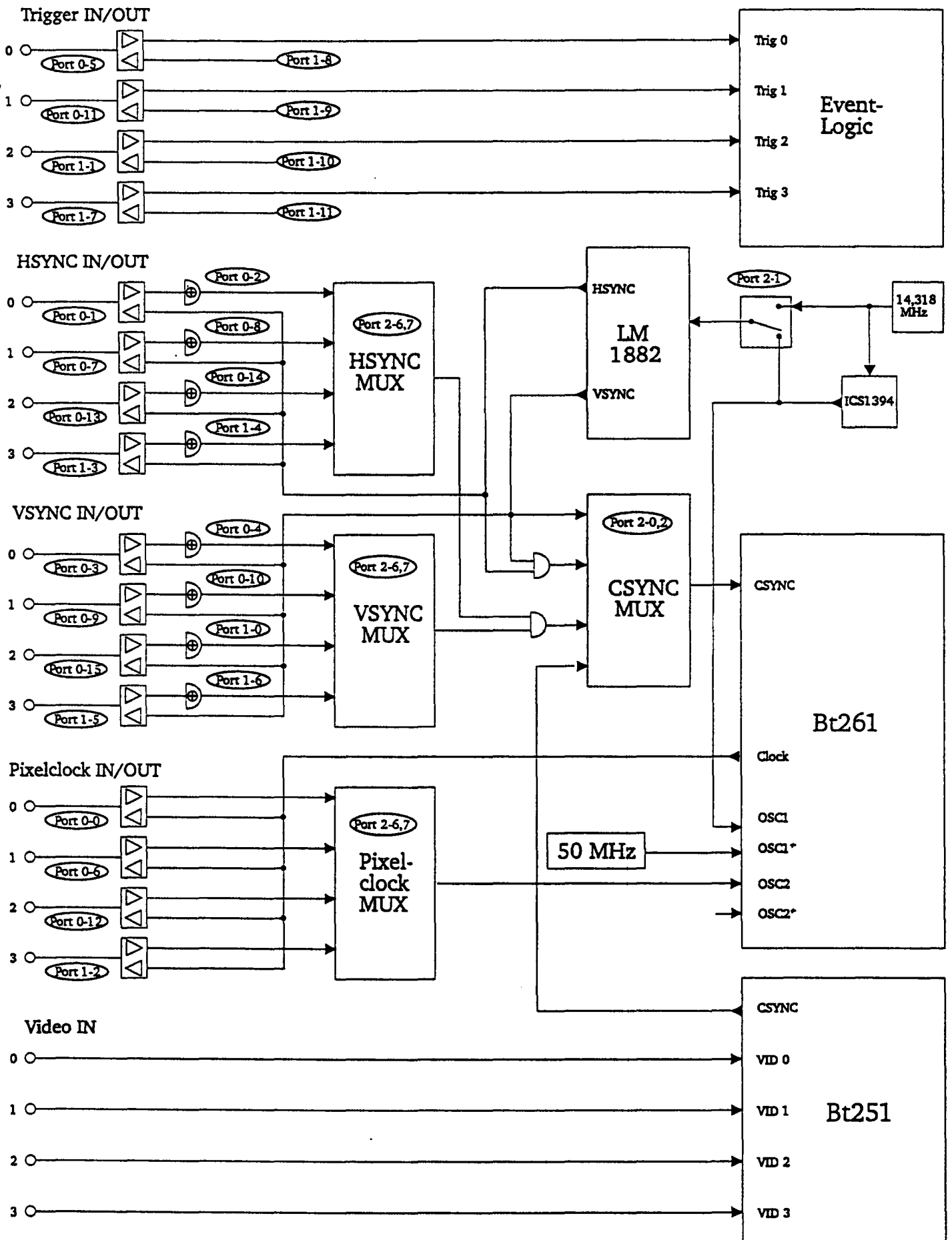| Intel 82c54 Control Register		'C' Definition
Bit 7,6	Counter Select	
0 0	Counter 0	(SEL_COUNT_0)
0 1	Counter 1	(SEL_COUNT_1)
1 0	Counter 2	(SEL_COUNT_2)
1 1	Multi Latch	(MULTI_LATCH)
Bit 5,4	Read/Write Mode	
0 0	Count Latch	(COUNT_LATCH)
0 1	Low Byte Only	(LOW_1_BYTE)
1 0	High Byte Only	(HIGH_1_BYTE)
1 1	Low Byte and High Byte	(LH_2_BYTE)
Bit 3,2,1	Count Modes	
0 0 0	Mode 0	(MODE_0)
0 0 1	Mode 1 HW Retrigg. One Shot	(MODE_1)
0 1 0	Mode 2	(MODE_2)
0 1 1	Mode 3	(MODE_3)
1 0 0	Mode 4	(MODE_4)
1 0 1	Mode 5	(MODE_5)
Bit 0	Binary/BCD Select	
0	Binary	(BINARY)
1	BCD	(BCD)

2.3.6   Video Interface

Das Video Interface des TIP-MFG bietet die Möglichkeit bis zu vier Video-Signalquellen anzuschliessen. Jeder der vier Video Ports besteht aus 5 Signalen, welche individuell als Eingang oder Ausgang konfigurierbar sind (vgl. Darstellung "Video Interface And Timing Generators" auf der nächsten Seite). Darüberhinaus läßt sich für die HSYNC- und VSYNC-Eingänge die Polarität festlegen, da diese im Allgemeinen kameraabhängig sind.

Signal	Konfigurierbar als	Invertierung
Video	Eingang	
HSYNC	Eingang/Ausgang	für Eingang möglich
VSYNC	Eingang/Ausgang	für Eingang möglich
Pixelclock	Eingang/Ausgang	
Trigger	Eingang/Ausgang	

Die Konfigurierung erfolgt über die Programmierung der 16-bit breiten Port-Register 0 und 1 des MFG. Jeweils 6 bit sind einem Kamera-Interface zugeordnet. Die genaue Belegung der MFG-Port-Register wird im nächsten Kapitel dargestellt.

MFG - Video-Interface and Timing Generators

Trigger IN/OUT

0 — Port 0-5 / Port 1-8 — Trig 0
1 — Port 0-1 / Port 1-9 — Trig 1
2 — Port 1-1 / Port 1-10 — Trig 2
3 — Port 1-7 / Port 1-11 — Trig 3

Event-Logic

HSYNC IN/OUT

0 — Port 0-1 / Port 0-2
1 — Port 0-7 / Port 0-8
2 — Port 0-13 / Port 0-14
3 — Port 1-3 / Port 1-4

HSYNC MUX (Port 2-6,7)

LM 1882 — HSYNC, VSYNC

Port 2-1

14,318 MHz

ICS1394

VSYNC IN/OUT

0 — Port 0-3 / Port 0-4
1 — Port 0-9 / Port 0-10
2 — Port 0-15 / Port 1-0
3 — Port 1-5 / Port 1-6

VSYNC MUX (Port 2-6,7)

CSYNC MUX (Port 2-0,2)

Bt261

- CSYNC
- Clock
- OSC1
- OSC1⁺
- OSC2
- OSC2⁺

50 MHz

Pixelclock IN/OUT

0 — Port 0-0
1 — Port 0-6
2 — Port 0-12
3 — Port 1-2

Pixel-clock MUX (Port 2-6,7)

Video IN

0 — VID 0
1 — VID 1
2 — VID 2
3 — VID 3

Bt251

CSYNC

The symbol Port 1-2 specifies port register and control bit.

2.3.7 Die MFG Portregister

Für allgemeine Einstellungen besitzt das MFG drei Portregister (nicht zu verwechseln mit den vier Kamera-Ports). Über diese Register lassen sich die vier Kameraports konfigurieren, die Sequencer starten und anhalten, sowie einige Multiplexer steuern. Die Portregister 0 und 1 sind jeweils 16 Bit breit, das Portregister 2 hat 8 Bit Breite. Die folgenden Tabellen zeigen die Adressen der Portregister im Speicher und die Bedeutung der einzelnen Bits im Detail:

Bit-Belegung für MFG Port Register 0		Adresse: $00000400	
Kamera Interface 0		**Richtung/Modus**	
0	Pixelclock	0 - Eingang	1 - Ausgang
1	HSYNC	0 - Eingang	1 - Ausgang
2	HSYNC Polarität *)	0 - nicht inv.	1 - invertiert
3	VSYNC	0 - Eingang	1 - Ausgang
4	VSYNC Polarität *)	0 - nicht inv.	1 - invertiert
5	Trigger	0 - Eingang	1 - Ausgang
Kamera Interface 1		**Richtung/Modus**	
6	Pixelclock	0 - Eingang	1 - Ausgang
7	HSYNC	0 - Eingang	1 - Ausgang
8	HSYNC Polarität *)	0 - nicht inv.	1 - invertiert
9	VSYNC	0 - Eingang	1 - Ausgang
10	VSYNC Polarität *)	0 - nicht inv.	1 - invertiert
11	Trigger	0 - Eingang	1 - Ausgang
Kamera Interface 2		**Richtung/Modus**	
12	Pixelclock	0 - Eingang	1 - Ausgang
13	HSYNC	0 - Eingang	1 - Ausgang
14	HSYNC Polarität *)	0 - nicht inv.	1 - invertiert
15	VSYNC	0 - Eingang	1 - Ausgang

*) Polarität kann nur für Betrieb als Eingang gewählt werden.

Bit-Belegung für MFG Port Register 1		Adresse: $00000440	
Kamera Interface 2		**Richtung/Modus**	
0	VSYNC Polarität *)	0 - nicht inv.	1 - invertiert
1	Trigger	0 - Eingang	1 - Ausgang
Kamera Interface 3		**Richtung/Modus**	
2	Pixelclock	0 - Eingang	1 - Ausgang
3	HSYNC	0 - Eingang	1 - Ausgang
4	HSYNC Polarität *)	0 - nicht inv.	1 - invertiert
5	VSYNC	0 - Eingang	1 - Ausgang
6	VSYNC Polarität *)	0 - nicht inv.	1 - invertiert
7	Trigger	0 - Eingang	1 - Ausgang
Steuerung der Trigger-Signale an den Kameraports			
8	Trigger 0	logisch '1' liefert ein TTL-High Signal	
9	Trigger 1	logisch '1' liefert ein TTL-High Signal	
10	Trigger 2	logisch '1' liefert ein TTL-High Signal	
11	Trigger 3	logisch '1' liefert ein TTL-High Signal	
12	reserviert		
13	reserviert		
FIFO Kontrolle			
14	Sequencer für FIFO-Eingangsseite	0 - Stop	1 - Start
15	Sequencer für FIFO-Ausgangsseite	0 - Stop	1 - Start

*) Polarität kann nur für Betrieb als Eingang gewählt werden.

Bit-Belegung für MFG Port Register 2	Adresse: $00000680

Bit 0 und 2 steuern den CSYNC Multiplexer, hiermit wird also ausgewählt, welches CSYNC-Signal zum Bt261 durchgeschaltet wird.

2	0	
0	0	CSYNC von Kamera Ports (HSYNC/VSYNC)
0	1	CSYNC vom Bt251
1	0	HSYNC/VSYNC vom LM1882
1	1	CSYNC vom LM1882 (auf VSYNC-Ausgang)

Mit Bit 1 wird der Eingangs-Oszillator für den LM1882 bestimmt

0	Programmierbarer Video Oszillator ICS 1394 .
1	14.318 MHz Quarz-Oszillator

Bit 3 legt den Modus fest, in dem die Bilddaten von der FIFO-Ausgangsseite in den Video-Speicher abgelegt werden

0	Alle Bildzeilen werden nacheinander abgelegt (consecutive mode)
1	Je eine Bildzeile wird in einer Videozeile abgelegt (row oriented mode)

Bit 4 legt fest wann auf der FIFO-Eingangsseite End-Of-Image Marken erzeugt werden. Diese EOI-Marken steuern auf der FIFO-Ausgangsseite das Zurücksetzen des Adresszeigers auf den VRAM-Anfang. Im Row-Oriented/Interlaced-Mode muß dieses Bit gesetzt sein.

0	EOI mit jedem FIELD
1	EOI mit jedem VSYNC

Bit 5 ist reserviert

Bit 6 und 7 steuern die Eingangs-Multiplexer der Kamera-Ports, d.h. sie legen fest von welchem Kamera-Port HSYNC, VSYNC und Pixelclock durchgeschaltet werden

7	6	
0	0	Kamera Port 0
0	1	Kamera Port 1
1	0	Kamera Port 2
1	1	Kamera Port 3

2.3.8   MFG Memory Layout

Transputer Sektion

$00000080	Status Register	32-bit	r/
$000000C0	Reset Register	32-bit	/w
$00000180	General Purpose Register	32-bit	r/w
$000001C0	Event Register	32-bit	r/w
$00000200	Analyse Register	32-bit	/w
$00000300	Reset Control Register	32-bit	/w

RAM Sektionen

$80000000	DRAM START
$803FFFFF	DRAM End
$90000000	VRAM Start
$901FFFFF	VRAM End

Digitizer Sektion

$00000400	PORT_0	16-bit	/w
$00000440	PORT_1	16-bit	/w
$00000680	PORT_2	16-bit	/w
$00000700	Image Register	32-bit	/w

Video Clock Generator ICS 1394

$00000480	I1394	8-bit	/w

Zähler-Baustein 82C54:

$00000500	COUNTER_0	8-bit	r/w
$00000504	COUNTER_1	8-bit	r/w
$00000508	COUNTER_2	8-bit	r/w
$0000050C	CONTROL_WORD	8-bit	/w

Bt251 Digitizers:

$00000580	ADDR_REG_251	8-bit	r/w
$00000584	RAM_LOC	8-bit	r/w
$00000588	COMMAND_REG	8-bit	r/w
$0000058C	RESERVED_LOC	8-bit	r/w

Bt261 Line Lock Controller:

$000005C0	ADDR_REG_261	8-bit	r/w
$000005C4	CONTROL_REG_261	8-bit	r/w

LM 1882 Video Sync Generator:

$00000540 LM_1882_LOAD	32-bit	/w
$000006C0 LM_1882_READ	32-bit	r/

TIP-Bus Sektion

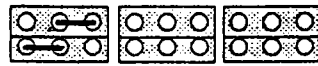|		
$00001000 Go Register	32-bit	/w
$00020000 Channel RAM Start	32-bit	r/w
$00030000 Parameter RAM Start	32-bit	r/w
$00040000 VRAM Address RAM Start	32-bit	r/w
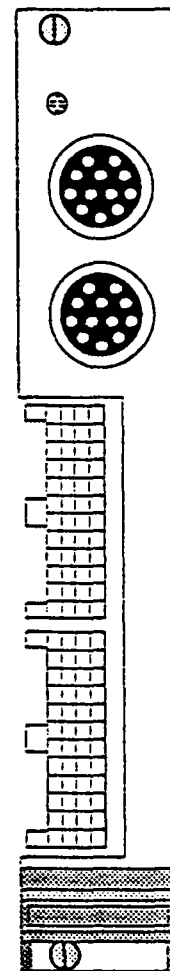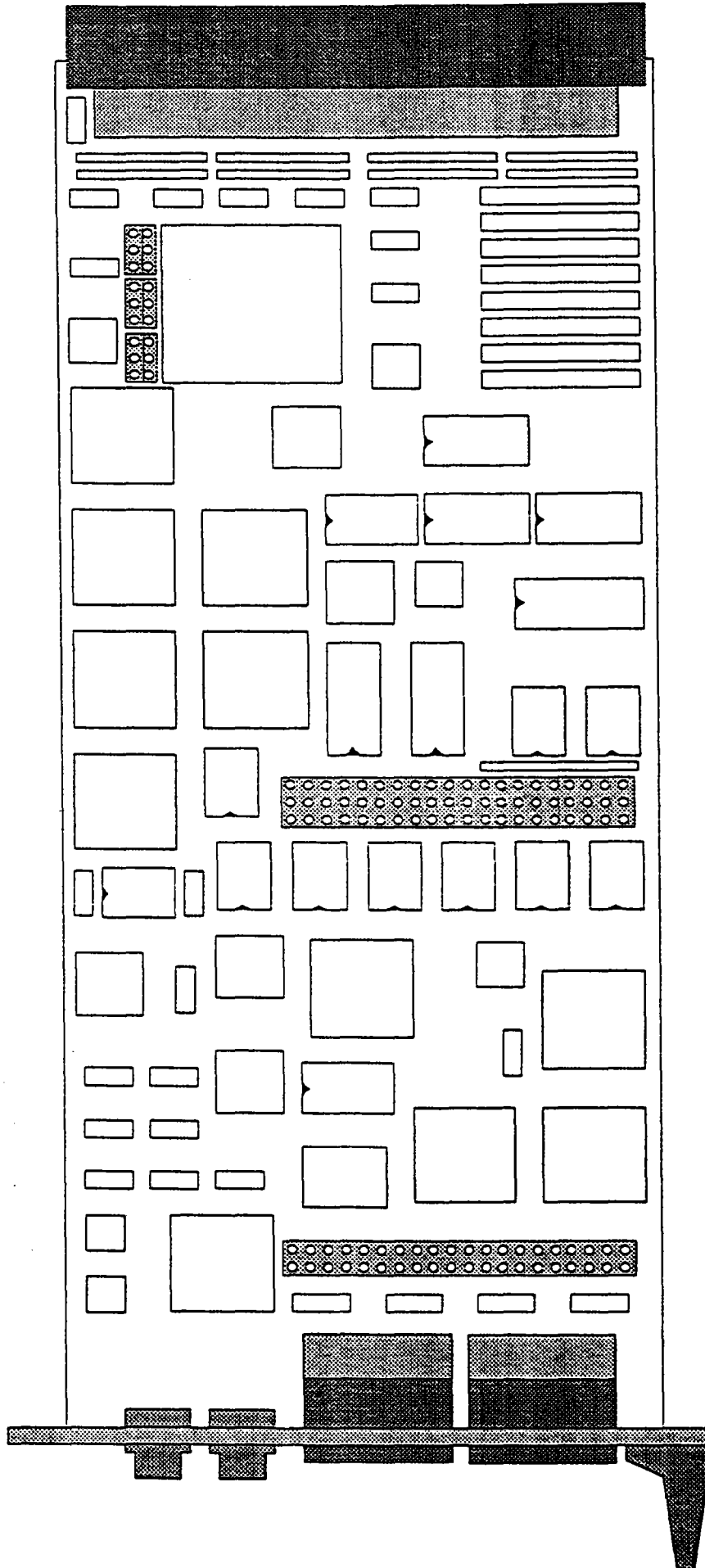
Video Input
Connector
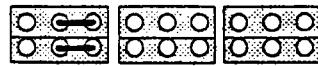(Hirose)

TIP-Bus
Connectors
(Metral)

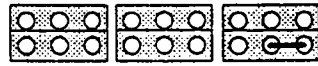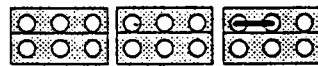**MFG - Jumperbelegung**
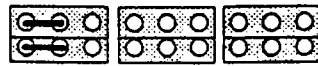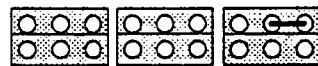
Prozessor-Takt

20 MHz
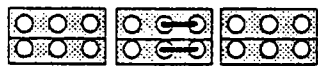
25 MHz

30 MHz

Zyklen für Speicherzugriff
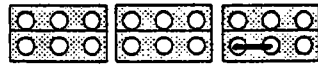
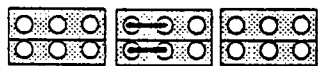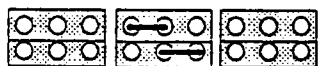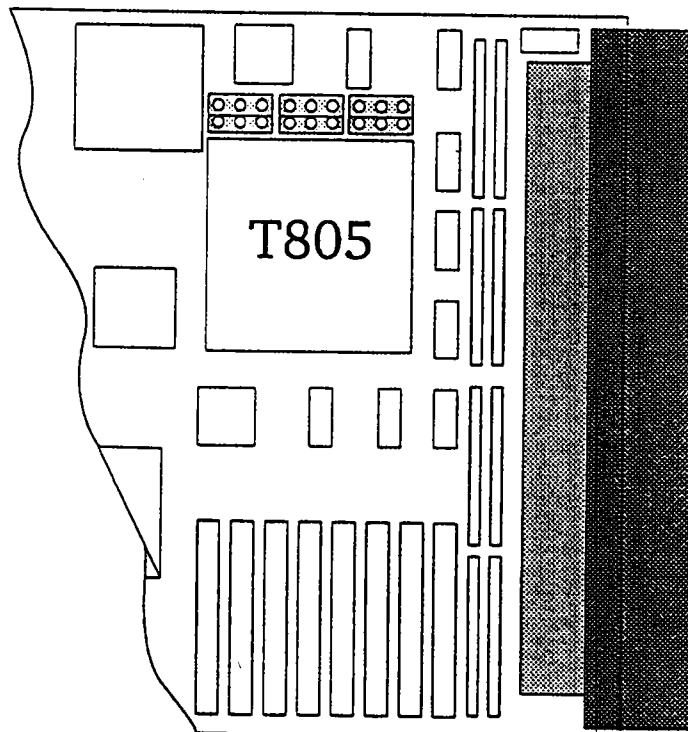3 Zyklen

4 Zyklen

5 Zyklen

6 Zyklen

Link Geschwindigkeit

Alle Links: 20 MB/s

Alle Links: 10 MB/s

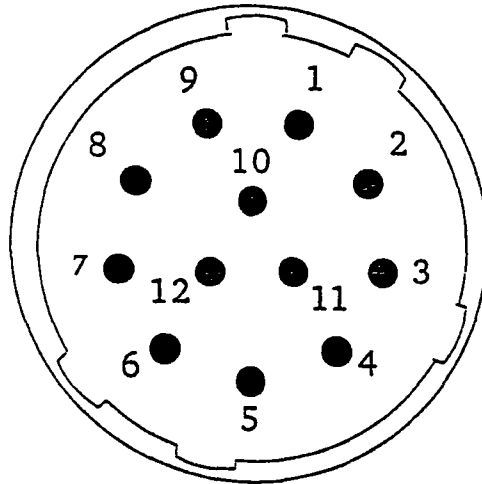Link 0: 20 MB/s, Links 1,2,3: 10 MB/s

Link 0: 10 MB/s, Links 1,2,3: 20 MB/s

T805

MFG - Belegung der 96-poligen DIN-Steckerleiste

	a	b	c
1	Reset 0 out +	Reset 1 out +	Reste 0 out -
2	Link 0 out +	Reset 1 out -	Link 0 out -
3	GND	Link 1 out +	GND
4	Link 0 in -	Link 1 out -	Link 0 in +
5	Reset 0 in -	Link 1 in -	Reset 0 in +
6	Link 1 in +	Reset 1 in -	Reset 1 in +
7	Reset 2 out +	Reset 3 out +	Reset 2 out -
8	Link 2 out +	Reset 3 out -	Link 2 out -
9	GND	Link 3 out +	GND
10	Link 2 in -	Link 3 out -	Link 2 in +
11	Reset 2 in -	Link 3 in -	Reset 2 in +
12	Link 3 in +	Reset 3 in -	Reset 3 in +
13	RTSC 2 out +	RTSC 2 out +	RTSC 2 out -
14	RTSC 0 out +	RTSC 2 out -	RTSC 0 out -
15	GND	RTSC 0 out +	GND
16	RTSC 0 in -	RTSC 0 out -	RTSC 0 in +
17	RTSC 2 in -	RTSC 0 in -	RTSC 2 in +
18	RTSC 0 in +	RTSC 2 in -	RTSC 2 in +
19	RTSC 3 out +	RTSC 3 out +	RTSC 3 out -
20	RTSC 1 out +	RTSC 3 out -	RTSC 1 out -
21	GND	RTSC 1 out +	GND
22	RTSC 1 in -	RTSC 1 out -	RTSC 1 out +
23	RTSC 3 in -	RTSC 1 in -	RTSC 3 in +
24	RTSC 1 in +	RTSC 3 in +	Master Reset
25	NC	RTSC 3 in -	NC
26	NC	LSP	NC
27	+5V	+5V	+5V
28	+5V	+5V	+5V
29	+5V	+5V	+5V
30	GND	GND	GND
31	GND	GND	GND
32	GND	GND	GND

UniLink Connectors

Link 0

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

Link 1

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

Link 2

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

Link 3

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

1 Reset in +
2 Reset in -
3 Link in +
4 Link in -
5 not connected
6 not connected
7 Link out -
8 Link out +
9 Reset out -
10 Reset out + out +

Real Time Sync Channel Connectors

RTSC 0 & 2

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

RTSC 0 & 2

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

1 RTSC 2 in +
2 RTSC 2 in -
3 RTSC 0 in +
4 RTSC 0 in -
5 not connected
6 not connected
7 RTSC 2 out -
8 RTSC 2 out +
9 RTSC 0 out -
10 RTSC 0 out +

RTSC 1 & 3

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

RTSC 1 & 3

2	4	6	8	10
o	o	o	o	o
o	o	o	o	o
1	3	5	7	9

1 RTSC 3 in +
2 RTSC 3 in -
3 RTSC 1 in +
4 RTSC 1 in -
5 not connected
6 not connected
7 RTSC 3 out -
8 RTSC 3 out +
9 RTSC 1 out -
10 RTSC 1 out +

1: PIXELCLOCK 0
2: VSYNC 0
3: GND
4: VIDEO 0
5: PIXELCLOCK 1
6: VSYNC 1
7: TRIGGER 1
8: GND
9: VIDEO 1
10: HSYNC 0
11: TRIGGER 0
12: HSYNC 1
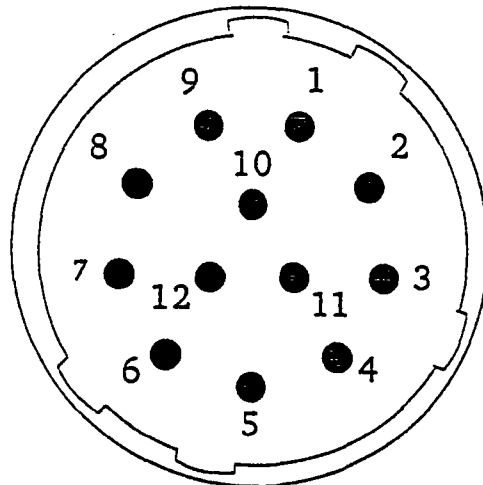
1: PIXELCLOCK 2
2: VSYNC 2
3: GND
4: VIDEO 2
5: PIXELCLOCK 3
6: VSYNC 3
7: TRIGGER 3
8: GND
9: VIDEO 3
10: HSYNC 2
11: TRIGGER 2
12: HSYNC 3

- - New Pinout Information - -

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

Distinguishing Features

- 4 Software Selectable Analog Inputs
- DC- or AC-Coupled Video Inputs
- Optional MPU Adjustment of Gain and Offset
- Composite Sync Detection
- 8-bit Flash A/D Converter
- R/2 Reference Ladder Tap
- 256 x 8 Lookup Table
- Genlock Externally Implemented
- Standard MPU Interface
- TTL Compatible
- +5v CMOS Monolithic Construction
- 44-pin PLCC Package
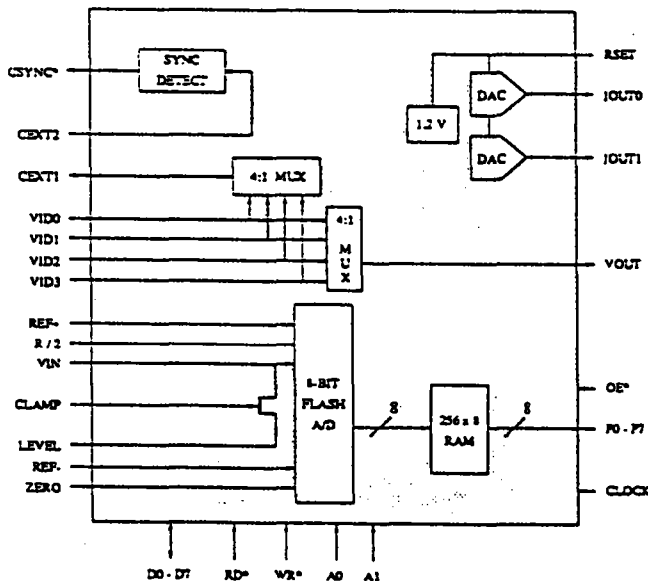- Typical Power Dissipation: 750 mW

Applications

- Image Processing
- Image Capture
- Desktop Publishing
- Graphic Art Systems

Related Products

- Bt253
- Bt261

Functional Block Diagram

18 MSPS
Monolithic CMOS
Single Channel
8-bit Image Digitizer

Product Description

The Bt251 Image Digitizer is designed to digitize standard video signals (RS-170, RS-170A RS-343A, RS-330, PAL, or SECAM). The architecture of the Bt251 enables the addition of external circuitry for filtering, gain, etc., along the signal path. A standard MPU interface is provided for accessing various control functions.

Four analog inputs are supported, selectable under MPU control. The MPU may select from which input to detect sync information for external genlocking independently of the video input being digitized. A TTL-compatible composite sync signal is output to interface to the genlock circuitry.

The output of the 8-bit A/D converter addresses 256 x 8 lookup table RAM, enabling real-time image manipulation prior to data storage including thresholding, contrast enhancement reversing video, implementing a nonlinear A/D etc. The digitized data outputs may be three-stated asynchronously to clock via the OE* control.

Optional MPU controlled adjustment of gain and offset is supported by the ability to program the levels of the REF+ and REF- inputs to the A/D Zeroing and clamping signals are available to control the A/D timing for application specific designs. The clamping level is externally set via the LEVEL pin.

Brooktree®

Circuit Description

MPU Interface

As shown in the functional block diagram, the Bt251 supports a standard MPU interface (D0 - D7, RD*, WR*, A0, and A1). MPU operations are asynchronous to the clock.

An internal 8-bit address register, in conjunction with A0 and A1, is used to specify which control register or RAM location the MPU is accessing, as shown in Table 1. All registers and RAM locations may be written to or read by the MPU at any time; however, while digitizing a video signal, the MPU should not access the RAM as this will corrupt the digitized data.

The address register increments after each MPU read or write cycle. After writing to location $FF, the address register resets to $00. ADDR0 corresponds to D0 and is the least significant bit.

Flash A/D Converter

The Bt251 uses an 8-bit flash A/D converter to digitize the video signal. The A/D digitizes analog signals in the range of REF- ≤ Vin ≤ REF+. The output will be a binary number from $00 (Vin ≤ REF-) to $FF (Vin ≥ REF+).

VIN may be either DC- or AC-coupled to the video signal. If AC-coupled, the CLAMP and LEVEL controls may be used to DC restore the video signal.

Analog Input Selection

The Bt251 supports four analog input sources, VID0 - VID3. The MPU specifies which one is to be digitized via the command register.

The selected video signal is output onto VOUT. VOUT may be connected directly to VIN if no filtering or gain of the video signal is required.

If digitizing a video signal containing color subcarrier information, and only the luminance information is to be digitized, a filter should be used to remove the subcarrier information to avoid possible artifacts on the display screen. A low pass filter, notch filter, or comb filter may be used to remove the chroma information.

Note that sync information (if present) will still be present on VOUT.

The multiplexers are not a break-before-make design. Therefore, during the multiplexer switching time it is possible for the input video signals to be connected together through the equivalent of 200 ohms.

The 75-ohm resistors to ground (Figure 1) provide the typical 75-ohm termination required by video signals.

A1	A0	ADDR7 - ADDR0	Addressed by MPU
0	0	xxxx xxxx	address register
0	1	0000 0000	RAM location $00
0	1	0000 001	RAM location $01
:	:	:	:
0	1	1111 1111	RAM location $FF
1	0	xxxx xx00	command register
1	0	xxxx xx01	IOUT0 data register
1	0	xxxx xx10	IOUT1 data register
1	0	xxxx xx11	reserved
1	1	xxxx xxxx	reserved

Table 1. Address Register Operation.

Circuit Description (continued)

A/D Reference Generation

As shown in Figure 1, the Bt251 may be configured to have either fixed or MPU-adjustable references for the A/D converter.

If jumpers J2 and J4 are selected, REF+ is connected to a 0.7v to 1.2v reference (VREF) and REF- is connected to GND. This mode of operation may be used when the only operation is to digitize video signals with an amplitude range of 0.7v to 1.2v with no adjustment of gain or offset.

If jumpers J1 and J3 are selected, gain and offset of the video signal may be done via the MPU adjustable outputs IOUT0 and IOUT1. This mode of operation allows top and bottom reference adjustments so that different video signals may be digitized or operations such as contrast enhancement or level adjustments may be implemented. The LM358 requires a ± 5v power supply in this instance. The ALD2701 or TLC272 dual CMOS op-amps can be used for single +5v operation.

IOUT0 and IOUT1 are current outputs (0 to 1 mA) generated by two 6-bit D/A converters. A 1200-ohm RSET resistor generates a 1 mA full scale output current. 1200-ohm resistors to GND generate a 0v to -1.2v level that drive the REF+ and REF- inputs through voltage followers. The top and bottom references may thus be adjusted with 19 mV resolution.

It is not recommended that the DAC outputs drive the top of the reference ladder directly as the reference ladder resistance changes slightly with temperature.

The DACs are current sources; they do not sink current. Thus, if MPU adjustment of REF- is desired, the DAC output must drive REF- using a voltage follower.

A/D Zeroing

The ZERO input is used to zero the comparators, and must be asserted sometime during each horizontal blanking interval. While ZERO is a logical one, the comparators are zeroed. During ZERO cycles, the P0 - P7 outputs are not updated. They retain the data loaded before the ZERO cycle.

A/D Input Clamping

If VIN is AC-coupled to the video signal, the CLAMP and LEVEL controls may be used to DC restore the video signal. While CLAMP is a logical one, the video signal is clamped to the voltage level present on the LEVEL pin.

When DC restoring RGB or luminance video signals, LEVEL is typically connected to GND (jumper J5 in Figure 1).

When DC restoring color difference video signals, LEVEL is typically at the mid-point between REF+ and REF-. The Bt251 provides an R/2 reference ladder tap that may be used to generate the proper DC voltage (jumper J6 in Figure 1).

If VIN is DC-coupled to the video signal, LEVEL should float or CLAMP should always be a logical zero.

VIN Input Considerations

The 50 - 300 ohm resistor shown in Figure 1 after the low pass filter is only required if an active low pass filter is used. It provides isolation from any clock kickback noise on VIN from being coupled onto the video signal. The exact value of the resistor should be adjusted for minimum clock kickback noise on VIN. If no filter or a passive low pass filter is used, the resistor is not required, as the resistance of the multiplexer serves to reduce the clock kickback noise.

The 0.1 μF capacitor shown in Figure 1 after the low pass filter is only required if an active low pass filter used and DC restoration must be performed. If no filter or a passive low pass filter is used, the capacitor is not required, as the DC restoration can still be implemented using the 0.1 μF capacitors on the VIDx inputs.

Circuit Description (continued)

Figure 1.   Typical Bt251 External Circuitry.
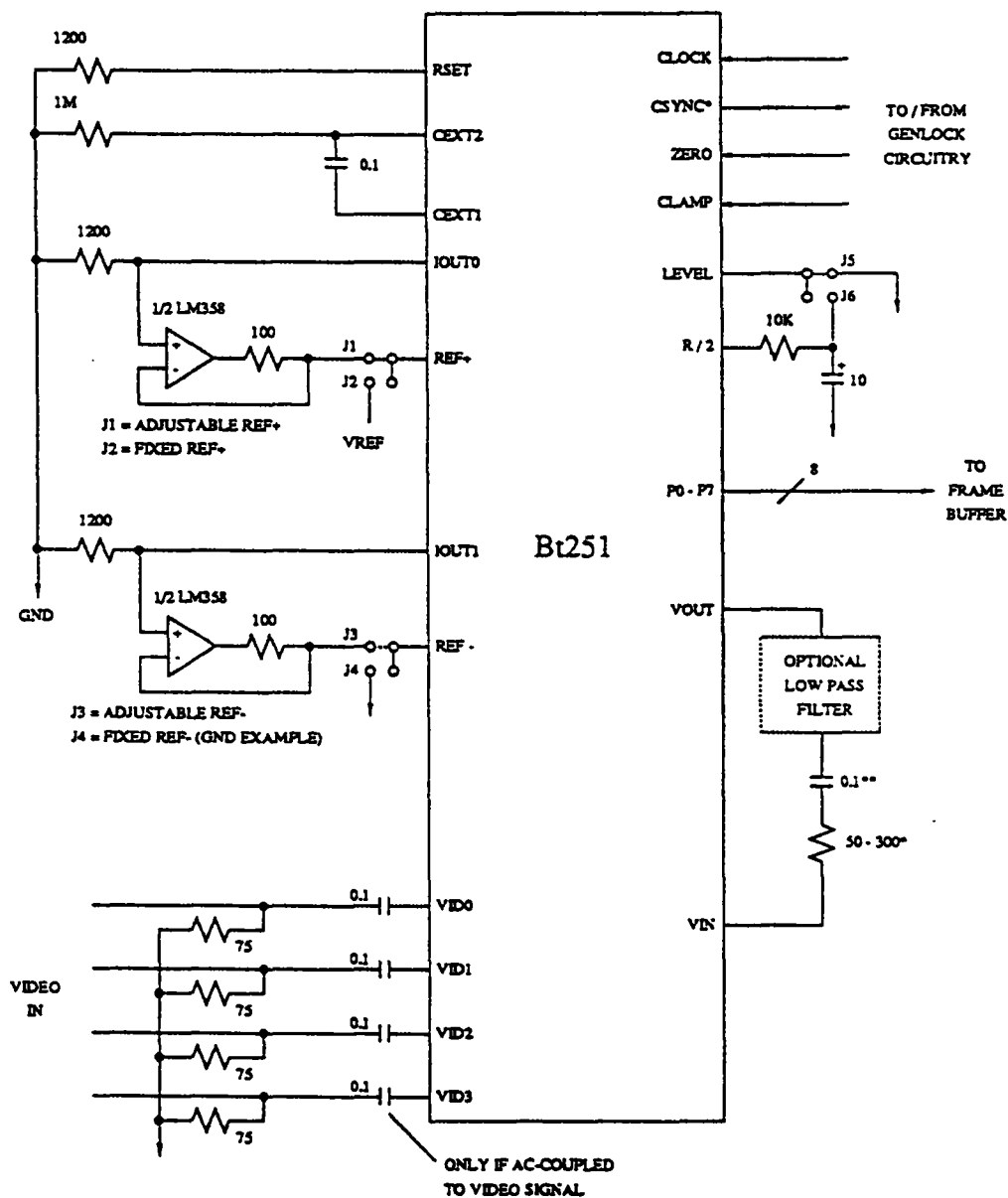
J5 = DC RESTORE TO GND
J6 = COLOR DIFFERENCE DC RESTORE

* NEEDED ONLY IF ACTIVE FILTER IS USED. ADJUST FOR MINIMUM CLOCK KICKBACK.
** NEEDED ONLY IF ACTIVE FILTER IS USED WITH DC RESTORATION.

Circuit Description (continued)

Lookup Table RAM

A 256 x 8 lookup table RAM is provided on-chip to implement simple imaging operations such as gamma manipulation, simple contrast enhancement, inverting of data, or a non-linear transfer function of the A/D converter. Data from the A/D is used to address the RAM; the addressed data is output onto P0 - P7.

The RAM may be effectively bypassed by loading each location with it's corresponding address. As the lookup table RAM is not dual-ported, MPU accesses have priority over digitized data passing through the RAM. During MPU accesses to the RAM, P0 - P7 are undefined.

Sync Detect Circuitry

The Bt251 performs composite sync detection from the analog input specified by the command register. Thus, sync information may be recovered from one analog input while another input is being digitized. The composite sync signal (CSYNC*) contains any serration and equalization pulses the video signal may contain. Note that CSYNC* is output asynchronously to the clock and there are no pipeline delays (the output delay from VIN to CSYNC* is approximately 25 ns).

The MPU specifies from which analog input to detect sync. The selected video signal is output on CEXT1. A 0.1 µF capacitor between CEXT1 and CEXT2 AC-couples the video signal to the sync detection circuit. The MPU selects one of four levels of sync threshold by selecting how many millivolts above the sync tip to use for sync detection. If the sync tip on CEXT2 is below the selected threshold, CSYNC* will be a logical zero.

If it is desired to low-pass filter the sync signal prior to sync detection, the low-pass filter should be inserted between CEXT1 and the 0.1 µF capacitor (see Figure 1.)

If the sync detection circuit is not used, CEXT2 should be connected to GND or VCC (CEXT1 may float), or an unused (grounded) video input selected for the sync detector.

Internal Registers

Command Register

The command register may be written to or read by the MPU at any time, and is not initialized. D0 is the least significant bit.

D7, D6	Digitize select		These bits specify which analog input is to be digitized. The selected signal is output onto VOUT.
	(00)	VID0	
	(01)	VID1	
	(10)	VID2	
	(11)	VID3	

D5, D4	Sync detect select		These bits specify from which analog input sync information is to be detected. The selected signal is output onto CEXT1. It is converted to TTL levels and output onto CSYNC*.
	(00)	VID0	
	(01)	VID1	
	(10)	VID2	
	(11)	VID3	

D3, D2	Sync detect level select		These bits specify how much above the sync tip to slice CEXT2 for sync detection.
	(00)	50 mV	
	(01)	75 mV	
	(10)	100 mV	
	(11)	125 mV	

D1, D0	reserved (logical zero)		

IOUT Data Registers

These two 8-bit registers specify the output current on the IOUT0 and IOUT1 outputs, from 0 mA ($00) to 1 mA ($FC). The six MSBs of data are used to drive the DACs. D0 and D1 (the two LSBs) must be programmed to be a logical zero.

These registers may be written to or read by the MPU at any time, and are not initialized. D0 is the least significant bit.

Pin Descriptions

Pin Name	Description

General Reference Functions

RSET

Full scale adjust control. An external 1200-ohm resistor must be connected between this pin and GND. It is used to provide reference information to the internal D/A converters. See Figure 1.

IOUT0, IOUT1

Current outputs. The amount of output current is specified by the IOUT data registers. External 1200-ohm resistors are typically connected between each pin and GND. See Figure 1. The relationship between full-scale IOUT and RSET is:

$$\text{IOUT (mA)} = 1{,}200 / \text{RSET (ohms)}$$

CEXT1, CEXT2

External capacitor pins. A 0.1 µF capacitor must be connected between CEXT1 and CEXT2 to AC-couple the video signal to the sync detect circuitry. A 1M-ohm resistor must also be connected between CEXT2 and GND. See Figure 1.

A/D Functions

REF+

Top of resistor ladder (voltage input). REF+ sets the VIN voltage level that generates $FF from the A/D converter. A decoupling capacitor is NOT recommended on REF+.

REF-

Bottom of resistor ladder (voltage input). REF- sets the VIN voltage level that generates $00 from the A/D converter.

R/2

Reference ladder mid-point tap. If not used, this pin should remain floating. A decoupling capacitor is NOT recommended on R/2.

ZERO

Zeroing control input (TTL compatible). While ZERO is a logical one, the comparators of the A/D are zeroed. ZERO is latched on the rising edge of CLOCK. During zeroing cycles, P0 - P7 are not updated; they retain the data loaded before the zeroing cycle.

CLAMP

Clamp control input (TTL compatible). While CLAMP is a logical one, the VIN input is forced to the voltage level on the LEVEL pin to perform DC restoration of the video signal. CLAMP is asynchronous to clock. In applications where VIN is DC-coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should always be a logical zero.

LEVEL

Level control input (voltage input). This input is used to specify what voltage level is to be for DC restoration while CLAMP is a logical one. In applications where VIN is DC-coupled to the video signal, LEVEL should float or be connected to VIN, or CLAMP should be a logical zero.

VIN

A/D converter input. The analog signal to be digitized should be connected to this analog input pin. It may be either DC- or AC-coupled to the video signal being digitized.

VID0 - VID3, VOUT

Analog inputs and analog output. VID0 - VID3 are connected to the video signals to be digitized. The signal selected to be digitized is output onto VOUT. Unused inputs should be connected to GND.

Timing Functions

CLOCK

Clock input (TTL compatible). CLOCK should be driven by a dedicated TTL buffer to minimize sampling jitter.

CSYNC*

Recovered composite sync output (TTL compatible). Sync information is detected on the VID0 - VID3 input specified by the command register, converted to TTL levels, and output onto this pin. It is output asynchronously to the clock and there are no pipeline delays.

Pin Descriptions (continued)

Pin Name	Description

Digital Control Functions

P0 - P7 Digitized video data outputs (TTL compatible). Digitized video data is output onto these pins following the rising edge of CLOCK. P0 is the least significant bit. They are three-stated if OE* is a logical one.

OE* Output enable control input (TTL compatible). A logical one three-states the P0 - P7 outputs asynchronously to CLOCK.

RD* Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0 - D7. RD* and WR* should not be asserted simultaneously.

WR* Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0 - D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.

D0 - D7 Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. D0 is the least significant bit.

A0, A1 Address control inputs (TTL compatible). A0 and A1 are used to specify the operation the MPU is performing as indicated in Table 1. They are latched on the falling edge of either RD* or WR*.

Power and Ground

VAA +5v power. All VAA pins must be connected together as close to the device as possible. A 0.1 µF ceramic capacitor should be connected between each group of VAA pins and GND, as close to the device as possible.

GND Ground. All GND pins must be connected.
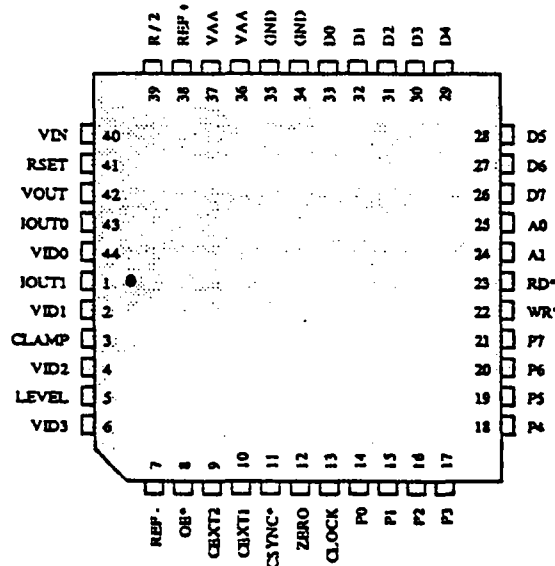
Note: This pinout is for production (Rev. C) silicon, available after September 1, 1989.

The pinout for Rev. A and Rev. B silicon may be obtained from the Second Edition (1989) databook. Rev. A or Rev. B silicon will not be available after December 1, 1989.

PC Board Layout Considerations

PC Board Considerations

The layout should be optimized for lowest noise on the Bt251 power and ground lines by shielding the digital inputs/outputs and providing good decoupling. The lead length between groups of VAA and GND pins should be minimized so as to minimize inductive ringing.

Ground Planes

The ground plane area should encompass all Bt251 ground pins, voltage reference circuitry, power supply bypass circuitry for the Bt251, the analog input traces, any input amplifiers, and all the digital signal traces leading up to the Bt251.

Power Planes

The Bt251 and any associated analog circuitry should have its own power plane, referred to as the analog power plane. This power plane should be connected to the regular PCB power plane (VCC) at a single point through a ferrite bead, as illustrated in Figure 2. This bead should be located within three inches of the Bt251.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all Bt251 power pins, any voltage reference circuitry, and any input amplifiers.

It is important that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode. This will reduce plane-to-plane noise coupling.

Supply Decoupling

The bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance.

Each group of VAA pins should have a 0.1 μF ceramic bypass capacitor to GND, located as close as possible to the device.

Digital Signal Interconnect

The digital signals of the Bt251 should be isolated as much as possible from the analog signals and other analog circuitry. Also, the digital signals should not overlay the analog power plane.

Any termination resistors for the digital signals should be connected to the regular PCB power and ground planes.

Analog Signal Interconnect

Long lengths of closely-spaced parallel video signals should be avoided to minimize crosstalk. Ideally, there should be a ground line between the video signal traces driving the VIDx inputs.

Also, avoid routing high-speed TTL signals close to the analog signals to minimize noise coupling.

PC Board Layout Considerations (continued)
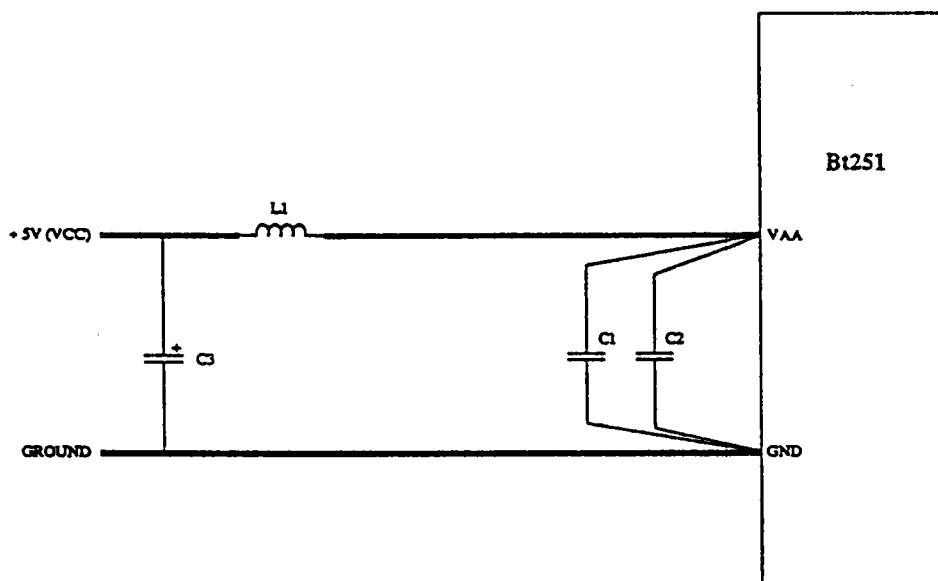
Location	Description	Vendor Part Number
C1, C2 C3 L1	0.1 μF ceramic capacitor 10 μF tantalum capacitor ferrite bead	Erie RPE112Z5U104M50V Mallory CSR13G106KM Fair-Rite 2743001111

Note: The above listed vendor numbers are listed only as a guide. Substitution of devices with similar characteristics will not affect the performance of the Bt251.

Figure 2. Typical Power Supply Connection Diagram and Parts List.

Application Information

Zeroing

Unlike many CMOS A/D converters requiring the comparators to be zeroed every clock cycle, the comparators in the Bt251 are designed to be only periodically zeroed. It is convenient to assert ZERO during each horizontal retrace interval.

Note that before using the Bt251 after a power-up condition, ZERO must be a logical one for at least 1000 clock cycles (cumulative) to initialize the comparators to the rated linearity. In normal video applications this will be transparent due to the number of horizontal scan lines that will have occurred before using the Bt251.

As long as the recommended zeroing interval is maintained, the Bt251 will meet linearity specifications. The longer between zeroing intervals, the more the linearity error increases.

Increasing the Resolution of DACs

With a 1200-ohm resistor connected between each DAC output (IOUT0, IOUT1) and GND, the resolution of the ladder adjustment is 19 mV. The resolution of the top of the resistor ladder (REF+) adjustment may be increased by biasing the DAC outputs and using the DAC outputs to adjust the voltage over a smaller range with finer resolution.

Figure 3 shows a circuit that allows adjustment of the REF+ inputs from 0.714v to 1v with 4.5 mV resolution. With the DAC data = $00, 0.714v is output; if the DAC data = $FC, 1v is output.

As the recommended maximum DAC output is 1 mA, if a 0.286v adjustable range is desired, R1 || R2 must equal 286 ohms. The minimum output voltage desired determines the ratio of R1 and R2:

$$Vmin = VREF * (R2 / (R1 + R2))$$

The bottom of the resistor ladder (REF-) may be adjusted from 0v to 0.287v with 4.5 mV resolution by using a 287-ohm resistor to ground rather than a 1200-ohm resistor. As long as the minimum range is 0v, the resistor to ground may be used to adjust the total range, and thus the resolution.

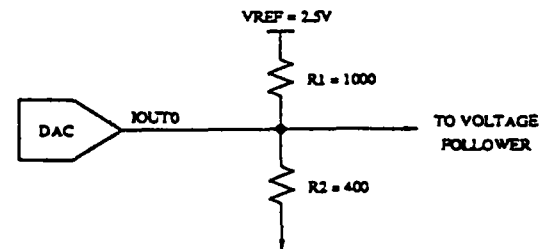| Video Standard	Nominal Amplitude	Worst Case Amplitudes
RS-170 w/o sync	1.0v	0.9v - 1.1v
RS-170 w/sync	1.4v	1.2v - 1.6v
RS-170A w/o sync	1.0v	0.9v - 1.1v
RS-170A w/sync	1.4v	1.0v - 1.8v
RS-343A w/o sync	0.7v	0.6v - 0.85v

Table 2.   Video Signal Tolerances.

Figure 3.   Increasing DAC Output Resolution.

Application Information (continued)

Using an External Reference

Figure 4 illustrates using a 1.2v LM385 to generate a 0v to 1.2v reference for applications requiring a better reference tempco than the internal reference can supply. Supply decoupling of the op-amp is not shown. Any standard op-amp may be used that is capable of operating from a single +5v supply.

As REF+ should be driven by a high AC impedance source, a 100-ohm resistor should be placed between REF+ and the output of the op-amp, as shown in Figure 4. REF- may be driven in a similar manner if a value other than GND is desired.

Input Ranges

Table 2 shows some common video signal amplitudes. For signals possibly exceeding 1.2v, the signal should be attenuated (using a resistor divider network) so as not to exceed the 1.2v input range.

When digitizing with a full scale range less than 0.7v, the Bt251's integral linearity errors are constant in terms of voltage regardless of the value of the reference voltage. Lower reference voltages will therefore produce larger integral linearity errors in terms of LSBs.

For example, by setting the reference difference to 0.6v, 0.6v video signals may be digitized; however the integral linearity error will increase to about ± 1.8 LSB; the SNR will be about 40 dB. With a reference difference of 0.6v, 0.5v video signals may be digitized with an IL error of about ± 2 LSB; the SNR will be about 39 dB.

SNR and Error Rate Vs. Clock Timing

Figure 5 illustrates the A/D error rate vs. clock low time, while Figure 6 illustrates the A/D SNR vs. clock high time.

An A/D error is defined as being a sample that is more than 8 LSBs (out of 255) from the expected value, where the previous and following samples are less than (or equal to) 8 LSBs from the expected value.

Output Noise

Although the A/D does exhibit some output noise for a DC input, the output noise remains relatively constant for any input bandwidth. Competitive A/D converters have no noise for a DC input; however, the output noise increases greatly as the input bandwidth and clock rate increases.

The output noise of the A/D may be reduced by adjusting the duty cycle of the clock -- this is especially true above 10 MHz clock operation. Note that uncorrelated noise less than 1% peak-to-peak will be perceived with the same quality as that of a consumer 1/2" VCR.

PC Board Sockets

If a socket is required, a low-profile socket is recommended.
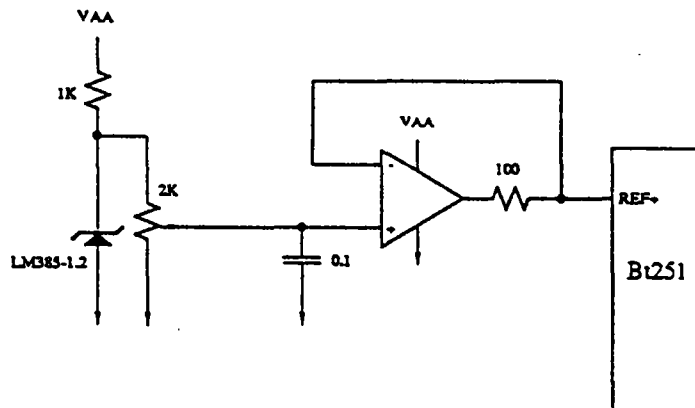

Figure 4. Using An External Reference.
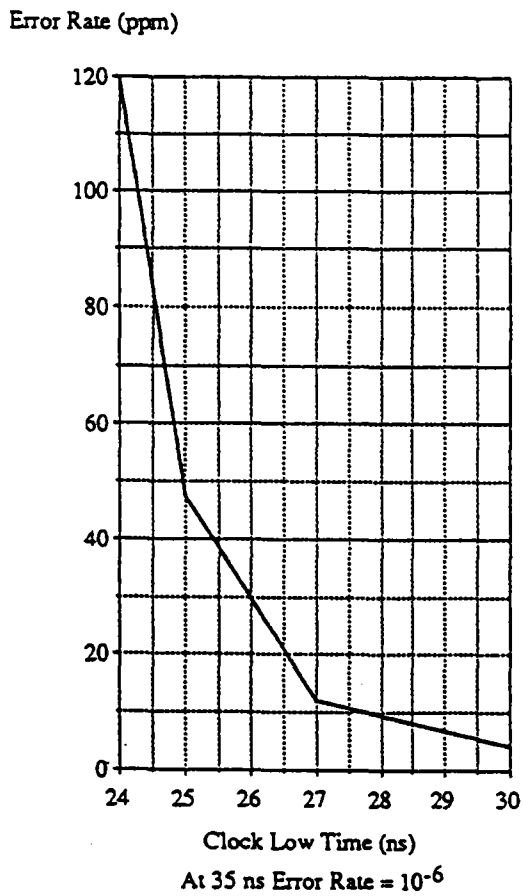
Application Information (continued)

Error Rate (ppm)

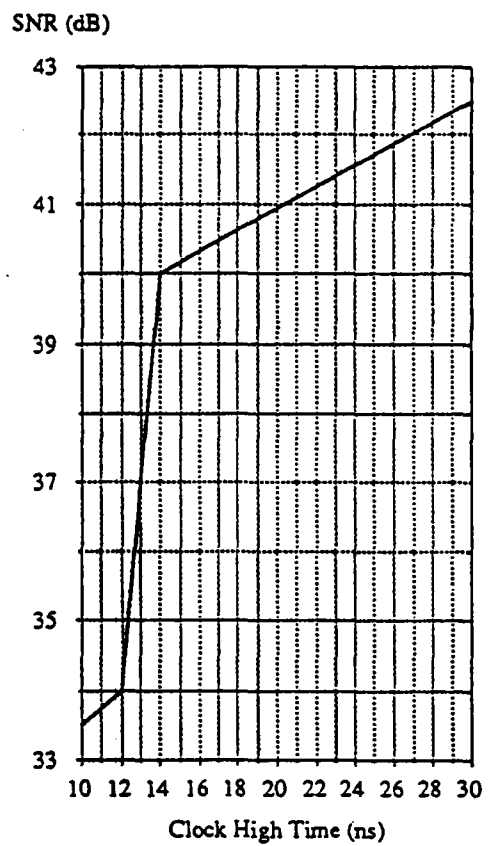**Figure 5.** *A/D Error Rate vs. Clock Low Time.*

At 35 ns Error Rate = 10^{-6}

SNR (dB)

Figure 6. *A/D SNR vs. Clock High Time.*

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VAA	4.75	5.00	5.25	Volts
Voltage References					
Top	REF+	0.7	1	2.0	Volts
Bottom	REF-	0	0	1.3	Volts
Difference (Top - Bottom)		0.7	1	1.2	Volts
VID0 - VID3 Amplitude Range		0.5			Volts
VIN Input Amplitude Range		0.7	1	1.2	Volts
VIN Input Range			REF- to REF+		Volts
LEVEL Input Voltage		GND - 0.5	REF-	REF+	Volts
Zeroing Interval			60	150	μS
Ambient Operating Temperature	TA	0		+70	°C.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VAA (measured to GND)				7.0	Volts
Voltage on any Digital Pin		GND - 0.5		VAA + 0.5	Volts
Analog Input Voltage	VIN, VIDx	GND - 0.5		VAA + 0.5	Volts
R/2 Output Current				25	μA
Ambient Operating Temperature	TA	- 55		+ 125	°C.
Storage Temperature	TS	- 65		+ 150	°C.
Junction Temperature	TJ			+ 150	°C.
Vapor Phase Soldering (1 minute)	TVSOL			220	°C.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
A/D Resolution		8	8	8	Bits
A/D Accuracy					
Integral Linearity Error (note 1)	IL			± 1	LSB
Differential Linearity Error	DL			± 1	LSB
A/D Offset Error					
Top			tbd		mV
Bottom			tbd		mV
Tempco			tbd		mV / °C.
A/D Coding					Binary
No Missing Codes			guaranteed		
VIN Analog Input (note 2)					
CLAMP = 0					
Input Impedance	RIN	10			M ohms
Input Current	IB			1	μA
Input Capacitance	CAIN		15		pF
CLAMP = 1					
Input Impedance	RIN		50		Ohms
VID0 - VID3 Analog Inputs (note 3)					
Input Impedance to VOUT					
Input Selected			100		Ohms
Input Deselected			10		M ohms
Input Capacitance			tbd		pF
REF+ Reference Input					
Input Current			1		mA
Input Impedance			1		K ohms
Clock Kickback (note 4)			tbd		pV - sec
Digital Inputs					
Input High Voltage	VIH	2.0			Volts
Input Low Voltage	VIL			0.8	Volts
Input High Current (Vin = 2.4v)	IIH			1	μA
Input Low Current (Vin = 0.4v)	IIL			- 1	μA
Input Capacitance	CIN		10		pF
P0 - P7 Digital Outputs					
Output High Voltage		2.4			Volts
(IOH = -400 μA)					
Output Low Voltage				0.8	Volts
(IOL = 1.6 mA)					
Three-State Current				1	μA
Output Capacitance			10		pF

See test conditions on next page.

D.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
D0 - D7 Digital Outputs					
Output High Voltage	VOH	2.4			Volts
(IOH = -400 μA)					
Output Low Voltage	VOL			0.8	Volts
(IOL = 3.2 mA)					
Three-State Current	IOZ			1	μA
Output Capacitance	COUT		10		pF
IOUT0 and IOUT1 Outputs					
DAC Output Current		0		1	mA
DAC Output Impedance			100		K ohms
DAC Output Capacitance			20		pF
DAC Output Compliance		- 1		+ 2	Volts
Power Supply Rejection Ratio	PSRR		tbd		% / %
(not including reference)					Δ VAA

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1v and REF- = GND. REF- ≤ Vin ≤ REF+, LEVEL = float.

Note 1: Best-fit linearity. Averaged value evaluated using a closed loop system. Linearity is tested with
         RAM transparent (data = address).
Note 2: LEVEL = GND.
Note 3: VOUT connected to GND.
Note 4: Measurement of noise coupled onto VIN due to clocking (Rs = 75 ohms). Typically occurs over a 5 ns
         interval.

Vin* (v)	P0 - P7	OE*
> 0.996	SFF	0
0.992	SFE	0
:	:	:
0.500	S81	0
0.496	S80	0
0.492	S7F	0
:	:	:
0.004	S01	0
< 0.002	S00	0
	3-state	1

*with REF+ = 1.000v and REF- = 0.000v. Ideal center values. 1 LSB = 3.9063 mV. RAM transparent (data = address).

Table 3.   A/D Coding.

A.C. Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Conversion Rate	Fs			18	MHz
Multiplexer Switching Time	Tmux		100		ns
Clock Cycle Time	1	55.5			ns
Clock Low Time	2	35*			ns
Clock High Time	3	20**			ns
P0 - P7 Output Delay	4			40	ns
OE* Asserted to P0 - P7 Valid	5			50	ns
OE* Negated to P0 - P7 3-Stated	6			50	ns
ZERO Setup Time	7	0			ns
ZERO Hold Time	8	20			ns
ZERO, CLAMP High Time (note 1)		1			Clock
Aperture Delay	9		10		ns
Aperture Jitter			50		ps
Full Power Input Bandwidth	BW	6			MHz
Transient Response (note 2)				1	Clock
Overload Recovery (note 3)				1	Clock
Zero Recovery Time (note 4)				1	Clock
RMS Signal to Noise Ratio	SNR				
Fin = 4.2 MHz, Fs = 10.7 MHz			43		dB
Fin = 4.2 MHz, Fs = 14.32 MHz			42		dB
Fin = 2.75 MHz, Fs = 6.75 MHz			44		dB
Fin = 5.75 MHz, Fs = 13.5 MHz			41		dB
Fin = 4.2 MHz, Fs = 17.72 MHz			41		dB
Analog Multiplexer Crosstalk					
All Hostile Crosstalk			- 50		dB
Single Channel Crosstalk			- 50		dB
Adjacent Input Crosstalk			- 50		dB
IOUT0, IOUT1 Settling Time to ± 1 LSB			100		ns
Differential Gain Error (note 5)	DG		2		%
Differential Phase Error (note 5)	DP		1		Degree
Supply Current (note 6) (Excluding REF+)	IAA		150	tbd	mA

See test conditions on next page.

A.C. Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Units
A0, A1 Setup Time	10	10			ns
A0, A1 Hold Time	11	10			ns
RD*, WR* High Time	12	50			ns
RD* Asserted to Data Bus Driven	13	5			ns
RD* Asserted to Data Valid	14			40	ns
RD* Negated to Data Bus 3-Stated	15			20	ns
WR* Low Time	16	50			ns
Write Data Setup Time	17	10			ns
Write Data Hold Time	18	10			ns
Pipeline Delay		2	2	2	Clocks

Test conditions (unless otherwise specified): "Recommended Operating Conditions" with REF+ = 1v and REF- = GND. REF- ≤ Vin ≤ REF+, LEVEL = float. TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. Timing reference points at 50% for digital inputs and outputs. D0 - D7, P0 - P7, CSYNC* output load ≤ 50 pF. VOUT, IOUT0, IOUT1 output load ≤ 25 pF.

Note 1: Number of clock cycles ZERO is a logical one does not affect linearity. For best performance, ZERO should be a logical one for an odd number of clock cycles.

Note 2: For full-scale step input, full accuracy attained in specified time.

Note 3: Time to recover to full accuracy after a > 1.2v input signal.

Note 4: Time to recover to full accuracy following a zero cycle.

Note 5: 4x NTSC subcarrier, unlocked.

Note 6: IAA (typ) at VAA = 5.0v, Fin = 4.2 MHz, Fs = 14.32 MHz.
IAA (max) at VAA = 5.25v, Fin = 6 MHz, Fs = 18 MHz.

*For 10^{-6} typical A/D error rate (see Figure 5).

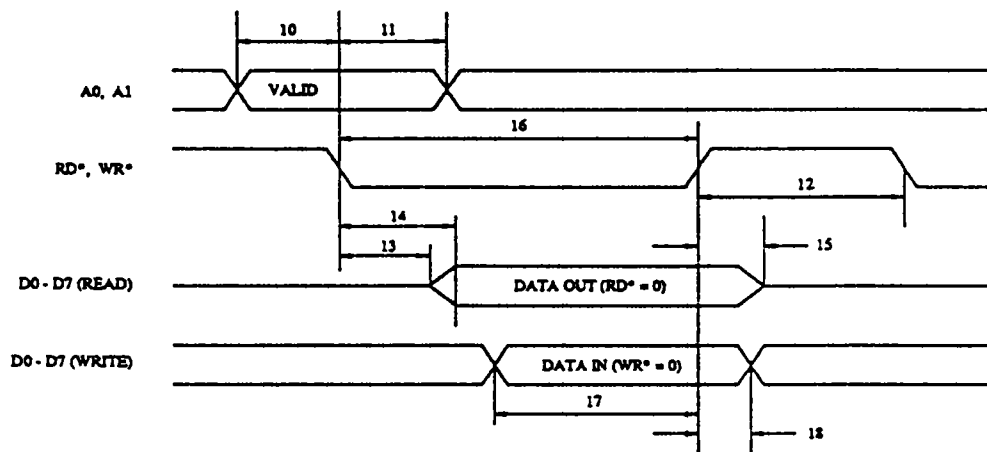**For typical A/D SNR of 41 dB (see Figure 6).
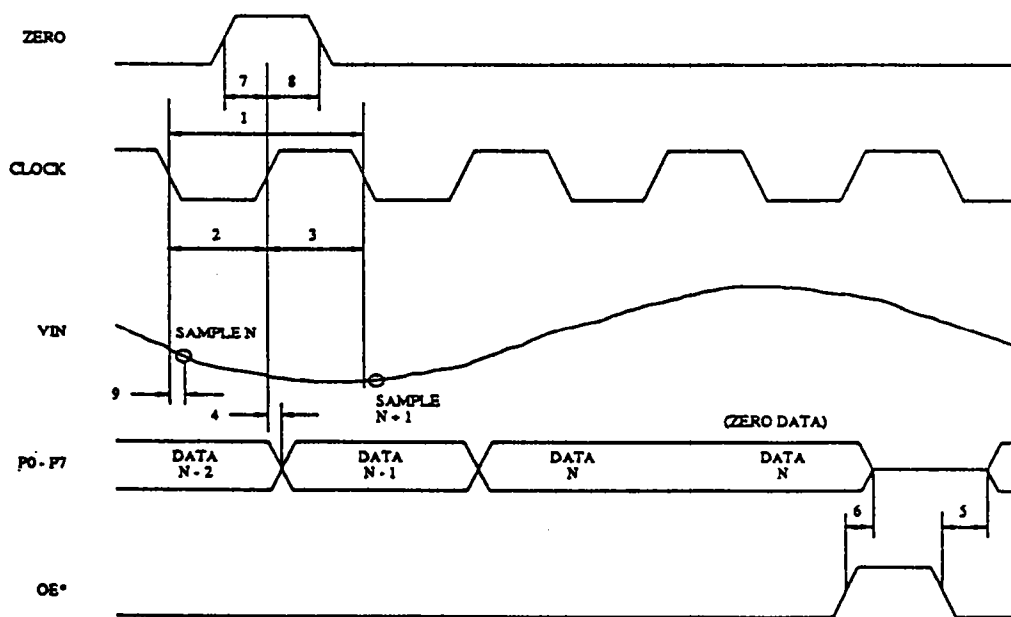
Timing Waveforms

Figure 7.   MPU Read/Write Timing.
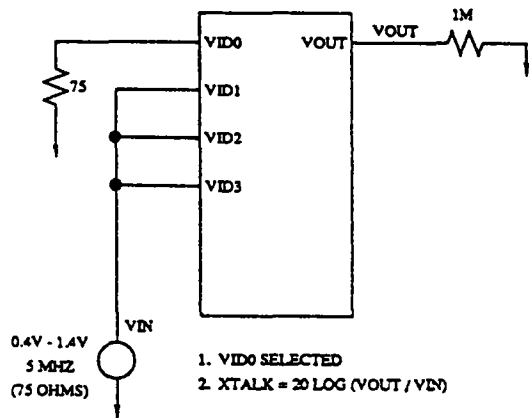

Figure 8.   Video Input/Output Timing.

Test Circuits

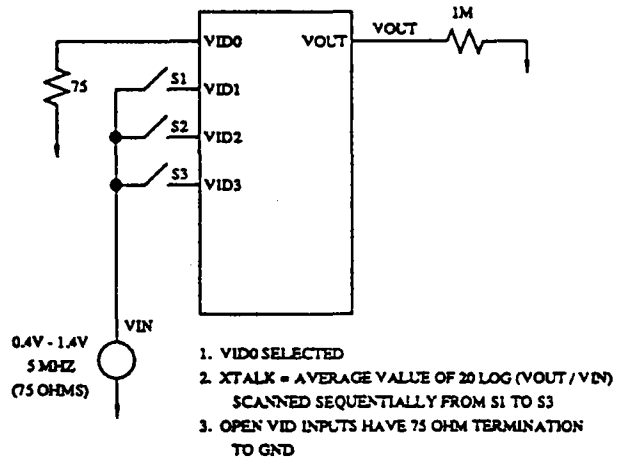**Figure 9.** *All Hostile Crosstalk Test Circuit.*
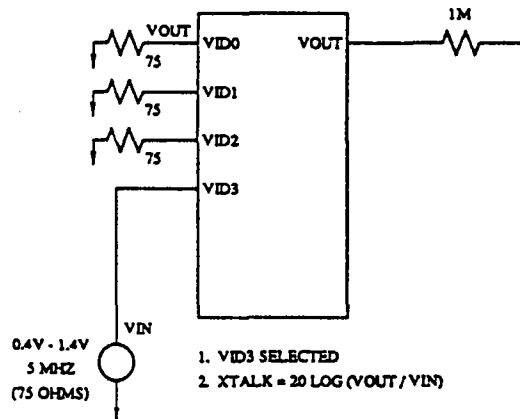

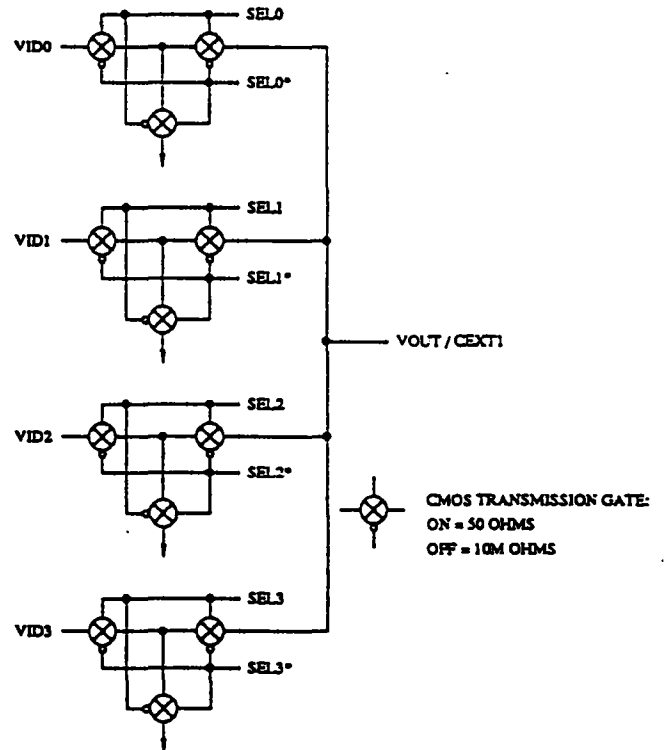**Figure 10.** *Single Channel Crosstalk Test Circuit.*

Figure 11. *Adjacent Input Crosstalk Test Circuit.*

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Ordering Information

Model Number	Package	Ambient Temperature Range
Bt251KPJ	44-pin Plastic J-Lead	0° to +70° C.
Bt251EVM	Bt251 Evaluation Board (includes Bt251KPJ)	

Analog Multiplexer Circuit
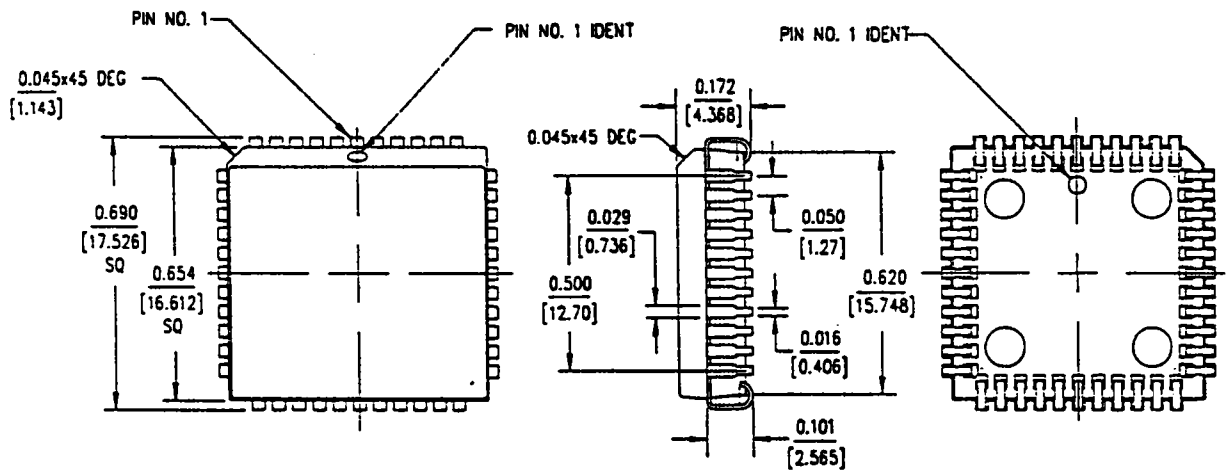
Revision History

Revision   *Change from Previous Revision*

E   Speed increased to 18 MSPS. production pinout added. AC and DC characteristics have "tbds" replaced with numbers.

Package Drawing -- 44-pin Plastic J-Lead

Notes -- Unless Otherwise Specified:

1. Dimensions are in inches [millimeters].
2. Tolerances are: x.xxx ± 0.005 [0.127]
3. This PLCC package is intended for surface mounting on solder lands on 0.050 [1.27] centers.

CAUTION

ESD sensitive device. Permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
Do not insert this device into powered sockets.
Remove power before insertion or removal.

Brooktree®

Bt261

30 MHz Pixel Clock Monolithic CMOS HSYNC Line Lock Controller

Distinguishing Features

- Programmable 12-Bit Video Timing
- Bidirectional HSYNC and CLOCK Pins
- Horizontal Sync Noise Gating
- External VCO Support
- Standard MPU Interface
- TTL Compatible
- + 5 V Monolithic CMOS
- 28-pin PLCC Package
- Typical Power Dissipation: 300 mW

Applications

- Image Processing
- Video Digitizing
- Desktop Publishing
- Graphic Art Systems

Product Description

The Bt261 HSYNC Line Lock Controller is designed specifically for image capture applications.

Either composite video or TTL composite sync information is input via VIDEO. An internal sync separator separates horizontal and vertical sync information. Programmable horizontal and vertical video timing enables recovery of both standard and non-standard timing information.

An external VCO may be used in conjunction with the on-chip phase comparator for implementation of clocks locked to the horizontal frequency.

Alternately, a high speed clock (OSC) may be divided down to generate the pixel clock. The OSC inputs may be configured to be either TTL or ECL compatible. Thus, four TTL clocks, two TTL clocks and one differential ECL clock, or two differential ECL clocks may be used. The ECL clock inputs are designed to be driven by 10KH ECL using a single +5 V supply. The higher the OSC clock rate, the lower the pixel clock jitter.

The CLAMP and ZERO outputs are programmed by the MPU for DC restoration of the video signal and zeroing the Image Digitizer or A/D converter at the appropriate time.

Functional Block Diagram
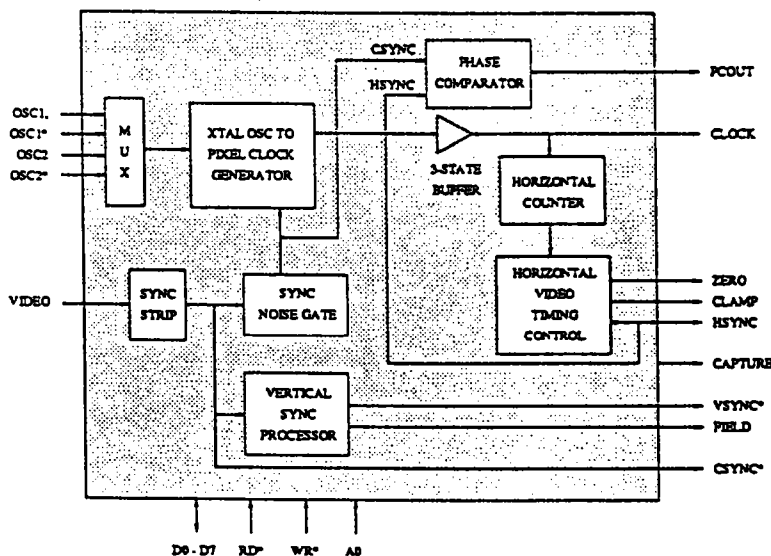
Brooktree®

Circuit Description

MPU Interface

As seen in the functional block diagram, the Bt261 supports a standard MPU interface (D0–D7, RD*, WR*, and A0). MPU operations are asynchronous to the clocks.

A0 is used to select either the internal 5-bit address register (A0 = logical zero) or the control register specified by the address register (A0 = logical one). ADDR5–ADDR7 are ignored during MPU write cycles, and are in an unknown state when read by the MPU. ADDR0 corresponds to D0 and is the least significant bit. ADDR0–ADDR4 increment following any MPU

read or write cycle to a control register other than the address register. MPU write cycles to reserved addresses are ignored and MPU read cycles from reserved addresses return invalid data.

Table 1 shows the internal register addressing.

Video Input / Sync Detector

Either an AC-coupled video signal or a DC-coupled TTL-compatible composite sync signal may be input via the VIDEO input pin (negative going sync polarity).

Command register_0 specifies the threshold above the sync tip to use for sync detection. If the sync tip on VIDEO is below the selected threshold, composite sync information is detected and output onto CSYNC* with no pipeline delay and asynchronous to the pixel clock.

Typically, the VIDEO input will be connected to the TTL-compatible CSYNC* output of the Bt251/253 Image Digitizer, and the highest sync slicing level will be selected.

Horizontal Counter

The rising edge of pixel clock (CLOCK) increments a 12-bit horizontal counter used to generate horizontal video timing information. The value of the counter is compared to various registers to determine when signals are to be asserted and negated. $000 corresponds to the falling edge of CSYNC* with a variable pipeline delay.

Horizontal Sync Separation

The Bt261 separates horizontal sync information from CSYNC* by use of the horizontal noise gate register, which derives gated composite sync by removing equalization and serration pulses at half-line intervals.

Two 12-bit noise gate start and stop registers specify at what horizontal count (with pixel clock resolution) to open and close sync transitions on the VIDEO input to be detected.

ADDR0 - ADDR4	Addressed by MPU
$00	command register_0
$01	command register_1
$02	command register_2
$03	command register_3
$04	VSYNC sample register
$05	OSC count low register
$06	OSC count high register
$07	status register
$08	HSYNC start low register
$09	HSYNC start high register
$0A	HSYNC stop low register
$0B	HSYNC stop high register
$0C	CLAMP start low register
$0D	CLAMP start high register
$0E	CLAMP stop low register
$0F	CLAMP stop high register
$10	ZERO start low register
$11	ZERO start high register
$12	ZERO stop low register
$13	ZERO stop high register
$14	FIELD gate start low register
$15	FIELD gate start high register
$16	FIELD gate stop low register
$17	FIELD gate stop high register
$18	noise gate start low register
$19	noise gate start high register
$1A	noise gate stop low register
$1B	noise gate stop high register
$1C	HCOUNT start low register
$1D	HCOUNT start high register
$1E	reserved
$1F	reserved

Table 1. Internal Register Addressing.

Circuit Description (continued)

External VCO Pixel Clock Generation

An external VCO or pixel clock may be used to drive the Bt261, as shown in Figure 2. The pixel clock signal (from the VCO if one is used) is connected to the CLOCK pin and any one of the OSC input pins (the one used must be selected by command bits CR00–CR02). Note that the VCO must have positive control voltage (positive voltage forces a higher frequency).

An on-chip phase comparator is available to compare the phase of HSYNC and the falling edge of the noise-gated CSYNC*.

If the falling edge of the noise-gated CSYNC* occurs before the beginning of HSYNC, the phase comparator "dumps" a charge onto an external capacitor, increasing the VCO frequency. If the falling edge of noise-gated CSYNC* occurs after the beginning of HSYNC, the phase comparator "sinks" a charge from the external capacitor, decreasing the VCO frequency.

The output of the phase comparator is PCOUT and it is a TTL-compatible three-statable output. The width of the output pulse on PCOUT is equal to the phase difference with a gain of 4π / VCC.
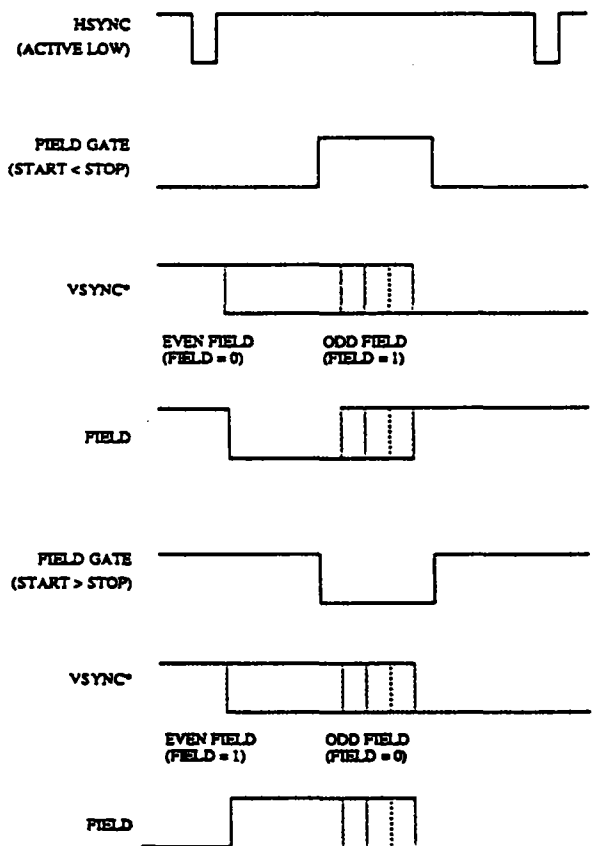

Figure 1. FIELD Output Operation.

Circuit Description (continued)

The "divide-by-N" for the PLL loop is the 12-bit HCOUNT register. Command register bits CR07 and CR06 must be set to (1,0) for proper operation. This configures the horizontal counter to be reset to zero upon reaching the HCOUNT value.

Phase/Frequency Detector Operation

The phase comparator compares the phase of the falling edge of the noise-gated CSYNC* and generated HSYNC. The HSYNC can be either internally generated (and optionally output onto the HSYNC pin) or an external HSYNC signal can be input via the HSYNC pin.

In the event of a missing horizontal sync (either recovered or generated), the phase comparator can be configured to ignore the missing pulse and to not adjust the frequency of the VCO. This phase limiting avoids adjusting the VCO frequency erroneously due to the large phase error that would otherwise occur until the next sync interval. Command bit CR10 enables or disables this capability.

If the falling edge of the noise-gated CSYNC* and generated HSYNC are within the number of pixel clock cycles specified by command bits CR24-CR27 (1 to 16 clock cycles), the Bt261 considers itself locked to the video signal. If the clock cycle condition (as specified by command bits CR24-CR27) is not met, status bit SR00 is set to low to indicate locking to the video signal was lost. If the line count condition (as specified by command bits CR30-CR37) is not met, the phase limiter is disabled.

In the event lock is lost, phase limiting is disabled until lock is re-established. Command bit CR22 may be used to override this feature to tell the phase comparator it is always locked.

Asynchronous (non-line locked) Pixel Clock Generation

Four oscillator clock inputs are provided (OSC), selectable by the MPU, configurable as either TTL or differential ECL inputs (designed to be driven by 10KH ECL using a single +5 V supply).

The selected OSC input is divided down to the desired pixel clock rate and duty cycle. The pixel clock low and high times are programmable by the MPU (as a function of OSC clock cycles) via the OSC count low and high registers. Note that both the rising and falling edge of the OSC inputs are used when specifying the OSC count (for example, values of 2 for the OSC count low and high registers will divide the OSC clock symmetrically by two).

The generated pixel clock is synchronized to the falling edge of the noise-gated CSYNC* each scan line. Each time a horizontal sync is detected on the VIDEO input, the CLOCK output is resynchronized by the OSC clock so that the beginning of a pixel clock cycle and the falling edge of the noise-gated CSYNC* are coincident (see Figure 3) within a period of the OSC input. While there is some sampling jitter on CLOCK associated with the falling edge of CSYNC*, the residual jitter in the remaining line interval is strictly a function of the OSC clock source
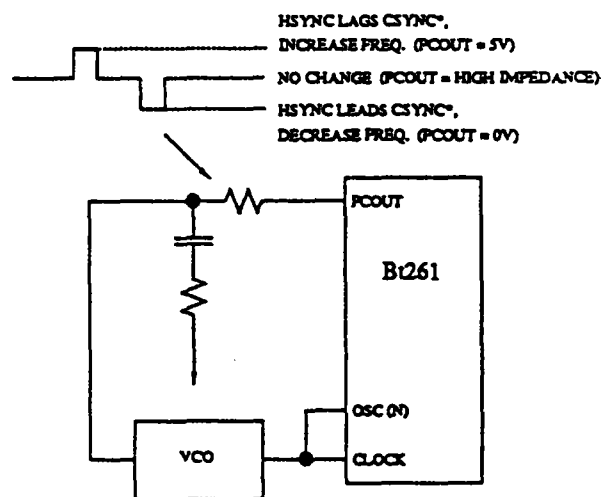

Figure 2. External VCO Configuration.

Circuit Description (continued)

jitter, and amplitude/slew rate jitter, at the OSC input. Differential OSC signals of fast edges will minimize the latter contribution.

There are three ways of controlling the horizontal counter, as determined by command bit CR07 and CR06.

CR07 and CR06 are (0,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter stops at the HCOUNT value and is held there until the next falling edge of the noise-gated CSYNC*, at which time it is reset to zero. CLOCK stops in the high state at the HCOUNT value, until the next falling edge of the noise-gated CSYNC*.

If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero by the falling edge of the noise-gated CSYNC*. CLOCK will be continuous and is resynchronized to each falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is known and is a fixed number.

CR07 and CR06 are (1,1): if a falling edge of the noise-gated CSYNC* does not occur before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is reset to zero upon reaching HCOUNT, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK is continuous and is resynchronized to each falling edge of the noise-gated CSYNC*.

If a falling edge of the noise-gated CSYNC* occurs before the number of pixel clock cycles specified by HCOUNT, the horizontal counter is cleared at the falling edge of the noise-gated CSYNC*, and begins incrementing again, until the next falling edge of the noise-gated CSYNC* or HCOUNT value is reached. CLOCK will be continuous and is resynchronized to the falling edge of the noise-gated CSYNC*. This mode is used if the number of pixel clock cycles per scan line is not known or an arbitrary value is to be used.

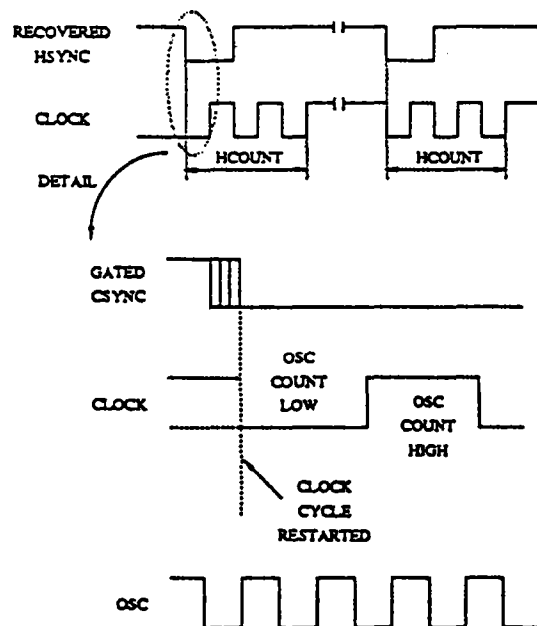CR07 and CR06 are (1,0): Resets H counter at HCOUNT only.

Figure 3. Pixel Clock Output Timing (Crystal-Based Clock).

Internal Registers

Horizontal Counter

The 12-bit horizontal counter is incremented on the rising edge of CLOCK. It is not accessible by the MPU.

Command Register_0

This command register may be written to or read by the MPU at any time and is not initialized. CR00 corresponds to D0 and is the least significant bit.

CR07, CR06	Horizontal counter control	A value of (01) or (11) forces the horizontal counter to be reset to zero at the beginning of every recovered horizontal sync. These modes (typically mode 01) should be selected when using crystal-based pixel clock generation.

(00) reserved
(01) reset each recovered HSYNC
(10) reset to zero upon reaching HCOUNT
(11) use both modes (01) and (10)

A value of (10) specifies that the horizontal counter will be reset to zero upon reaching the HCOUNT value. This mode should be selected when using the horizontal counter as a simple divide-by-N circuit (such as when using an external VCO).

CR05 Capture strobe

This bit is synchronized to VSYNC* and FIELD and output onto the CAPTURE output pin.

CR04, CR03 Sync detect select

(00) 25 mV
(01) 50 mV
(10) 100 mV
(11) 125 mV

These bits specify how much above the sync tip to slice VIDEO for sync detection. If inputting TTL sync information, the highest slicing level should be selected.

CR02–CR00 Clock input select

(000) TTL compatible OSC1
(001) TTL compatible OSC1*
(010) TTL compatible OSC2
(011) TTL compatible OSC2*
(100) ECL compatible OSC1, OSC1*
(101) ECL compatible OSC2, OSC2*
(110) reserved
(111) reserved

These bits specify which OSC input is to be used to generate pixel clock information. ECL input selection is compatible with 10KH differential ECL driven by a single +5 V supply.

Internal Registers (continued)

Command Register_1

This command register may be written to or read by the MPU at any time and is not initialized. CR10 corresponds to D0 and is the least significant bit.

CR17	Interlaced or noninterlaced select	This bit specifies whether an interlaced or noninterlaced video signal is being digitized. The MPU must write a logical zero followed by a logical one to this bit to reset the status bit (SR00) to a logical one.
	(0) noninterlaced operation	
	(1) interlaced operation	

CR16	CLOCK output disable	This bit specifies whether the CLOCK pin is three-stated (logical one) or is actively driven (logical zero). A logical one enables an external pixel clock to drive the internal counters, ignoring the OSC inputs and pixel clock generator.
	(0) drive CLOCK output	
	(1) three-state CLOCK output	

CR15	CSYNC* output disable	This bit specifies whether the CSYNC* output is three-stated (logical one) or is actively driven (logical zero).
	(0) drive CSYNC* output	
	(1) three-state CSYNC* output	

CR14	VSYNC* output disable	This bit specifies whether the VSYNC* output is three-stated (logical one) or is actively driven (logical zero).
	(0) drive VSYNC* output	
	(1) three-state VSYNC* output	

CR13	HSYNC output disable	This bit specifies whether the HSYNC output is three-stated (logical one) or is actively driven with the internally generated HSYNC signal (logical zero). If external circuitry is driving the HSYNC pin, this bit must be set to a logical one.
	(0) drive HSYNC output	
	(1) three-state HSYNC output	

Internal Registers (continued)

Command Register_1 (continued)

CR12   Reset lock loss status bits

        (0) reset status bits
        (1) inactive

This bit resets the status bits indicating loss of lock. The MPU must write a logical zero to this bit to clear the status bits (SR05 and SR00) to a logical zero.

CR11   Phase comparator input select

        (0) HSYNC pin
        (1) internally generated HSYNC

One input to the phase comparator is recovered composite sync. The other input to the phase comparator is specified by this bit to be either the internally generated HSYNC or the HSYNC pin. When an external source is driving the HSYNC pin, this bit should be set to a logical zero.

CR10   Phase limit enable

        (0) inhibit phase limiting
        (1) enable phase limiting

If this bit is a logical one, both horizontal sync signals (recovered and either internally or externally generated) must be present to adjust the VCO frequency. If one is missing, the VCO frequency is not adjusted. If this bit is a logical zero, a missing horizontal sync signal will adjust the VCO frequency.

Internal Registers (continued)

Command Register_2

This command register may be written to or read by the MPU at any time and is not initialized. CR20 corresponds to D0 and is the least significant bit.

CR27–CR24   Phase lock pixel count

        (0001)   2 clock cycles
            :
        (1111)   16 clock cycles

These bits specify the maximum number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal (either internally or externally generated) to be considered locked.

If the number of pixel clock cycles between the falling edge of noise-gated CSYNC* and the HSYNC signal exceed this value, lock is considered to be lost for that scan line, and the lock loss status bit (SR00) is set to a logical zero.

CR23   Pixel clock mask enable

        (0)   continuous pixel clock
        (1)   stop pixel clock at HCOUNT

If this bit is a logical one, the CLOCK output is stopped in the logical one state when the horizontal counter reaches the HCOUNT value. This ensures a minimum pulse width when the noise-gated CSYNC* signal is asynchronously sampled. If it is a logical zero, the CLOCK output will continuously clock (if command bit CR16 is a logical zero). This bit is ignored if an external pixel clock is driving the CLOCK pin (command bit CR16 is a logical one).

CR22   Lock override

        (1)   normal operation
        (0)   tell phase comparator it's locked

If the Bt261 goes out of lock, the phase limiter is automatically disabled until it is back in lock. If this bit is a logical zero, this function is overridden.

CR21, CR20   Pixel clock select

        (00)   OSC inputs
        (01)   external pixel clock
        (10)   OSC drives CLOCK direct
        (11)   reserved

These bits specify whether to use the OSC-generated pixel clock or an external pixel clock (driving the CLOCK pin) to clock internal counters.

In mode (00), the selected OSC input(s) is divided down by the OSC count registers to generate the pixel clock (CLOCK).

If mode (01) is selected, an external pixel clock must drive the CLOCK pin and one of the OSC inputs. Command bit CR16 must be a logical one.

If mode (10) is selected, the OSC clock is output directly onto the CLOCK pin. The OSC count low and high registers are ignored.

Internal Registers (continued)

Command Register_3

This command register may be written to or read by the MPU at any time and is not initialized. CR30 corresponds to D0 and is the least significant bit.

CR37–CR30   Phase lock line count

(0000 0000) 1 scan line

(0000 0001) 2 scan lines

:

(1111 1111) 256 scan lines

These bits specify the number of consecutive scan lines for which lock must be maintained. If lock is not maintained for the specified number of scan lines, the phase limiter is disabled only if command bit CR22 is a logical one.

VSYNC Sample Register

This 8-bit register specifies the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to sample the CSYNC* signal each scan line. This register may be written to or read by the MPU at any time and is not initialized. Values from $00 (1) to $FF (256) may be specified. A value of [1/4 HCOUNT] is recommended (greater than the maximum horizontal sync pulse width of about 5 µS). For a conventional video input with negative-going syncs, this produces a negative-going VSYNC* at the number of clock cycles specified after the falling CSYNC* edge with some pipeline delay.

OSC Count Low and High Registers

These two 4-bit registers specify the number of rising and falling edges of an OSC input the pixel clock output (CLOCK) is to be low and high. Values from $02 (2) to $0E (15) may be specified. These registers may be written to or read by the MPU at any time and are not initialized. A value of $00 results in no pixel clock generation while the OSC inputs are used. Note that the counters clock on both the rising and falling edge of the selected OSC input.

Status Register

This status register may be read by the MPU at any time and is not initialized. MPU write cycles to this register are ignored. SR00 corresponds to D0 and is the least significant bit.

SR00   Lock loss status (pixel count related)

(0) lock loss detected
(1) reset or no lock loss

This bit is reset if loss of lock occurred for a period defined by CR24–CR27. It is reset by writing to command bit CR12.

Internal Registers (continued)

HSYNC Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the HSYNC output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that the HSYNC output is set low. If [start value] = [stop value], HSYNC will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and HSYNC outputs.

D4–D7 of HSYNC start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC start register is not updated until the write cycle to the HSYNC start high register. Thus, the writing sequence should be [HSYNC start low] [HSYNC start high].

D4–D7 of HSYNC stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HSYNC stop register is not updated until the write cycle to the HSYNC stop high register. Thus, the writing sequence should be [HSYNC stop low] [HSYNC stop high].

	HSYNC Start/Stop High				HSYNC Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

CLAMP Start and Stop Registers

These two 16-bit registers specify the horizontal count (in pixel clocks) at which to assert and negate the CLAMP output. The [start value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set high. The [stop value] specifies the number of CLOCK cycles after the falling edge of noise-gated CSYNC* that CLAMP is set low. If [start value] = [stop value], CLAMP will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and CLAMP outputs.

D4–D7 of CLAMP start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP start register is not updated until the write cycle to the CLAMP start high register. Thus, the writing sequence should be [clamp start low] [clamp start high].

D4–D7 of CLAMP stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit CLAMP stop register is not updated until the write cycle to the CLAMP stop high register. Thus, the writing sequence should be [clamp stop low] [clamp stop high].

	CLAMP Start/Stop High				CLAMP Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A value corresponding to 1 µS after the falling edge of CSYNC* is recommended for the [start] value, and a value of 1 µS before the rising edge of CSYNC* is recommended for the [stop] value if DC restoration is to occur during the horizontal sync interval. If DC restoration is to occur during the back porch interval, a value corresponding to 500 ns after the rising edge of CSYNC* is recommended for the [start] value and a value corresponding to 2.5 µS after the rising edge of CSYNC* is recommended for the [stop] value.

Internal Registers (continued)

ZERO Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to assert or negate the ZERO output. The [start value] sets this output high at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. The [stopvalue] sets this output low at the specified number of CLOCK cycles following the falling edge of noise-gated CSYNC*. If [start value] = [stop value], ZERO will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Note that there is a variable pipeline delay between the CSYNC* and ZERO outputs.

D4–D7 of ZERO start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO start register is not updated until the write cycle to the ZERO start high register. Thus, the writing sequence should be [zero start low] [zero start high].

D4–D7 of ZERO stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit ZERO stop register is not updated until the write cycle to the ZERO stop high register. Thus, the writing sequence should be [zero stop low] [zero stop high].

	ZERO Start/Stop High				ZERO Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Since an active high signal is need for the Bt208, Bt251, and Bt253 during non-acquisition intervals, the ZERO output can be programmed to be within the horizontal retrace interval.

Internal Registers (continued)

FIELD Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to start and stop the FIELD gate "window." With the noise gate properly programmed to ignore half-line vertical interval pulses, the VSYNC* transition will occur half a line later during the vertical sync interval between fields one and two (assuming a typical 2:1 interlaced video signal). By programming the FIELD start and stop values to have an interval exceeding half a line (e.g. starting at 1/4 line time and stopping at 3/4 line time) the FIELD output is high during field one if [start value] < [stop value] or low during field one if [start value] > [stop value], with transitions at every falling edge of VSYNC*. If [start value] = [stop value], FIELD will remain a constant logical zero. Values from $0000 (1) to $0FFF (4096) may be specified. Field edge coincides with VSYNC* falling edge.

D4–D7 of FIELD gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate start register is not updated until the write cycle to the FIELD gate start high register. Thus, the writing sequence should be [field gate start low] [field gate start high].

D4–D7 of FIELD gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit FIELD gate stop register is not updated until the write cycle to the FIELD gate stop high register. Thus, the writing sequence should be [field gate stop low] [field gate stop high].

	FIELD Gate Start/Stop High				FIELD Gate Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A difference between [start] and [stop] greater than [HCOUNT/2] is recommended, resulting in an active high FIELD output (field one = 1, field two = 0).

Internal Registers (continued)

Noise Gate Start and Stop Registers

These two 16-bit registers specify the number of pixel clock cycles after the falling edge of noise-gated CSYNC* at which to force the Noise Gate to be closed (start value) or open (stop value). If [start value] = [stop value], the Noise Gate will remain open. Values from $0000 (1) to $0FFF (4096) may be specified.

D4–D7 of Noise Gate start high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit Noise Gate start register is not updated until the write cycle to the Noise Gate start high register. Thus, the writing sequence should be [Noise Gate start low] [Noise Gate start high].

D4–D7 of Noise Gate stop high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit Noise Gate stop register is not updated until the write cycle to the Noise Gate stop high register. Thus, the writing sequence should be [Noise Gate stop low] [Noise Gate stop high].

	Noise Gate Start/Stop High				Noise Gate Start/Stop Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

A value corresponding to [HCOUNT/2 – 2.5 µS] is recommended for the [start] value and a value of [> HCOUNT/2] is recommended for the [stop] value to remove typical equalization and serration pulses. This register should be initialized early to minimize indeterminate outputs during vertical retrace.

HCOUNT Register

This 16-bit register specifies the maximum number of pixel clocks to generate per horizontal line.

The HCOUNT low and high registers are cascaded to form a 16-bit HCOUNT register. D4–D7 of HCOUNT high are ignored during MPU write cycles and return a logical zero during MPU read cycles. The 16-bit HCOUNT register is not updated until the write cycle to the HCOUNT high register. Thus, the writing sequence should be [HCOUNT low] [HCOUNT high]. Values from $0000 (1) to $0FFF (4096) may be specified. This register should be written first during initialization to minimize indeterminate output activity.

|	HCOUNT High				HCOUNT Low							
Data Bit	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Cascaded Value	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0

Pin Descriptions

Pin Name	Description
HSYNC	Horizontal sync input/output (TTL compatible). As an output, HSYNC is programmed to be either a logical zero or logical one during the desired horizontal sync interval. It is output following the rising edge of CLOCK. As an input, it is input into the phase comparator asynchronously to the clocks with no pipeline delays.
VSYNC*	Vertical sync output (TTL compatible) with a negative composite sync output. VSYNC* is a logical zero for scan lines during detected vertical sync intervals on the VIDEO input. It is output following the rising edge of CLOCK.
CSYNC*	Composite sync output (TTL compatible). CSYNC* is a logical zero during negative composite sync intervals detected on the VIDEO input. It is output asynchronous to the clocks with no pipeline delays.
ZERO	Zero output (TTL compatible). This output is used to control the ZERO input of the Image Digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
CLAMP	Clamp output (TTL compatible). This output is used to control the CLAMP input of the Image Digitizer or A/D converter. It may be programmed to be either active high or active low and is output following the rising edge of CLOCK.
FIELD	Even/odd field output (TTL compatible). For interlaced operation, this output (with transitions coincident with the VSYNC* output) indicates whether the current field is even or odd; the polarity is programmable. For noninterlaced operation, this output is always either a logical one or a logical zero, depending on whether it is programmed to be active high or low. It is output on the falling edge of VSYNC*.
PCOUT	Phase comparator output (TTL compatible). This three-state output indicates the phase difference in time between the generated horizontal sync signal (either the internally generated HSYNC or the HSYNC pin) and the recovered horizontal sync signal. High = lags, Low = leads.
VIDEO	Video and composite sync input. Either a DC-coupled TTL composite sync information or an AC-coupled analog video signal (less than 2v peak-to-peak) may be input via this pin for detection of sync information. Sync information must be of negative polarity.
CLOCK	Pixel clock input/output (TTL compatible). The device may either drive this pin with a generated clock or an external pixel clock may drive this pin.
OSC1, OSC1*, OSC2, OSC2*	External clock inputs (TTL or ECL compatible). These inputs are programmed to be either TTL or ECL compatible (10KH differential ECL driven by a single +5 V supply).
CAPTURE	Active video output (TTL compatible). This output is active high for a frame duration and is synchronized to the vertical sync interval and FIELD signal. It is output following the rising edge of FIELD for interlaced, or the falling edge of VSYNC* if non-interlaced.
RD*	Read control input (TTL compatible). If RD* is a logical zero, data is output onto D0–D7. RD* and WR* should not be asserted simultaneously.
WR*	Write control input (TTL compatible). If WR* is a logical zero, data is written into the device via D0–D7. Data is latched on the rising edge of WR*. RD* and WR* should not be asserted simultaneously.
D0–D7	Bidirectional data bus (TTL compatible). MPU data is transferred into and out of the device over this 8-bit data bus. If RD* is a logical one, D0–D7 are three-stated.

Pin Descriptions (continued)

Pin Name	Description
A0	Address control inputs (TTL compatible). A0 specifies whether the MPU is accessing the address register (A0 = 0) or the control register specified by the address register (A0 = 1).
VCC	Power.
GND	Ground.
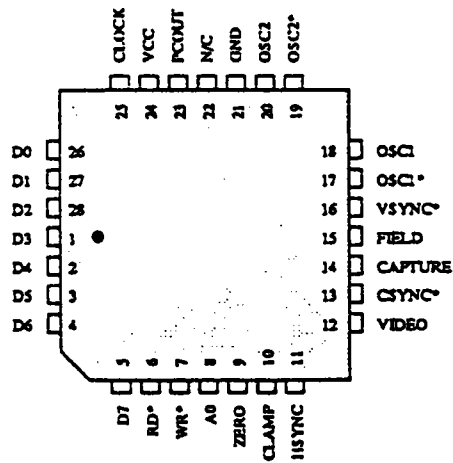
Application Information

Interfacing to the Bt208

Figure 4 illustrates interfacing the Bt261 to the Bt208 Flash A/D Converter. The VIDEO input of the Bt261 connects to the VIN input of the Bt208 through a 0.1 µF ceramic capacitor. The sync slicing level of the Bt261 should be selected for optimum performance.

The Bt261 provides the ZERO and CLAMP signals required by the Bt208, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

Figure 4. Interfacing to the Bt208.

Application Information (continued)

Interfacing to the Bt251

Figure 5 illustrates interfacing the Bt261 to the Bt251 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt251. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt251, in addition to the CLOCK.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.
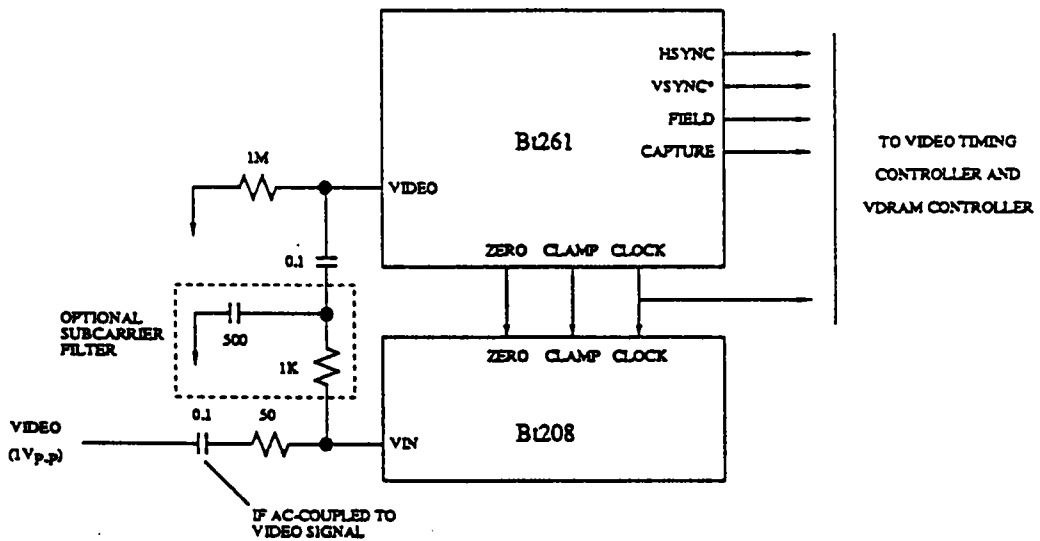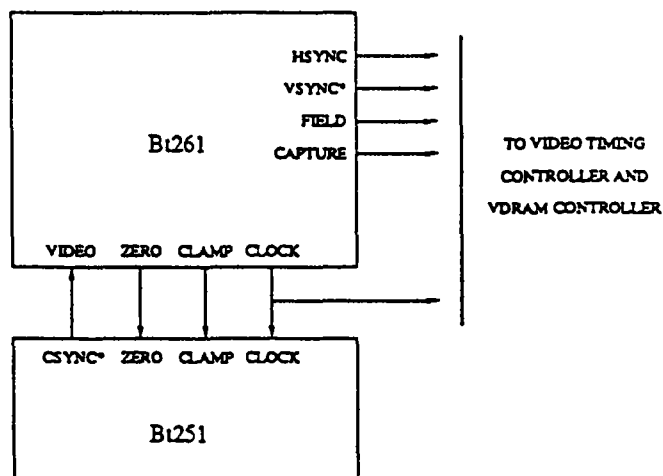

Figure 5. Interfacing to the Bt251.

Application Information (continued)

Interfacing to the Bt253

Figure 6 illustrates interfacing the Bt261 to the Bt253 Image Digitizer. The VIDEO input of the Bt261 connects directly to the CSYNC* output of the Bt253. As CSYNC* is a TTL-compatible output, the highest sync slicing level should be selected on the Bt261.

The Bt261 provides the ZERO and CLAMP signals required by the Bt253, in addition to the (R,G,B) CLOCK inputs of the Bt253.

The HSYNC, VSYNC*, FIELD, and CAPTURE signals of the Bt261 interface to the video timing controller and video DRAM controller.

ESD and Latchup Considerations

Correct ESD-sensitive handling procedures are required to prevent device damage, which can produce symptoms of catastrophic failure or erratic device behavior with somewhat "leaky" inputs.

Latchup can be prevented by assuring that all VCC pins are at the same potential and that the VCC supply voltage is applied before the signal pin voltages. The correct power-up sequence assures that any signal pin voltage will never exceed the power supply voltage by more than +0.5 V.
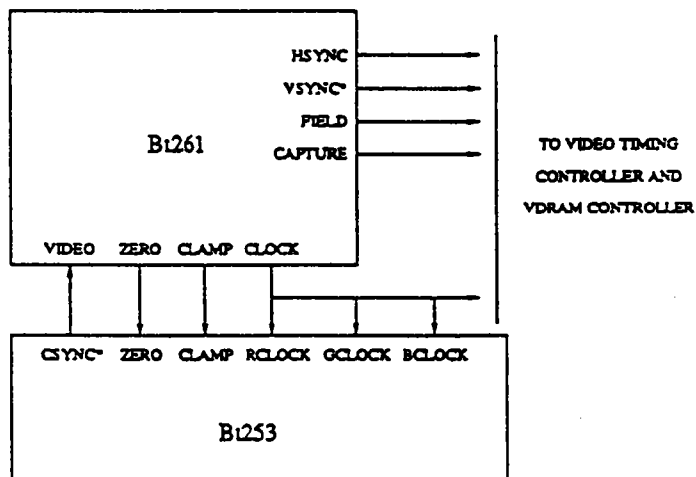

Figure 6. Interfacing to the Bt253.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power Supply	VCC	4.75	5.00	5.25	Volts
Ambient Operating Temperature	TA	0		+70	°C
Video Input					
DC-coupled				5	Volts
AC-coupled*		0.2		2	Voltspp

* Video input DC quiesent about (VCC/2) volts.

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VCC (measured to GND)		·		7.0	Volts
Voltage on any Signal Pin*		GND–0.5		VCC + 0.5	Volts
Ambient Operating Temperature	TA	–55		+ 125	°C
Storage Temperature	TS	–65		+ 150	°C
Junction Temperature	TJ			+ 150	°C
Vapor Phase Soldering (1 minute)	TVSOL			220	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device employs high impedance CMOS devices on all signal pins. It should be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V can induce destructive latchup.

DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
TTL Digital Inputs					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	μA
Input Low Current (Vin = 0.4 V)	IIL			–1	μA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		7		pF
OSC Digital Inputs					
TTL Mode					
Input High Voltage	VIH	2.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		0.8	Volts
Input High Current (Vin = 2.4 V)	IIH			1	μA
Input Low Current (Vin = 0.4 V)	IIL			–1	μA
Input Capacitance (f = 1 MHz, Vin = 2.4 V)	CIN		7		pF
ECL Mode					
Input High Voltage	VIH	VCC–1.0		VCC + 0.5	Volts
Input Low Voltage	VIL	GND–0.5		VCC–1.6	Volts
Input High Current (Vin = 4.0 V)	IIH			1	μA
Input Low Current (Vin = 0.4 V)	IIL			–1	μA
Input Capacitance (f = 1 MHz, Vin = 2.4v)	CIN		7		pF
D0 - D7 Digital Outputs					
Output High Voltage (IOH = –400 μA)	VOH	2.4			Volts
Output Low Voltage (IOL = 6.4 mA)	VOL			0.4	Volts
3-state Current	IOZ			50	μA
Output Capacitance	COUT		20		pF
PCOUT Output					
Output High Voltage (IOH = –400 μA)	VOH			100	Ω
Output Low Voltage (IOL = 3.2 mA)	VOL			75	Ω
3-state Current	IOZ			50	μA
Output Capacitance	COUT		20		pF
Other Digital Outputs					
Output High Voltage (IOH = –400 μA)	VOH	2.4			Volts
Output Low Voltage (IOL = 3.2 mA)	VOL			0.4	Volts
3-State Current	IOZ			50	μA
Output Capacitance	COUT		20		pF

Test conditions (unless otherwise specified): "Recommended Operating Conditions." Typical values are based on nominal temperature, i.e., room, and nominal voltage, i.e., 5 V.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
OSC Cycle Time	OSCmax	10			ns
CLOCK Cycle Time*	Fmax	33.33			ns
A0 Setup Time	1	10			ns
A0 Hold Time	2	10			ns
RD*/WR* Low Time	3	50			ns
RD*/WR* High Time	4	50			ns
RD* Asserted to Data Bus Driven	5	5			ns
RD* Asserted to Data Valid	6			40	ns
RD* Negated to Data Bus 3-Stated	7			20	ns
Write Data Setup Time	8	10			ns
Write Data Hold Time	9	10			ns
OSC High Time	10	3.5			ns
OSC Low Time	11	3.5			ns
CLOCK Low Time	12	tbd		tbd	ns
CLOCK High Time	13	tbd		tbd	ns
OSC to CLOCK Output Delay Pipelines	14			tbd	ns
VIDEO to CSYNC* Output Delay	15			tbd	ns
HSYNC, ZERO, CLAMP Output Delay	16			tbd	ns
VSYNC*, FIELD Output Delay Pipelines	17			tbd	ns
PCOUT Output Delay	18			tbd	ns
Minimum Compare Differential	19		5	tbd	ns
VCC Supply Current**	ICC		60	tbd	mA

Test conditions (unless otherwise specified): "Recommended Operating Conditions". TTL input values are 0–3 V, with input rise/fall times ≤ 4 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. CLOCK, HSYNC, CLAMP, ZERO, VSYNC*, FIELD, CAPTURE, and CSYNC* output load ≤ 50 pF, D0–D7 output load ≤ 130 pF. Typical values are based on nominal temperature, i.e., and nominal voltage, i.e., 5 V.

*Maximum load of 20 pf.
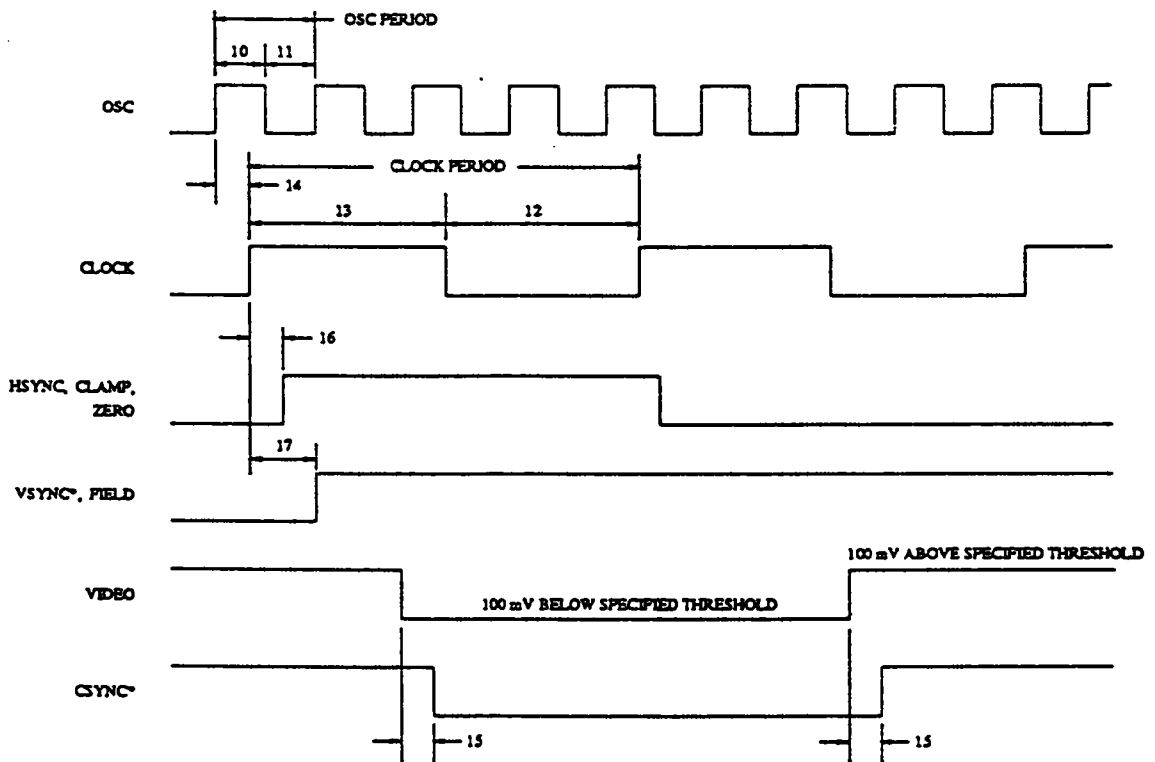**At Fmax. ICC (typ) at VCC = 5.0 V. ICC (max) at VCC = 5.25 V. OSC/PCLOCK = 2, CLOCK/HSYNC ≥100.

Timing Waveforms
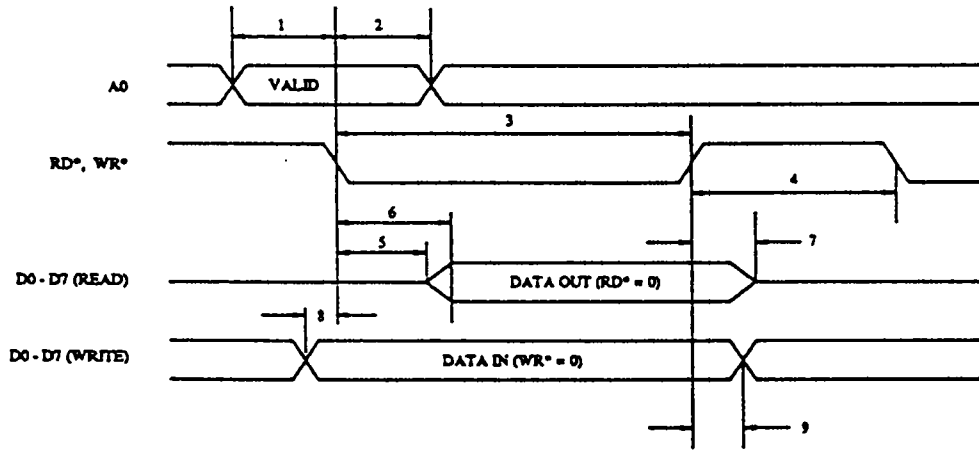
MPU Read/Write Timing.

Video Input/Output Timing.

Timing Waveforms (continued)
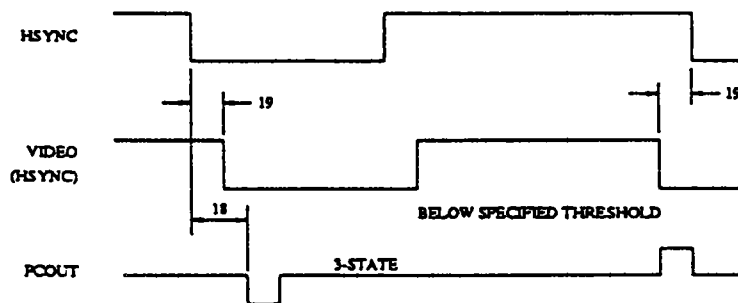
Video Input/Output Timing.

Ordering Information

Model Number	Package	Ambient Temperature Range
Bt261KPJ	28-pin Plastic J-Lead	0° to +70° C

Package Drawing—28-pin Plastic J-Lead (PLCC)
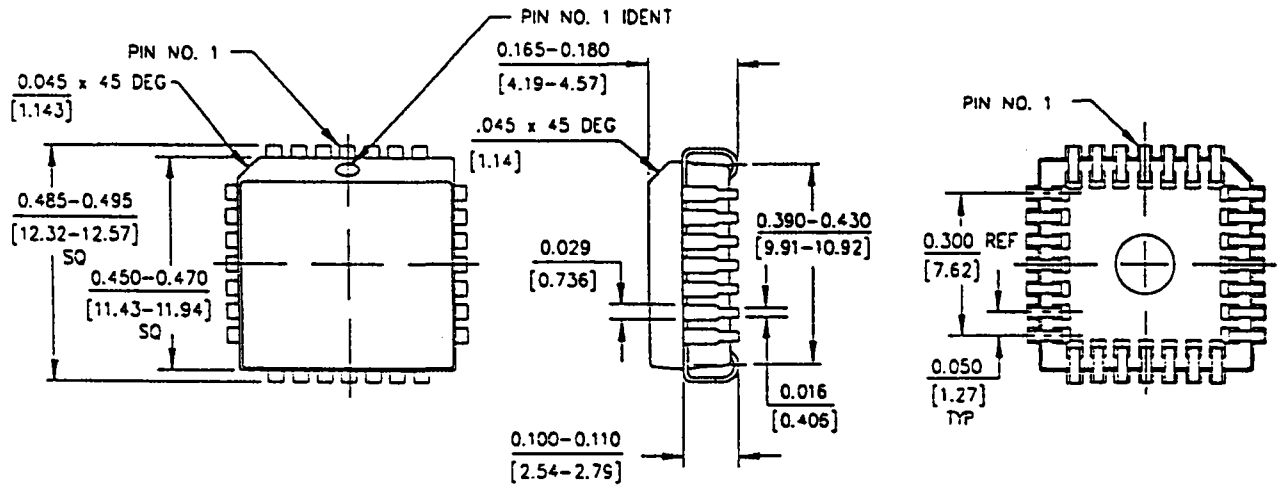
NOTES - Unless otherwise specified:
1. Dimensions are in inches [millimeters].
2. Tolerances are: .xxx ± 0.005 [0.127].
3. PLCC packages are intended for surface mounting on solder lands on 0.050 [1.27] centers.

Brooktree®

> **CAUTION**
>
> ESD sensitive device. Permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
>
> Do not insert this device into powered sockets. Remove power before insertion or removal.

◪ National Semiconductor

54ACT/74ACT715•LM1882
Programmable Video Sync Generator

General Description

The 'ACT715/LM1882 is a 20-pin TTL-input compatible device capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The device is capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

The 'ACT715/LM1882 makes no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

Features

- Maximum Input Clock Frequency > 100 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- Orderable as linear device LM1882CN or LM1882CM

Connection Diagrams

Pin Assignment for DIP, Flatpak and SOIC

D_0 — 1		20 — V_{CC}
D_1 — 2		19 — $\overline{ADDR}/DATA$
D_2 — 3		18 — $\overline{L}/HBYTE$
D_3 — 4		17 — LOAD
D_4 — 5		16 — ODD/$\overline{EVEN}$
D_5 — 6		15 — HSYNVDR
D_6 — 7		14 — VCSYNC
D_7 — 8		13 — HBLHDR
CLR — 9		12 — VCBLANK
GND — 10		11 — CLOCK
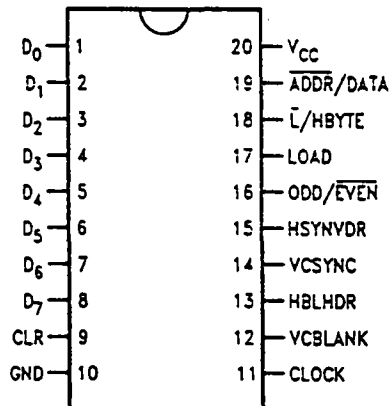
TL/F/10137-1

Pin Assignment for LCC

D_7 D_6 D_5 D_4 D_3
[8] [7] [6] [5] [4]

CLR [9]   [3] D_2
GND [10]   [2] D_1
CLOCK [11]   [1] D_0
VCBLANK [12]   [20] V_{CC}
HBLHDR [13]   [19] $\overline{ADDR}/DATA$

[14] [15] [16] [17] [18]
VCSYNC HSYNVDR ODD/$\overline{EVEN}$ LOAD $\overline{L}/HBYTE$
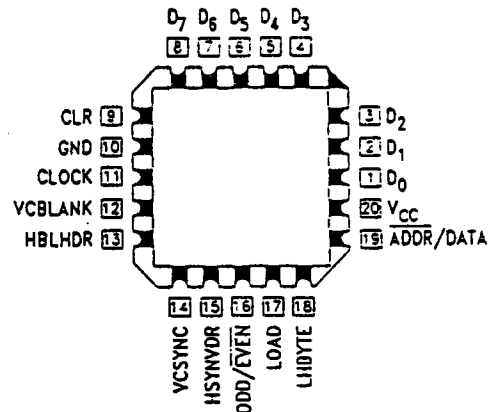
TL/F/10137-2

Logic Block Diagram

TL/F/10137-3

Pin Description

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

Data Inputs D0-D7: The Data Input pins connect to the Address Register and the Data Input Register.

$\overline{ADDR}/DATA$: The $\overline{ADDR}/DATA$ signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus.

$\overline{L}/HBYTE$: The $\overline{L}/HBYTE$ signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/ ATA is a 0 enables Auto-Load Mode.

LOAD: The Load control pin loads data into the Address or Data Registers on the rising edge. $\overline{ADDR}/DATA$ and $\overline{L}/HBYTE$ data is loaded into the device on the falling edge of the clock. The Load pin has been implemented as a Schmitt trigger input for better noise immunity.

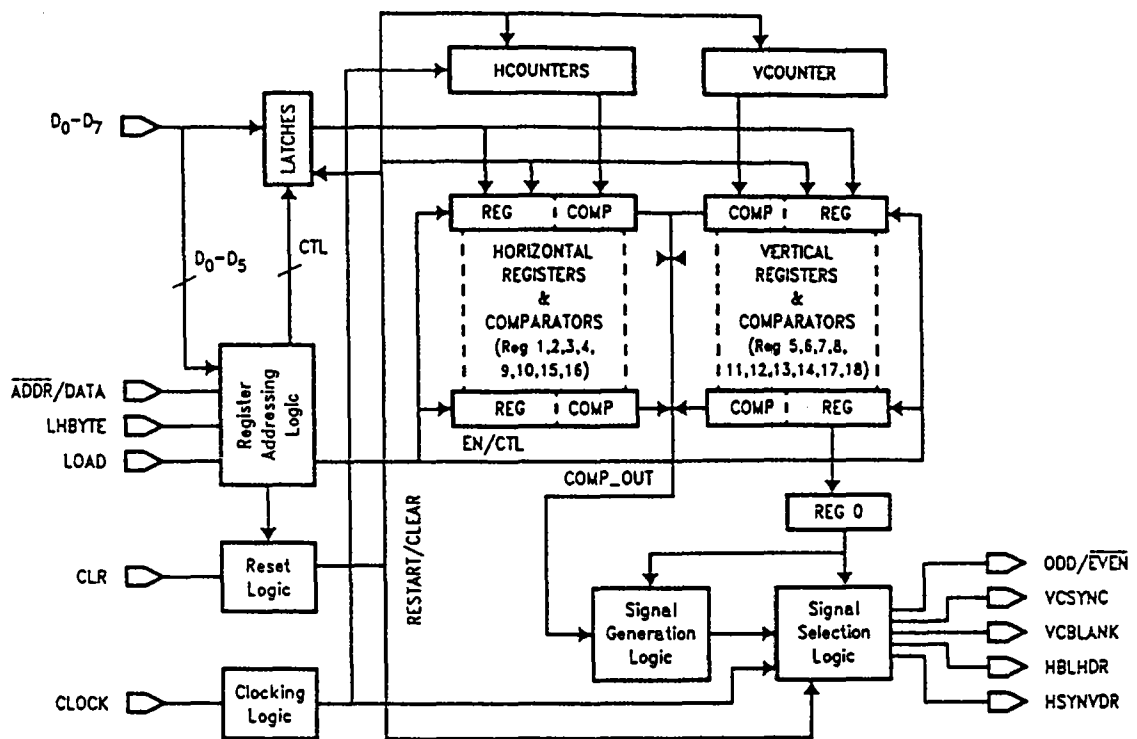CLOCK: System Clock input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity.

CLR: The Clear pin is an asynchronous input that initializes the device when it is high. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The clear pin has been implemented as a Schmitt trigger for better noise immunity.

ODD/$\overline{EVEN}$: Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this input is always HIGH. Data can be serially scanned out on nis pin during test mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register.

VCBLANK: Outputs Vertical or Composite Blanking signal based on value of the Status Register.

HBLHDR: Outputs Horizontal Blanking signal, Horizontal Gating signal or cursor position based on value of the Status Register.

HSYNVDR: Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

Register Description

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

REG0—STATUS REGISTER

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs.

Bits 0-2

B_2	B_1	B_0	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0	CBLANK	CSYNC	HGATE	VGATE
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	HGATE	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

2

Register Description (Continued)

Bits 3-4

B$_4$	B$_3$	Mode of Operation
0	0	Interlaced Double Serration and Equalization
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Bits 5-8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates a pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5— VCBLANK Polarity

B6— VCSYNC Polarity

B7— HBLHDR Polarity

B8— HSYNVDR Polarity

Bits 9-11

Bits 9 through 11 enable several different features of the vice.

B9— Enable Equalization/Serration Pulses (0)
Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0)
Enable System Clock (1)

B11— Disable Counter Test Mode (0)
Enable Counter Test Mode (1)

HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width   # of Clocks per Line

VERTICAL INTERVAL REGISTERS

The Vertical Interval Registers determine the number of es per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width   # of Lines per Frame

EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

CURSOR LOCATION REGISTERS

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals.

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

Signal Specification

HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2 × the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

Horizontal Period (HPER) $= REG(4) \times ckper$

Horizontal Blanking Width $= [REG(3) - 1] \times ckper$

Horizontal Sync Width $= [REG(2) - REG(1)] \times ckper$

Horizontal Front Porch $= [REG(1) - 1] \times ckper$

VERTICAL SYNC AND BLANK SPECIFICATION

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC.

Vertical Frame Period (VPER) $= REG(8) \times hper$

Vertical Field Period (VPER/n) $= REG(8) \times hper/n$

Vertical Blanking Width $= [REG(7) - 1] \times hper/n$

Vertical Syncing Width $= [REG(6) - REG(5)] \times hper/n$

Vertical Front Porch $= [REG(5) - 1] \times hper/n$

where n = 1 for noninterlaced
    n = 2 for interlaced

COMPOSITE SYNC AND BLANK SPECIFICATION

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The serration pulse interval occurs in place of the Vertical Sync interval. Equalization puls-

Signal Specification (Continued)

es occur preceding and/or following the serration pulses. The width and location of these pulses can be programmed through the registers shown below.

Horizontal Equalization PW = [REG(9) − REG(1)] × ckper

Horizontal Serration PW = [REG(4)/n + REG(1) − REG(10)] × ckper

Where n = 1 for noninterlaced single serration/equalization

n = 2 for noninterlaced double serration/equalization

n = 2 for interlaced operation

HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of bit 2 of the status register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) − REG(15)] × ckper

Vertical Gating Signal Width = [REG(18) − REG(17)] × hper

CURSOR POSITION AND VERTICAL INTERRUPT

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected and bit 2 of the Status Register is set to the value of 1. The cursor position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

Horizontal Cursor Width = [REG(16) − REG(15)] × ckper

Vertical Cursor Width = [REG(18) − REG(17)] × hper

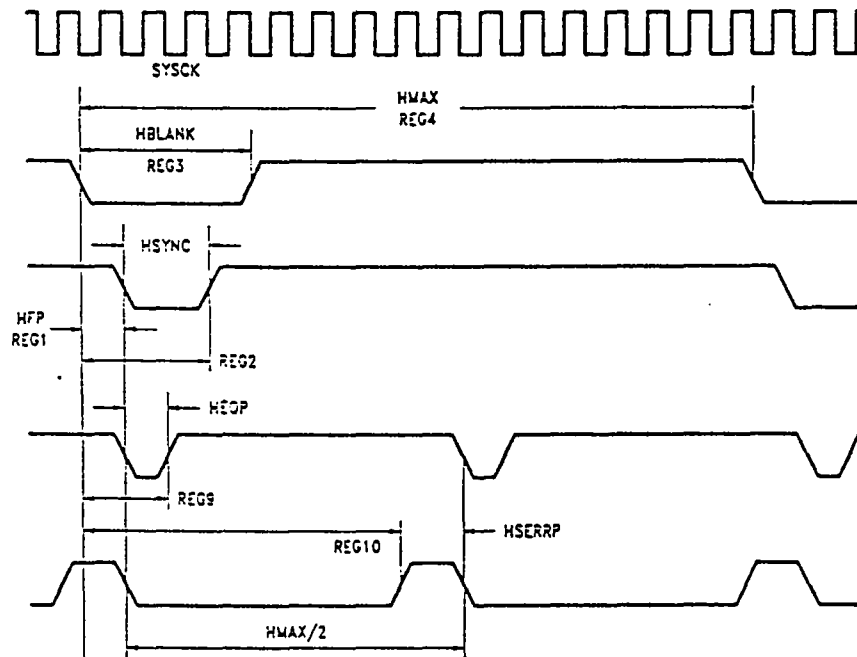Vertical Interrupt Width = [REG(14) − REG(13)] × hper

TL/F/10137–4

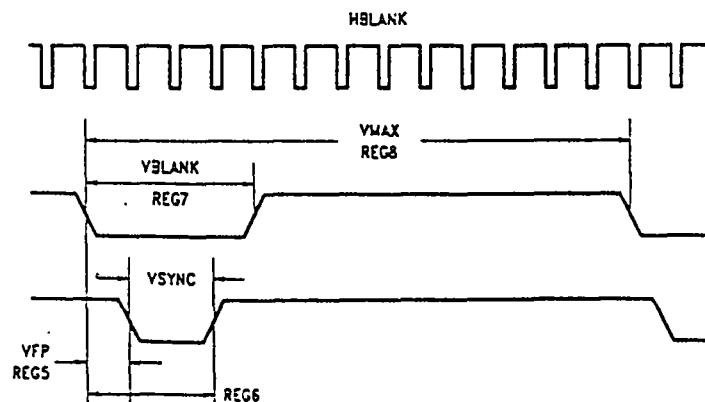**FIGURE 1. Horizontal Waveform Specification**

TL/F/10137–5

**FIGURE 2. Vertical Waveform Specification**

4

Addressing Logic

The register addressing logic is composed of two blocks of logic. The first is the address register and counter (^DDRCNTR), and the second is the address decode ^ JDRDEC).

ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 Load cycles (19 Address and 38 Data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 Load cycles to completely program all registers (1 Address and 38 Data). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of load when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of load after ADDRDATA and LHBYTE goes low.
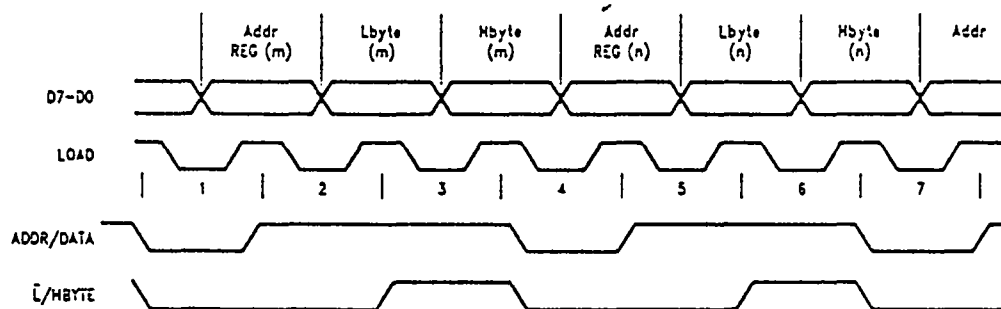
TL/F/10137-7

Manual Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Manual Addressing	Load Address m
2	Enable Lbyte Data Load	Load Lbyte m
3	Enable Hbyte Data Load	Load Hbyte m
4	Enable Manual Addressing	Load Address n
5	Enable Lbyte Data Load	Load Lbyte n
6	Enable Hbyte Data Load	Load Hbyte n
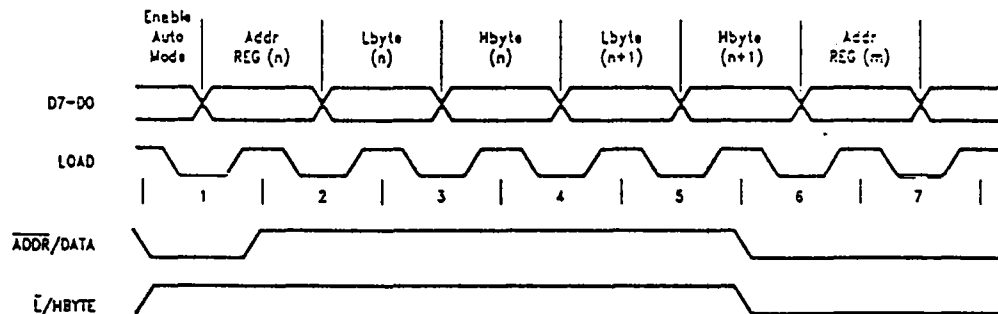
TL/F/10137-8

Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge
1	Enable Auto Addressing	Load Start Address n
2	Enable Lbyte Data Load	Load Lbyte (n)
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter
4	Enable Lbyte Data Load	Load Lbyte (n + 1)
5	Enable Hbyte Data Load	Load Hbyte (n + 1); Inc Counter
6	Enable Manual Addressing	Load Address

5

Addressing Logic (Continued)

ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and gen-
rates the enable signal for the appropriate register. The
enable values for the registers and counters change on the
falling edge of LOAD. Since the data registers are disabled
at this time any overlap of enable signals will not cause
register data to change. The following Addresses are used
by the device.

Address 0   Status Register REG0

Address 1-18   Data Registers REG1-REG18

Address 19-21   Unused

Address 22/54   Restart Vector (Restarts Device)

Address 23/55   Clear Vector (Zeros All Registers)

Address 24-31   Unused

Address 32-50   Register Scan Addresses

Address 51-53   Counter Scan Addresses

Address 56-63   Unused

At any given time only one register at most is selected. It is
possible to have no registers selected.

VECTORED CLEAR ADDRESS

Addresses 23 (17H) or 55 (37H) is used to clear all registers
simultaneously. This function may be desirable to use prior
to loading new data into the Data or Status Registers. This
address is read into the device in a similar fashion as all of
the other registers.

VECTORED RESTART ADDRESS

The function of addresses 22 (16H) or 54 (36H) are similar
to that of the CLR pin except that the programming of the
registers is not affected. It is recommended but not required
that this address is read after the initial device configuration
load sequence.

SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that al-
lows the user to non-destructively verify the contents of the
registers. Scan mode is invoked through reading a scan ad-
dress into the address register. The scan address of a given
register is defined by the Data register address ÷ 32. The
internal Clocking signal is disabled when a scan address is
read. Disabling the clock freezes the device in it's present
state. Data can then be serially scanned out of the data
registers through the ODD/EVEN Pin. The value of the two
horizontal counters and 1 vertical counter can also be
scanned out by using address numbers 51-53.

Normal device operation can be resumed by latching in a
non-scan address. As the scanning of the registers is a non-
destructive scan, the device will resume correct operation
from the point at which it was halted.

RS170 Default Register Values

The tables below show the values programmed for the
RS170 Format and how they compare against the actual
EIA RS170 Specifications. The default signals that will be
displayed are CSYNC, CBLANK, HDRIVE and VDRIVE. The
device initially starts at the beginning of the odd field of
interlace. All signals have active low pulses and the clock is
disabled at power up. Registers 13 and 14 are not involved
in the actual signal information. If the Vertical Interrupt was
selected a pulse indicating the active lines would be dis-
played.

Reg	D Value	H	Register Description
REG0	0	000	Status Register
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007.	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	038	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time (1)
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 µs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

Signal	Width	µs	%H	Specification (µs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER IOD	910 Clocks	63.556	100	

RS170 Default Register Values (Continued)

Signal	Width	μs	%V	Specification
VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP Intrvl	9 Lines		3.63	9 Lines/Field
VPERIOD (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERIOD (frame)	525 Lines	33.367 ms		33.367 ms/Frame

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	$-0.5V$ to $+7.0V$
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} +0.5V$	$+20$ mA
DC Input Voltage (V_I)	$-0.5V$ to $V_{CC} +0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} +0.5V$	$+20$ mA
DC Output Voltage (V_O)	$-0.5V$ to $V_{CC} +0.5V$
DC Output Source or Sink Current (I_O)	± 15 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	± 20 mA
Storage Temperature (T_{STG})	$-65°C$ to $+150°C$
Junction Temperature (T_J)	
CDIP	175°C
PDIP	140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACT/LM1882	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
74ACT/LM1882	$-40°C$ to $+85°C$
54ACT/LM1882	$-55°C$ to $+125°C$
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT/LM1882 Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$ $C_L = 50$ pF Typ	74ACT/LM1882 $T_A = +25°C$ $C_L = 50$ pF Guaranteed Limits	54ACT/LM1882 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4		4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.49	5.4		5.4	V	
		4.5		3.86		3.76	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		4.86		4.76	V	$I_{OH} = -8$ mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1		0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.001	0.1		0.1	V	
		4.5		0.36		0.44	V	*$V_{IN} = V_{IL}/V_{IH}$
		5.5		0.36		0.44	V	$I_{OH} = +8$ mA
I_{OLD}	Minimum Dynamic Output Current	5.5				32.0	mA	$V_{OLD} = 1.65V$

*All outputs loaded; thresholds on input associated with input under test.

DC Characteristics

For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified) (Continued)

nbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$ $C_L = 50\,pF$		54ACT/LM1882 $T_A = -55°C$ to $+125°C$ $C_L = 50\,pF$	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units	Conditions
			Typ	Guaranteed Limits				
I_{OHD}	Minimum Dynamic Output Current	5.5				-32.0	mA	$V_{OHD} = 3.85V$
I_{IN}	Maximum Input Leakage Current	5.5		±0.1		±1.0	μA	$V_I = V_{CC},\,GND$
I_{CC}	Supply Current Quioscont	5.5		8.0		80	μA	$V_{IN} = V_{CC},\,GND$
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6			1.5	mA	$V_{IN} = V_{CC} - 2.1V$

Note 1: Test Load 50 pF, 500Ω to Ground.

AC Electrical Characteristics

nbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$ $C_L = 50\,pF$			54ACT/LM1882 $T_A = -55°C$ to $+125°C$ $C_L = 50\,pF$		74ACT/LM1882 $T_A = -40°C$ to $+85°C$ $C_L = 50\,pF$		Units
			Min	Typ	Max	Min	Max	Min	Max	
f_{MAXI}	Interlaced f_{MAX} (HMAX/2 is ODD)	5.0	170	190				150		MHz
f_{MAX}	Non-Interlaced f_{MAX} (HMAX/2 is EVEN)	5.0	190	220				175		MHz
t_{PLH1} t_{PHL1}	Clock to Any Output	5.0	4.0	13.0	15.5			3.5	18.5	ns
t_{PLH2} t_{PHL2}	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0			3.5	20.5	ns
t_{PLH3}	Load to Outputs	5.0	4.0	11.5	16.0			3.0	19.5	ns

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C_{PD}	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

AC Operating Requirements

Symbol	Parameter	V_{CC} (V)	74ACT/LM1882 $T_A = +25°C$		54ACT/LM1882 $T_A = -55°C$ to $+125°C$	74ACT/LM1882 $T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimums			
t_{sc} t_{sc}	Control Setup Time ADDR/DATA to LOAD− L/HBYTE to LOAD−	5.0	3.0 3.0	4.0 4.0		4.5 4.5	ns ns
t_{sd}	Data Setup Time D7−D0 to LOAD+	5.0	2.0	4.0		4.5	ns
t_{hc}	Control Hold Time LOAD− to ADDR/DATA LOAD− to L/HBYTE	5.0	0 0	1.0 1.0		1.0 1.0	ns ns
t_{hd}	Data Hold Time LOAD+ to D7−D0	5.0	1.0	2.0		2.0	ns
t_{rec}	LOAD+ to CL− (Note 1)	5.0	5.5	7.0		8.0	ns
t_{wld-} t_{wld+}	Pulse Width Load Low Load High	5.0 5.0	3.0 3.0	5.5 5.0		5.5 7.5	ns ns
t_{wclr}	CLR Pulse Width HIGH	5.0	5.5	6.5		9.5	ns
t_{wck}	CLOCK Width (High or Low)	5.0	2.5	3.0		3.5	ns

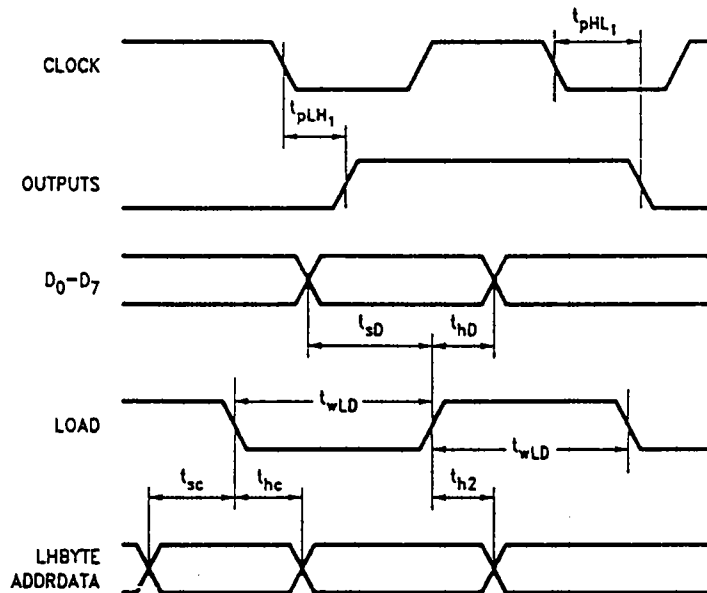Note 1: Removal of Vectored Reset to Clock.

FIGURE 3. AC Specifications

TL/F/10137−6

intel®

82C54
CHMOS PROGRAMMABLE INTERVAL TIMER

- Compatible with all Intel and most other microprocessors
- High Speed, "Zero Wait State" Operation with 8 MHz 8086/88 and 80186/188
- Handles Inputs from DC to 8 MHz — 10 MHz for 82C54-2
- Available In EXPRESS
  — Standard Temperature Range
  — Extended Temperature Range

- Three Independent 16-bit counters
- Low Power CHMOS
  — I_{CC} = 10 mA @ 8 MHz Count frequency
- Completely TTL Compatible
- Six Programmable Counter Modes
- Binary or BCD counting
- Status Read Back Command
- Available In 24-Pin DIP and 28-Pin PLCC

The Intel 82C54 is a high-performance, CHMOS version of the industry standard 8254 counter/timer which is designed to solve the timing control problems common in microcomputer system design. It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz. All modes are software programmable. The 82C54 is pin compatible with the HMOS 8254, and is a superset of the 8253.

Six programmable timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications.

The 82C54 is fabricated on Intel's advanced CHMOS III technology which provides low power consumption with performance equal to or greater than the equivalent HMOS product. The 82C54 is available in 24-pin DIP and 28-pin plastic leaded chip carrier (PLCC) packages.
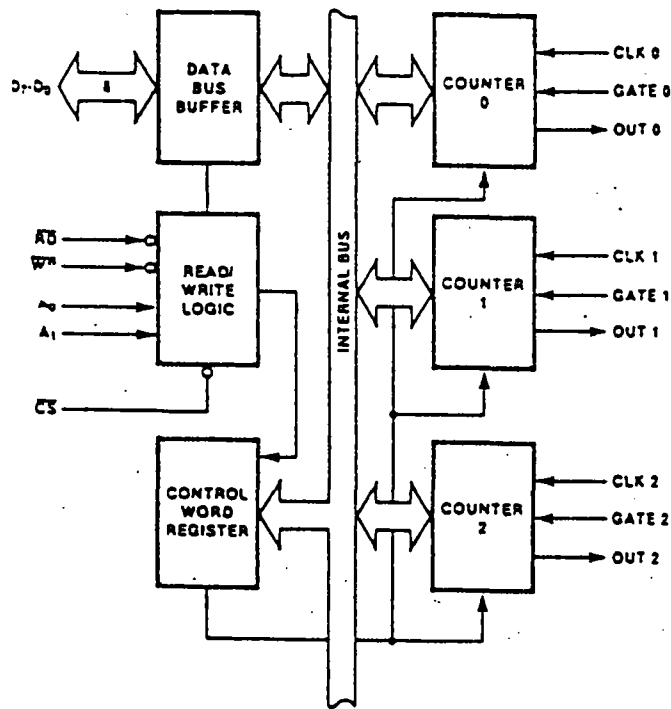
Figure 1. 82C54 Block Diagram
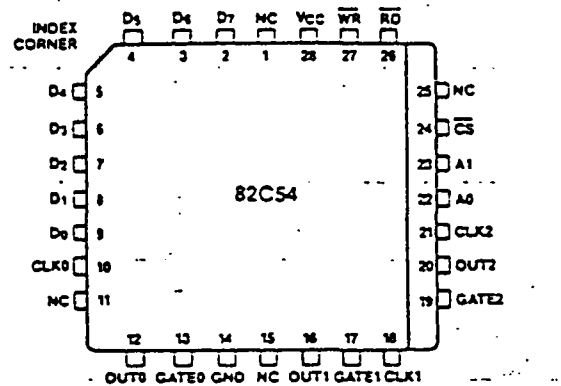
PLASTIC LEADED CHIP CARRIER

Diagrams are for pin reference only.
Package sizes are not to scale.

Figure 2. 82C54 Pinout

Table 1. Pin Description

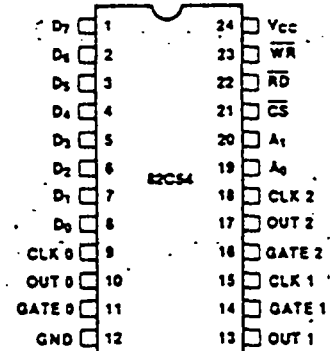| Symbol	Pin Number		Type	Function
	DIP	PLCC		
D_7-D_0	1-8	2-9	I/O	Data: Bidirectional tri-state data bus lines, connected to system data bus.
CLK 0	9	10	I	Clock 0: Clock input of Counter 0.
OUT 0	10	12	O	Output 0: Output of Counter 0.
GATE 0	11	13	I	Gate 0: Gate input of Counter 0.
GND	12	14		Ground: Power supply connection.
OUT 1	13	16	O	Out 1: Output of Counter 1.
GATE 1	14	17	I	Gate 1: Gate input of Counter 1.
CLK 1	15	18	I	Clock 1: Clock input of Counter 1.
GATE 2	16	19	I	Gate 2: Gate input of Counter 2.
OUT 2	17	20	O	Out 2: Output of Counter 2.
CLK 2	18	21	I	Clock 2: Clock input of Counter 2.
A_1, A_0	20-19	23-22	I	Address: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.

A_1	A_0	Selects
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

Symbol	DIP	PLCC	Type	Function
$\overline{CS}$	21	24	I	Chip Select: A low on this input enables the 82C54 to respond to $\overline{RD}$ and $\overline{WR}$ signals. $\overline{RD}$ and $\overline{WR}$ are ignored otherwise.
$\overline{RD}$	22	26	I	Read Control: This input is low during CPU read operations.
$\overline{WR}$	23	27	I	Write Control: This input is low during CPU write operations.
V_{CC}	24	28		Power: +5V power supply connection.
NC		1, 11, 15, 25		No Connect

FUNCTIONAL DESCRIPTION

General

The 82C54 is a programmable interval timer/counter designed for use with Intel microcomputer systems. It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 82C54 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 82C54 to match his requirements and programs one of the counters for the desired delay. After the desired delay, the 82C54 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.

Some of the other counter/timer functions common to microcomputers which can be implemented with the 82C54 are:

- Real time clock
- Even counter
- Digital one-shot
- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

DATA BUS BUFFER

This 3-state, bi-directional, 8-bit buffer is used to interface the 82C54 to the system bus (see Figure 3).
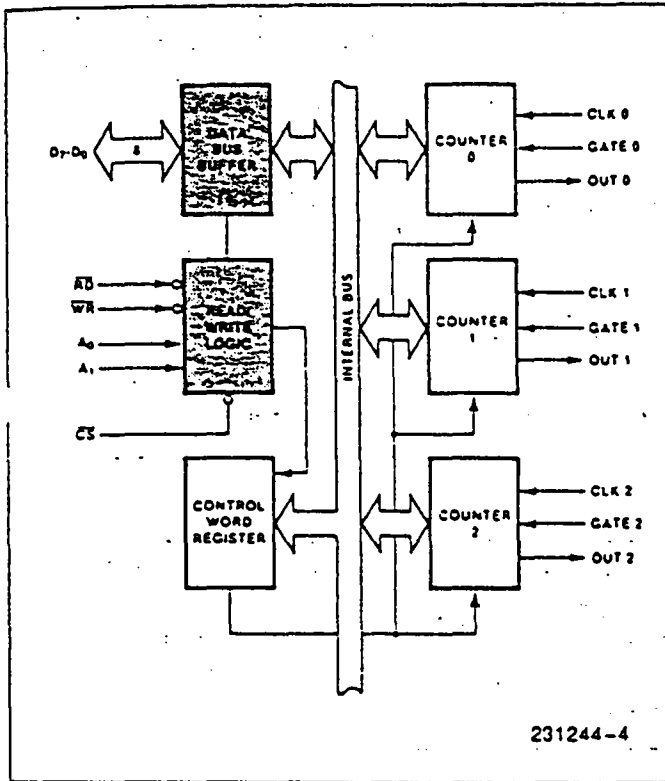

231244-4

Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

READ/WRITE LOGIC

The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 82C54. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into. A "low" on the $\overline{RD}$ input tells the 82C54 that the CPU is reading one of the counters. A "low" on the $\overline{WR}$ input tells the 82C54 that the CPU is writing either a Control Word or an initial count. Both $\overline{RD}$ and $\overline{WR}$ are qualified by $\overline{CS}$; $\overline{RD}$ and $\overline{WR}$ are ignored unless the 82C54 has been selected by holding $\overline{CS}$ low.

CONTROL WORD REGISTER

The Control Word Register (see Figure 4) is selected by the Read/Write Logic when A_1, $A_0 = 11$. If the CPU then does a write operation to the 82C54, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

The Control Word Register can only be written to; status information is available with the Read-Back Command.

231244-5
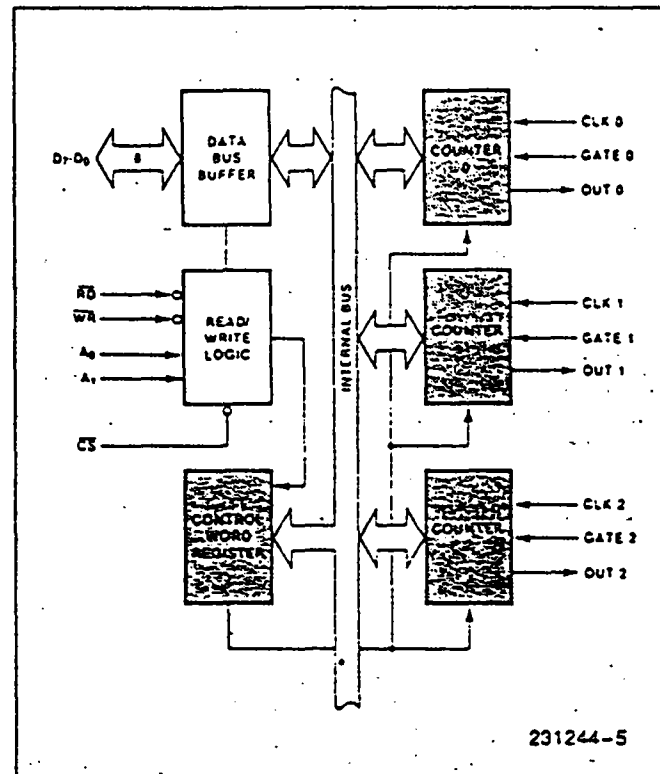
Figure 4. Block Diagram Showing Control Word Register and Counter Functions

COUNTER 0, COUNTER 1, COUNTER 2

These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.

The Counters are fully independent. Each Counter may operate in a different Mode.

The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.
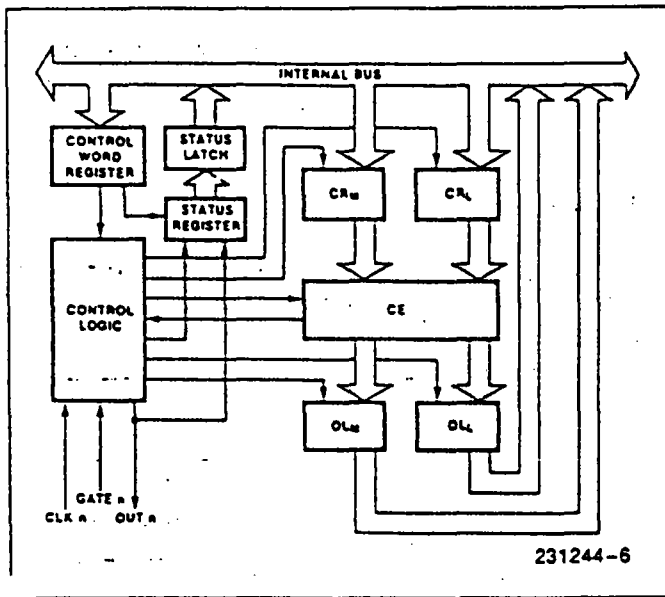
Figure 5. Internal Block Diagram of a Counter

The status register, shown in the Figure, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)

The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter.

OL_M and OL_L are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively. Both are normally referred to as one unit and called just OL. These latches normally "follow" the CE, but if a suitable Counter Latch Command is sent to the 82C54, the latches "latch" the present count until read by the CPU and then return to "following" the CE. One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Similarly, there are two 8-bit registers called CR_M and CR_L (for "Count Register"). Both are normally referred to as one unit and called just CR. When a new count is written to the Counter, the count is

stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously. CR_M and CR_L are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero. Note that the CE cannot be written into; whenever a count is written, it is written into the CR.

The Control Logic is also shown in the diagram. CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.

82C54 SYSTEM INTERFACE

The 82C54 is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.
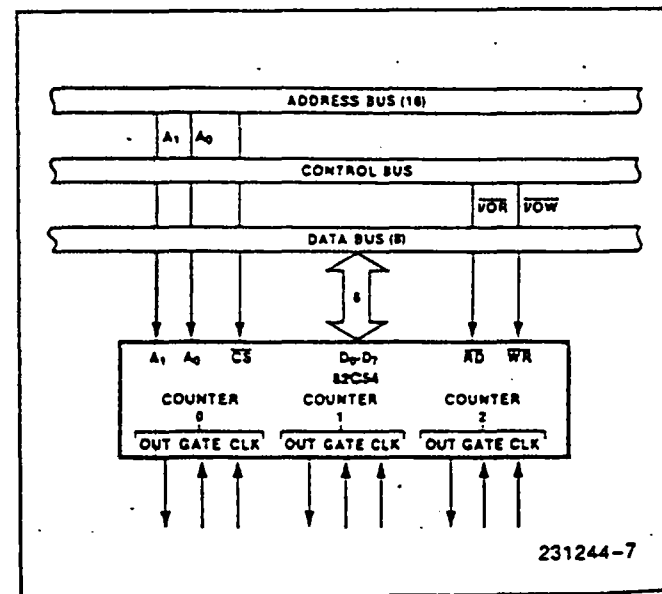

Figure 6. 82C54 System Interface

OPERATIONAL DESCRIPTION

General

After power-up, the state of the 82C54 is undefined. The Mode, count value, and output of all Counters are undefined.

How each Counter operates is determined when it is programmed. Each Counter must be programmed before it can be used. Unused counters need not be programmed.

Programming the 82C54

Counters are programmed by writing a Control Word and then an initial count. The control word format is shown in Figure 7.

All Control Words are written into the Control Word Register, which is selected when $A_1, A_0 = 11$. The Control Word itself specifies which Counter is being programmed.

By contrast, initial counts are written into the Counters, not the Control Word Register. The A_1, A_0 inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.

Control Word Format

$A_1, A_0 = 11$ $\overline{CS} = 0$ $\overline{RD} = 1$ $\overline{WR} = 0$

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD
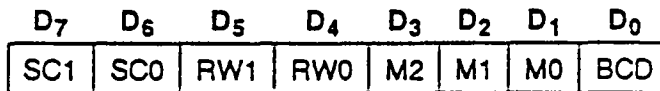
SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (See Read Operations)

RW — Read/Write:

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only.
1	0	Read/Write most significant byte only.
1	1	Read/Write least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 7. Control Word Format

Write Operations

The programming procedure for the 82C54 is very flexible. Only two conventions need to be remembered:

1) For each Counter, the Control Word must be written before the initial count is written.

2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC0, SC1 bits), no special instruction sequence is required. Any programming sequence that follows the conventions above is acceptable.

.A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.

If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

		A_1	A_0			A_1	A_0
Control Word —	Counter 0	1	1	Control Word —	Counter 2	1	1
LSB of count —	Counter 0	0	0	Control Word —	Counter 1	1	1
MSB of count —	Counter 0	0	0	Control Word —	Counter 0	1	1
Control Word —	Counter 1	1	1	LSB of count —	Counter 2	1	0
LSB of count —	Counter 1	0	1	MSB of count —	Counter 2	1	0
MSB of count —	Counter 1	0	1	LSB of count —	Counter 1	0	1
Control Word —	Counter 2	1	1	MSB of count —	Counter 1	0	1
LSB of count —	Counter 2	1	0	LSB of count —	Counter 0	0	0
MSB of count —	Counter 2	1	0	MSB of count —	Counter 0	0	0
		A_1	A_0			A_1	A_0
Control Word —	Counter 0	1	1	Control Word —	Counter 1	1	1
Counter Word —	Counter 1	1	1	Control Word —	Counter 0	1	1
Control Word —	Counter 2	1	1	LSB of count —	Counter 1	0	1
LSB of count —	Counter 2	1	0	Control Word —	Counter 2	1	1
LSB of count —	Counter 1	0	1	LSB of count —	Counter 0	0	0
LSB of count —	Counter 0	0	0	MSB of count —	Counter 1	0	1
MSB of count —	Counter 0	0	0	LSB of count —	Counter 2	1	0
MSB of count —	Counter 1	0	1	MSB of count —	Counter 0	0	0
MSB of count —	Counter 2	1	0	MSB of count —	Counter 2	1	0

NOTE:
In all four examples, all counters are programmed to read/write two-byte counts.
These are only four of many possible programming sequences.

Figure 8. A Few Possible Programming Sequences

Read Operations

It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 82C54.

There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command. Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A1, A0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic. Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

COUNTER LATCH COMMAND

The second method uses the "Counter Latch Command". Like a Control Word, this command is written to the Control Word Register, which is selected when A_1, A_0 = 11. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.

A_1, A_0 = 11; $\overline{CS}$ = 0; $\overline{RD}$ = 1; $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4 - 00 designates Counter Latch Command

X - don't care

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.
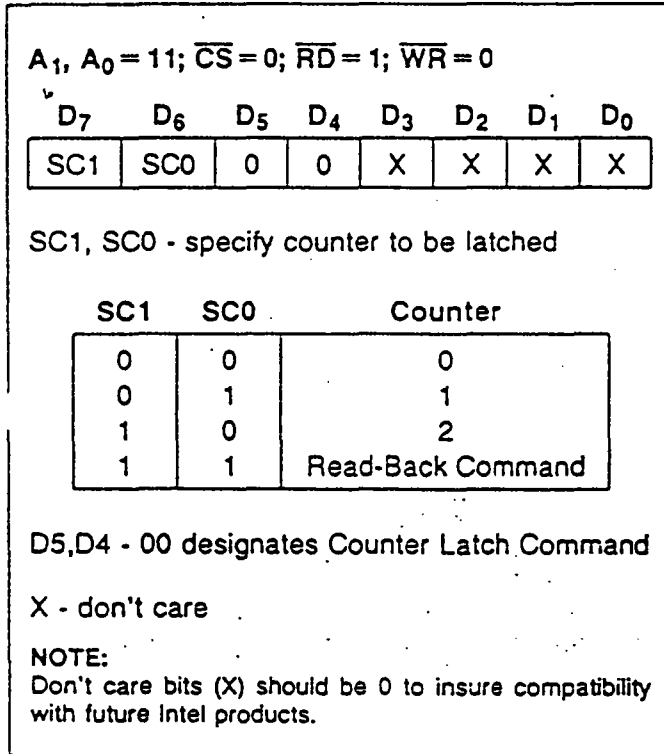
Figure 9. Counter Latching Command Format

The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed). The count is then unlatched automatically and the OL returns to "following" the counting element (CE). This allows reading the contents of the Counters "on the fly" without affecting counting in progress. Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read. Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.

With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other; read or write or pro-

gramming operations of other Counters may be inserted between them.

Another feature of the 82C54 is that reads and writes of the same Counter may be interleaved; for example, if the Counter is programmed for two byte counts, the following sequence is valid.

1. Read least significant byte.
2. Write new least significant byte.
3. Read most significant byte.
4. Write new most significant byte.

If a Counter is programmed to read/write two-byte counts, the following precaution applies; A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.

READ-BACK COMMAND

The third method uses the Read-Back command. This command allows the user to check the count value, programmed Mode, and current state of the OUT pin and Null Count flag of the selected counter(s).

The command is written into the Control Word Register and has the format shown in Figure 10. The command applies to the counters selected by setting their corresponding bits D3,D2,D1 = 1.
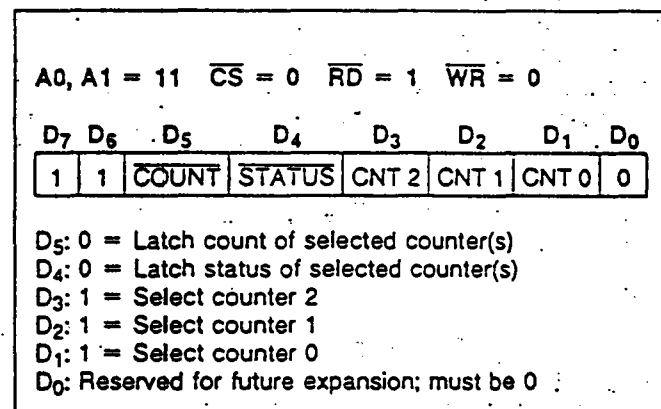
A0, A1 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	1	COUNT	STATUS	CNT 2	CNT 1	CNT 0	0

D_5: 0 = Latch count of selected counter(s)
D_4: 0 = Latch status of selected counter(s)
D_3: 1 = Select counter 2
D_2: 1 = Select counter 1
D_1: 1 = Select counter 0
D_0: Reserved for future expansion; must be 0

Figure 10. Read-Back Command Format

The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit D5 = 0 and selecting the desired counter(s). This single command is functionally equivalent to several counter latch commands, one for each counter latched. Each counter's latched count is held until it is read (or the counter is reprogrammed). That counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the

count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.

The read-back command may also be used to latch status information of selected counter(s) by setting STATUS bit D4 = 0. Status must be latched to be read; status of a counter is accessed by a read from that counter.

The counter status format is shown in Figure 11. Bits D5 through D0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D7 contains the current state of the OUT pin. This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system.
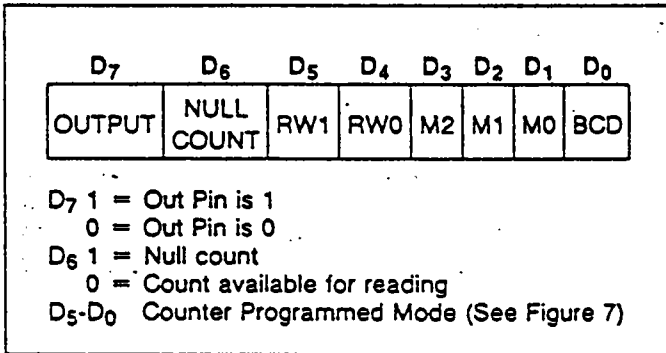
D7	D6	D5	D4	D3	D2	D1	D0
OUTPUT	NULL COUNT	RW1	RW0	M2	M1	M0	BCD

D7 1 = Out Pin is 1
    0 = Out Pin is 0
D6 1 = Null count
    0 = Count available for reading
D5-D0 Counter Programmed Mode (See Figure 7)

Figure 11. Status Byte

NULL COUNT bit D6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE). The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter. If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 12.
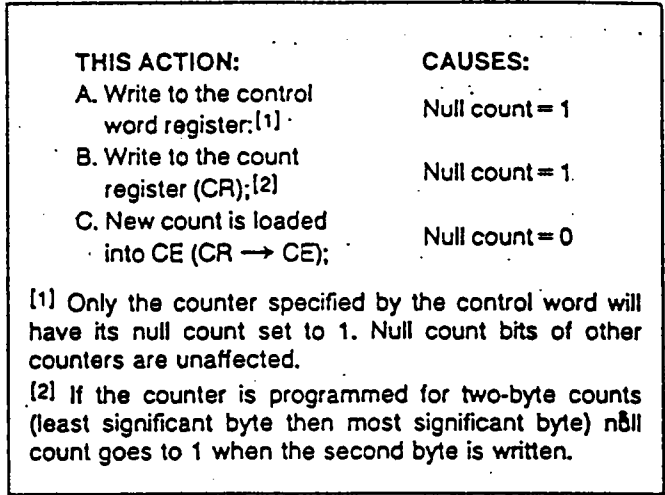
THIS ACTION:	CAUSES:
A. Write to the control word register:[1]	Null count = 1
B. Write to the count register (CR):[2]	Null count = 1
C. New count is loaded into CE (CR → CE):	Null count = 0

[1] Only the counter specified by the control word will have its null count set to 1. Null count bits of other counters are unaffected.
[2] If the counter is programmed for two-byte counts (least significant byte then most significant byte) null count goes to 1 when the second byte is written.

Figure 12. Null Count Operation

If multiple status latch operations of the counter(s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.

Both count and status of the selected counter(s) may be latched simultaneously by setting both COUNT and STATUS bits D5,D4 = 0. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also. Specifically, if multiple count and/or status read-back commands are issued to the same counter(s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 13.

If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

	Command							Description	Results
D7	D6	D5	D4	D3	D2	D1	D0		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 13. Read-Back Command Example

CS	RD	WR	A₁	A₀	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Mode Definitions

The following are defined for use in describing the operation of the 82C54.

CLK PULSE: a rising edge, then a falling edge, in that order, of a Counter's CLK input.

TRIGGER: a rising edge of a Counter's GATE input.

COUNTER LOADING: the transfer of a count from the CR to the CE (refer to the "Functional Description")

MODE 0: INTERRUPT ON TERMINAL COUNT

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then ‚oes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N + 1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).

2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the counting sequence to be synchronized by software. Again, OUT does not go high until i + 1 CLK pulses after the new count of N is written

If an initial count is written while GATE = 0, it wi still be loaded on the next CLK pulse. When GAT goes high, OUT will go high N CLK pulses later; n CLK pulse is needed to load the Counter as this ha already been done.

231244-8
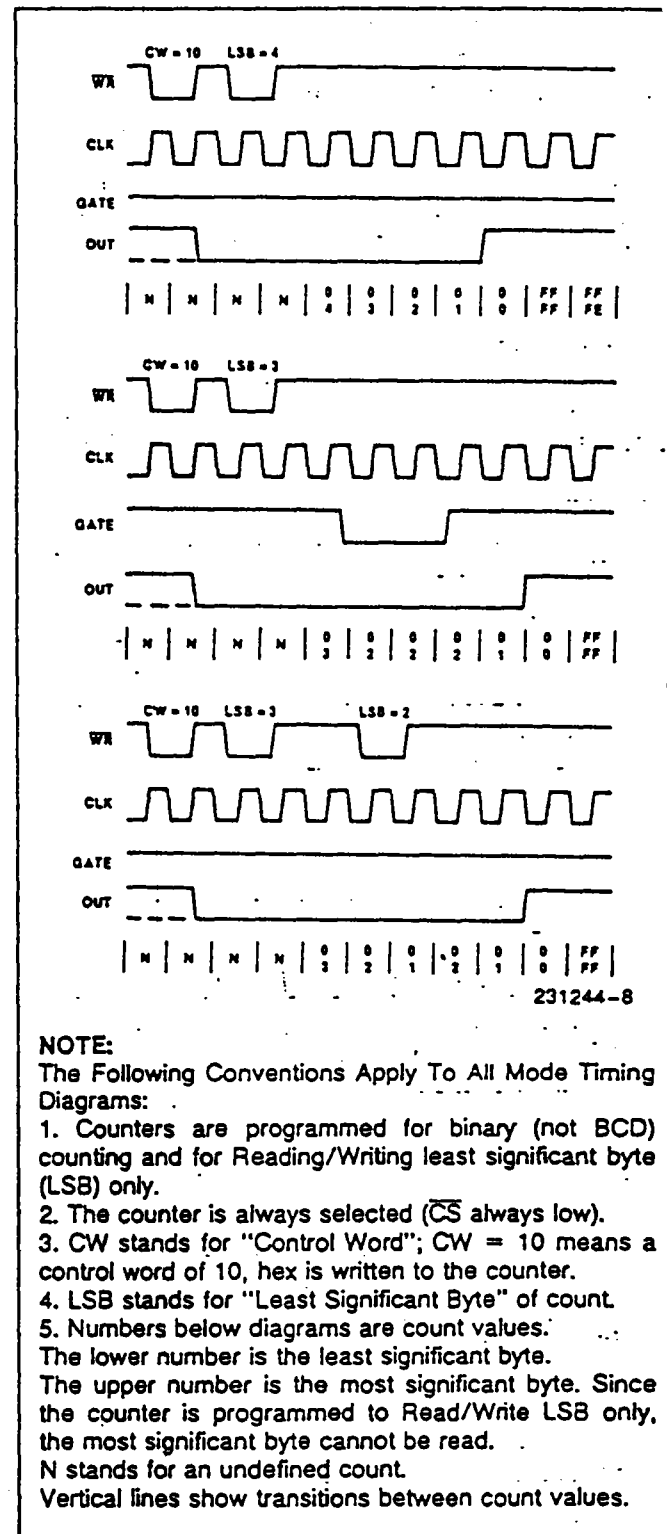
NOTE:
The Following Conventions Apply To All Mode Timing Diagrams:
1. Counters are programmed for binary (not BCD) counting and for Reading/Writing least significant byte (LSB) only.
2. The counter is always selected (CS always low).
3. CW stands for "Control Word"; CW = 10 means a control word of 10, hex is written to the counter.
4. LSB stands for "Least Significant Byte" of count.
5. Numbers below diagrams are count values.
The lower number is the least significant byte.
The upper number is the most significant byte. Since the counter is programmed to Read/Write LSB only, the most significant byte cannot be read.
N stands for an undefined count.
Vertical lines show transitions between count values.

Figure 15. Mode 0

MODE 1: HARDWARE RETRIGGERABLE ONE-SHOT

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero. OUT will then go high and remain high until the CLK pulse after the next trigger. .

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.

a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the Counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.
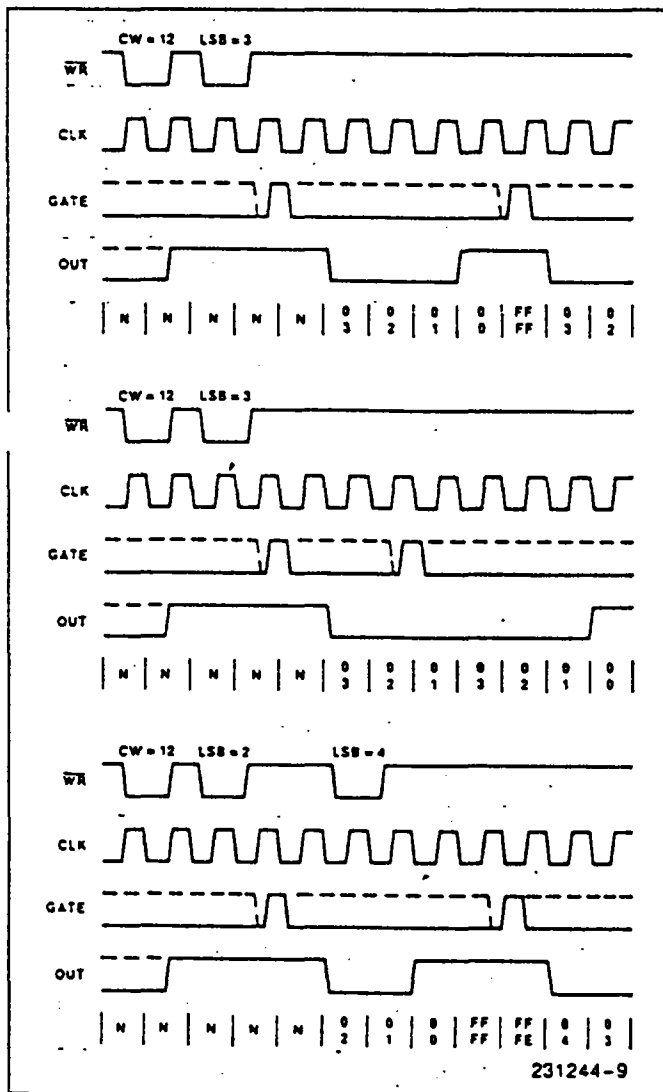
MODE 2: RATE GENERATOR

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

231244–9

Figure 16. Mode 1

231244–10
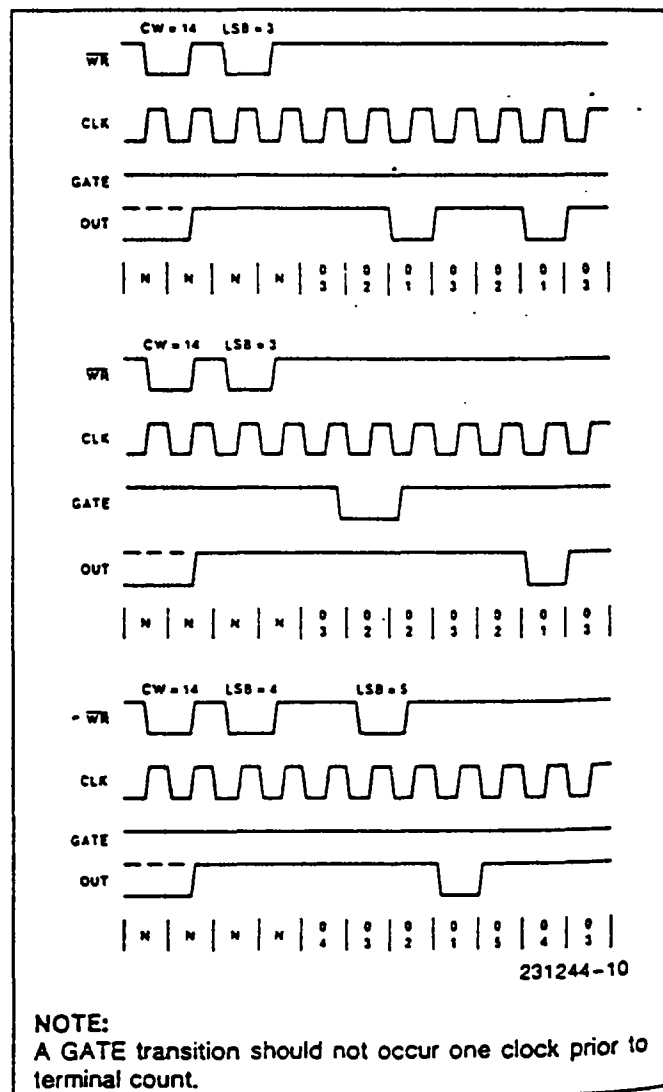
NOTE:
A GATE transition should not occur one clock prior to terminal count.

Figure 17. Mode 2

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.

MODE 3: SQUARE WAVE MODE

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the ext CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts,

OUT will be high for (N + 1)/2 counts and low for (N − 1)/2 counts.

NOTE:
A GATE transition should not occur one clock prior to terminal count.
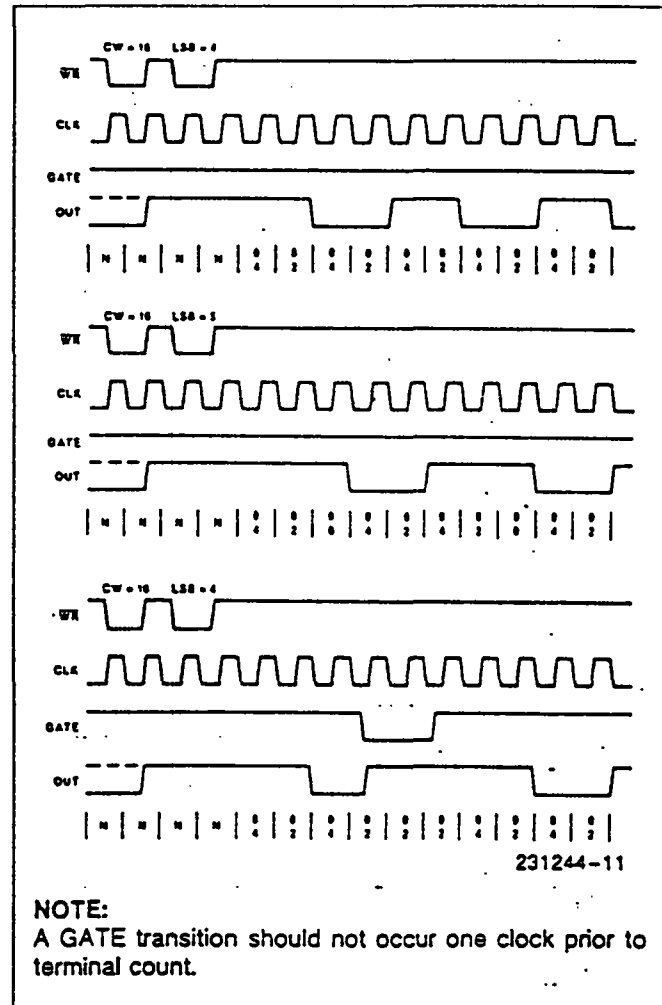
Figure 18. Mode 3

MODE 4: SOFTWARE TRIGGERED STROBE

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is "triggered" by writing the initial count.

GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N + 1 CLK pulses after the initial count is written.

If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

1) Writing the first byte has no effect on counting.

2) Writing the second byte allows the new count to be loaded on the next CLK pulse.

This allows the sequence to be "retriggered" by software. OUT strobes low N+1 CLK pulses after the new count of N is written.
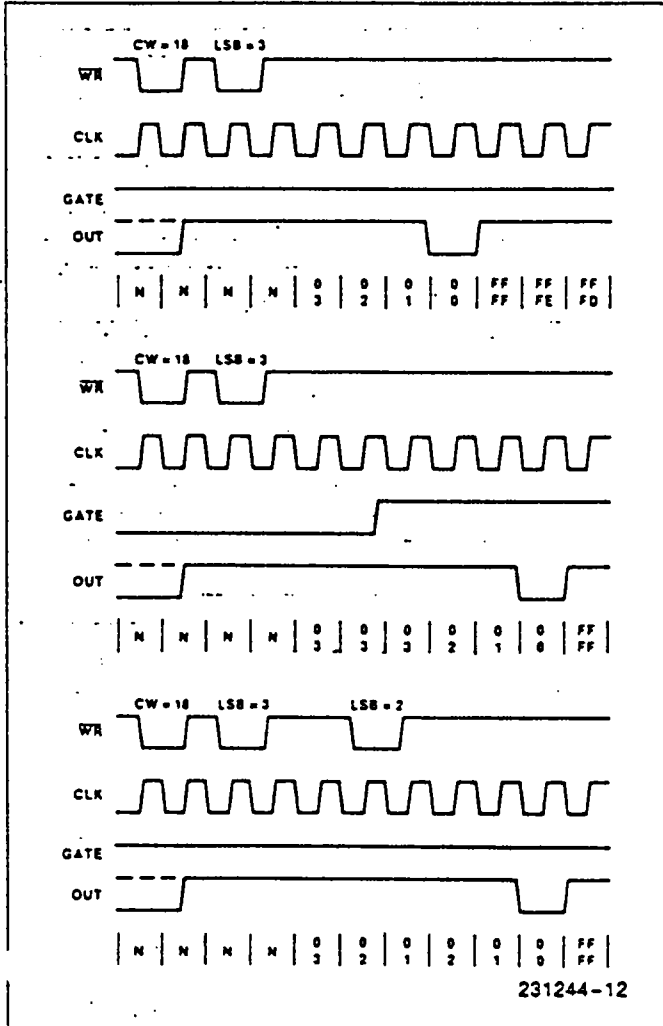
After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N + 1 CLK pulses after any trigger. GATE has no effect on OUT.

If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

Figure 19. Mode 4

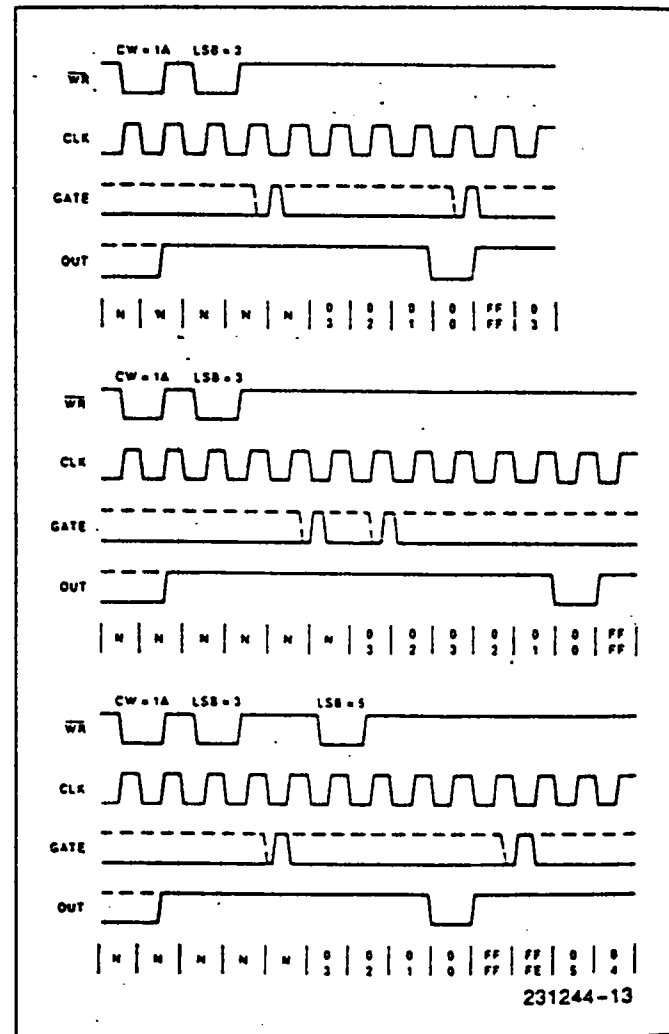**MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)**

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

Figure 20. Mode 5

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables counting	—	Enables counting
1	—	1) Initiates counting 2) Resets output after next clock	—
2	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	—	Enables counting
5	—	Initiates counting	—

Figure 21. Gate Pin Operations Summary

MODE	MIN COUNT	MAX COUNT
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0

NOTE:
0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting

Figure 22. Minimum and Maximum Initial Counts

Operation Common to All Modes

Programming

When a Control Word is written to a Counter, a Control Logic is immediately reset and OUT goes t a known initial state; no CLK pulses are required fc this.

GATE

The GATE input is always sampled on the risin edge of CLK. In Modes 0, 2, 3, and 4 the GATE inpu is level sensitive, and the logic level is sampled o the rising edge of CLK. In Modes 1, 2, 3, and 5 th GATE input is rising-edge sensitive. In these Modes a rising edge of GATE (trigger) sets an edge-sens tive flip-flop in the Counter. This flip-flop is then sam pled on the next rising edge of CLK; the flip-flop i reset immediately after it is sampled. In this way, trigger will be detected no matter when it occurs— high logic level does not have to be maintained unt the next rising edge of CLK. Note that in Modes and 3, the GATE input is both edge- and level-sensi tive. In Modes 2 and 3, if a CLK source other tha the system clock is used, GATE should be pulse immediately following $\overline{WR}$ of a new count value.

COUNTER

New counts are loaded and Counters are decre mented on the falling edge of CLK.

The largest possible initial count is 0; this is equiva lent to 2^{16} for binary counting and 10^4 for BCI counting.

The Counter does not stop when it reaches zero. I Modes 0, 1, 4, and 5 the Counter "wraps around" t the highest count, either FFFF hex for binary count ing or 9999 for BCD counting, and continues count ing. Modes 2 and 3 are periodic; the Counter reload: itself with the initial count and continues countin from there.

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias.......0°C to 70°C
Storage Temperature ....−65° to +150°C
Supply Voltage ....−0.5 to +8.0V
Operating Voltage ....+4V to +7V
Voltage on any Input............GND −2V to +6.5V
Voltage on any Output ..GND−0.5V to V$_{CC}$ + 0.5V
Power Dissipation ....1 Watt

*Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS
(T$_A$ = 0°C to 70°C, V$_{CC}$ = 5V ± 10%, GND = 0V) (T$_A$ = −40°C to +85°C for Extended Temperature)

Symbol	Parameter	Min	Max	Units	Test Conditions
V$_{IL}$	Input Low Voltage	−0.5	0.8	V	
V$_{IH}$	Input High Voltage	2.0	V$_{CC}$ + 0.5	V	
V$_{OL}$	Output Low Voltage		0.4	V	I$_{OL}$ = 2.5 mA
V$_{OH}$	Output High Voltage	3.0 V$_{CC}$ − 0.4		V V	I$_{OH}$ = −2.5 mA I$_{OH}$ = −100 μA
I$_{IL}$	Input Load Current		±2.0	μA	V$_{IN}$ = V$_{CC}$ to 0V
I$_{OFL}$	Output Float Leakage Current		±10	μA	V$_{OUT}$ = V$_{CC}$ to 0.0V
I$_{CC}$	V$_{CC}$ Supply Current		20	mA	Clk Freq = 8MHz 82C54 10MHz 82C54-2
I$_{CCSB}$	V$_{CC}$ Supply Current-Standby		10	μA	CLK Freq = DC $\overline{CS}$ = V$_{CC}$. All Inputs/Data Bus V$_{CC}$ All Outputs Floating
I$_{CCSB1}$	V$_{CC}$ Supply Current-Standby		150	μA	CLK Freq = DC $\overline{CS}$ = V$_{CC}$. All Other Inputs, I/O Pins = V$_{GND}$, Outputs Open
C$_{IN}$	Input Capacitance		10	pF	f$_c$ = 1 MHz
C$_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND(5)
C$_{OUT}$	Output Capacitance		20	pF	

A.C. CHARACTERISTICS
T$_A$ = 0°C to 70°C, V$_{CC}$ = 5V ±10%, GND = 0V) (T$_A$ = −40°C to +85°C for Extended Temperature)

BUS PARAMETERS (Note 1)
READ CYCLE

Symbol	Parameter	82C54		82C54-2		Units
		Min	Max	Min	Max	
t$_{AR}$	Address Stable Before $\overline{RD}$ ↓	45		30		ns
t$_{SR}$	$\overline{CS}$ Stable Before $\overline{RD}$ ↓	0		0		ns
t$_{RA}$	Address Hold Time After $\overline{RD}$ ↑	0		0		ns
t$_{RR}$	$\overline{RD}$ Pulse Width	150		95		ns
t$_{RD}$	Data Delay from $\overline{RD}$ ↓		120		85	ns
t$_{AD}$	Data Delay from Address		220		185	ns
t$_{DF}$	$\overline{RD}$ ↑ to Data Floating	5	90	5	65	ns
t$_{RV}$	Command Recovery Time	200		165		ns

NOTE:
1. AC timings measured at V$_{OH}$ = 2.0V, V$_{OL}$ = 0.8V.

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	82C54		82C54-2		Units
		Min	Max	Min	Max	
t_{AW}	Address Stable Before $\overline{WR}$ ↓	0		0		ns
t_{SW}	$\overline{CS}$ Stable Before $\overline{WR}$ ↓	0		0		ns
t_{WA}	Address Hold Time After $\overline{WR}$ ↑	0		0		ns
t_{WW}	$\overline{WR}$ Pulse Width	150		95		ns
t_{DW}	Data Setup Time Before $\overline{WR}$ ↑	120		95		ns
t_{WD}	Data Hold Time After $\overline{WR}$ ↑	0		0		ns
t_{RV}	Command Recovery Time	200		165		ns

CLOCK AND GATE

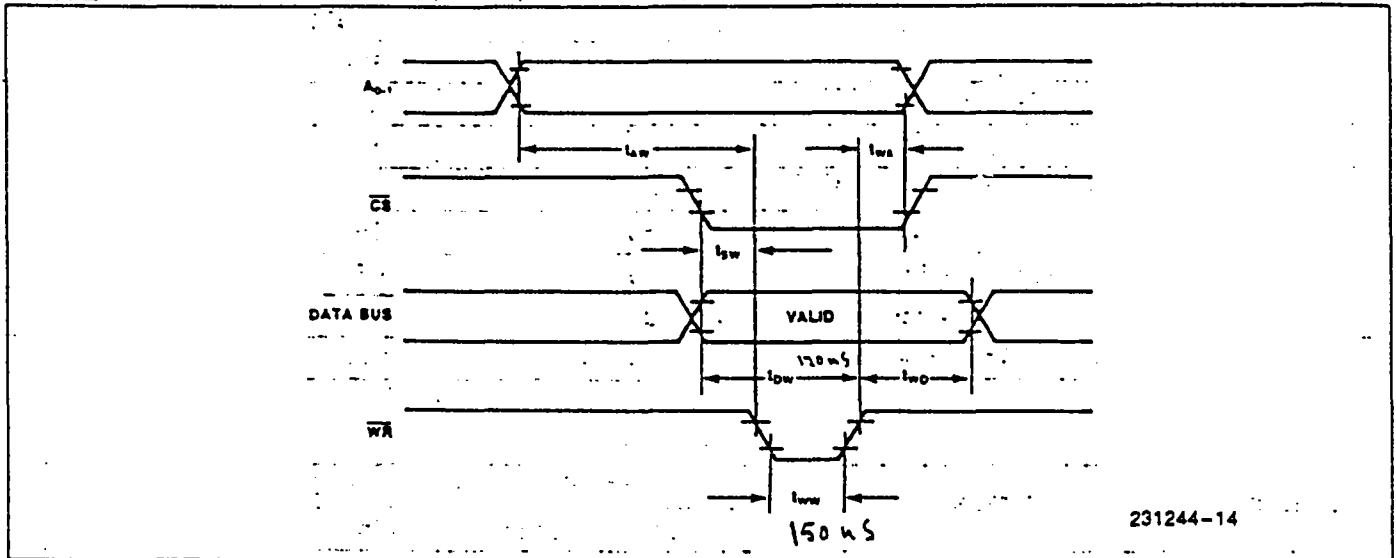| Symbol	Parameter	82C54		82C54-2		Units
		Min	Max	Min	Max	
t_{CLK}	Clock Period	125	DC	100	DC	ns
t_{PWH}	High Pulse Width	60(3)		30(3)		ns
t_{PWL}	Low Pulse Width	60(3)		50(3)		ns
T_R	Clock Rise Time		25		25	ns
t_F	Clock Fall Time		25		25	ns
t_{GW}	Gate Width High	50		50		ns
t_{GL}	Gate Width Low	50		50		ns
t_{GS}	Gate Setup Time to CLK ↑	50		40		ns
t_{GH}	Gate Hold Time After CLK ↑	50(2)		50(2)		ns
T_{OD}	Output Delay from CLK ↓		150		100	ns
t_{ODG}	Output Delay from Gate ↓		120		100	ns
t_{WC}	CLK Delay for Loading(4)	0	55	0	55	ns
t_{WG}	Gate Delay for Sampling(4)	−5	50	−5	40	ns
t_{WO}	OUT Delay from Mode Write		260		240	ns
t_{CL}	CLK Set Up for Count Latch	−40	45	−40	40	ns

NOTES:
2. In Modes 1 and 5 triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the 82C54-2) of the rising clock edge may not be detected.
3. Low-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring counter reprogramming.
4. Except for Extended Temp., See Extended Temp. A.C. Characteristics below.
5. Sampled not 100% tested. $T_A = 25°C$.
6. If CLK present at T_{WC} min then Count equals N+2 CLK pulses, T_{WC} max equals Count N+1 CLK pulse. T_{WC} min Twc max, count will be either N+1 or N+2 CLK pulses.
7. In Modes 1 and 5, if GATE is present when writing a new Count value, at T_{WG} min Counter will not be triggered, at T_{WG} max Counter will be triggered.
8. If CLK present when writing a Counter Latch or ReadBack Command, at T_{CL} min CLK will be reflected in count value latched, at T_{CL} max CLK will not be reflected in the count value latched. Writing a Counter Latch or ReadBack Command between T_{CL} min and T_{WL} max will result in a latched count value which is ± one least significant bit.

EXTENDED TEMPERATURE ($T_A = -40°C$ to $+85°C$ for Extended Temperature)

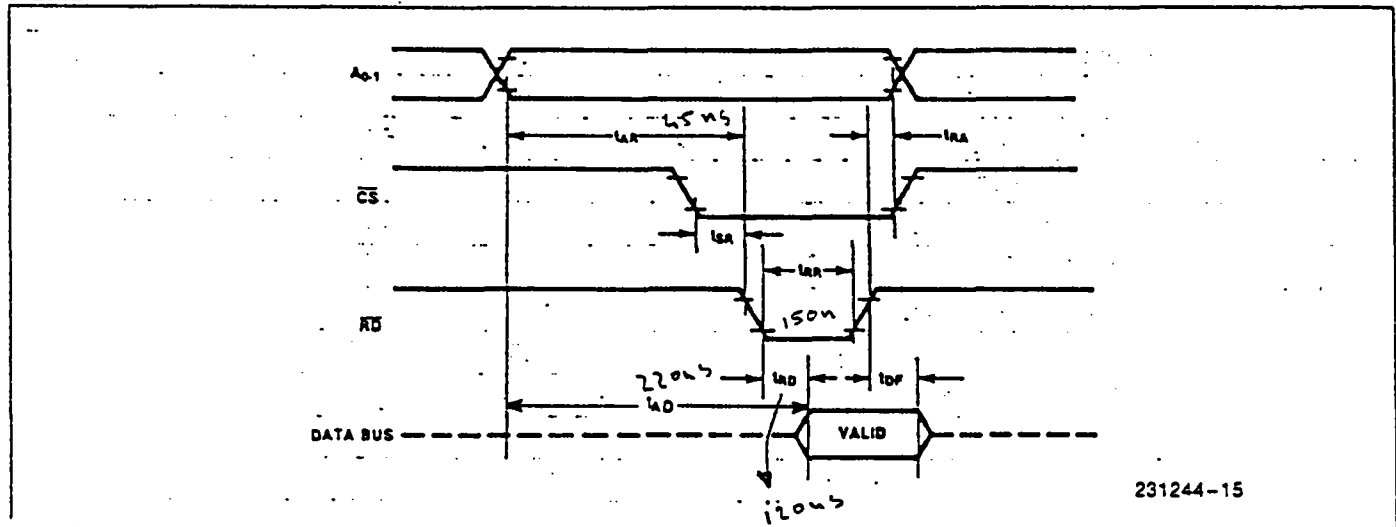| Symbol	Parameter	82C54		82C54-2		Units
		Min	Max	Min	Max	
t_{WC}	CLK Delay for Loading	−25	25	−25	25	ns
t_{WG}	Gate Delay for Sampling	−25	25	−25	25	ns

WAVEFORMS

WRITE

231244-14

READ

231244-15

RECOVERY

231244-16

CLOCK AND GATE

231244-17

* Last byte of count being written
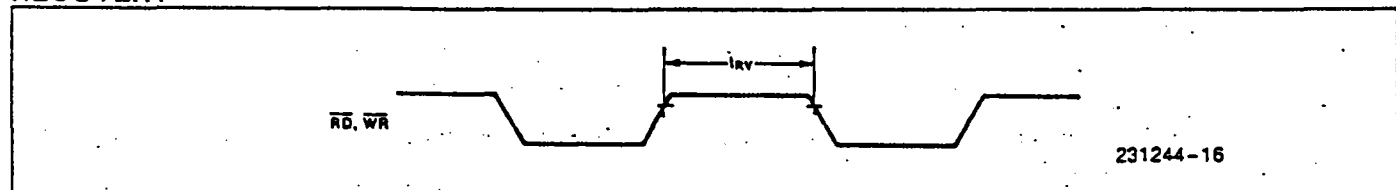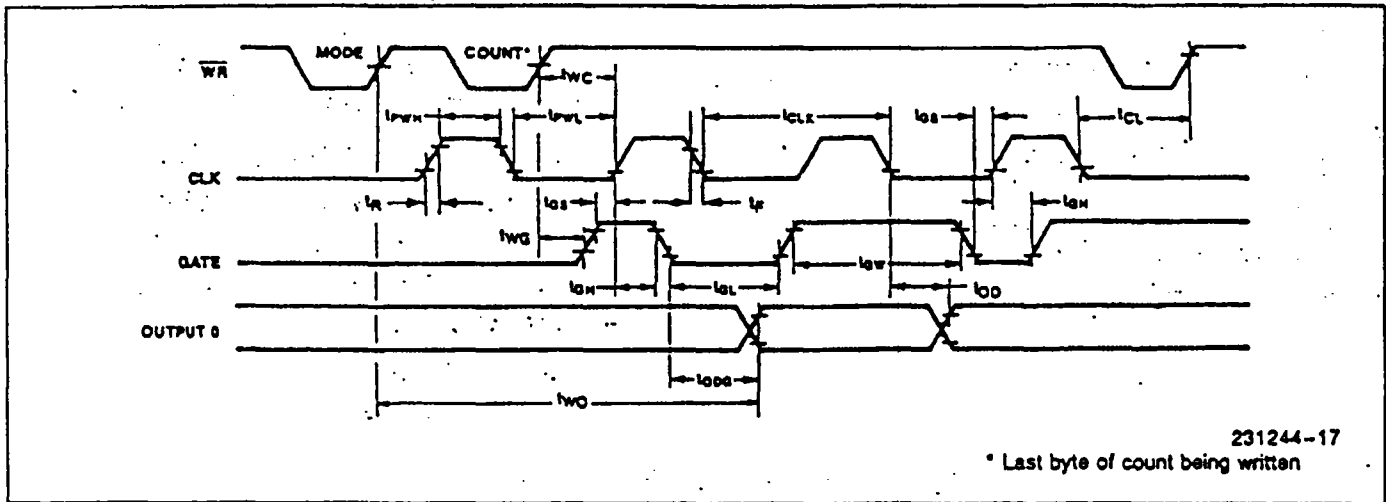
A.C. TESTING INPUT, OUTPUT WAVEFORM

231244-18

A.C. Testing: Inputs are driven at 2.4V for a logic "1" and 0.45V for a logic "0." Timing measurements are made at 2.0V for a logic "1" and 0.8V for a logic "0."

A.C. TESTING LOAD CIRCUIT

231244-19

$C_L = 150$ pF
C_L includes jig capacitance