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User Manual

IMS B419-4 Graphics TRAM

Contents

IMPORTANT— READ THIS BEFORE PROCEEDING

The IMS B419 can be damaged by improper handling and incorrect installation. You must read section A before installing the board.

Look for an errata sheet in the package, if present it contains important information which must be read.

1 Introduction

The IMS B419 is one of a range of INMOS **TRA**nsputer **M**odules (TRAMs). TRAMs integrate processor, memory and peripheral functions; allowing powerful, flexible, transputer based systems to be produced with the minimum of design effort. [1]

The IMS B419 combines the IMS G300 Colour Video Controller (CVC) with the IMS T800 32-bit, floating point transputer, to form a high performance graphics subsystem. The frame store consists of 2 Mbytes of dual ported Video RAM which supports displays of arbitrary resolution at 8 bits/pixel.

The IMS G300 is a combined video timing generator, and colour look-up table. It can be programmed by the IMS T800 to generate a variety of display resolutions, limited only by its maximum dot rate. The colour look-up table expands an eight-bit pixel value to a 24-bit RGB value which describes the colour displayed on the monitor screen. The look-up table contents are programmed by the IMS T800.

The IMS T800 has direct access to the 2 Mbytes of frame store and also to 2 Mbytes of workspace RAM. The IMS T800 is a 32-bit processor with on-chip floating point arithmetic unit, capable of 1.5Mflops. This makes it ideal for performing 2d and 3d graphical transformations and drawing operations.

The IMS T800 can also input drawing commands or image data from an array of transputers, or TRAMs, on its four INMOS serial links at a total data rate of up to 6.7 Mbytes/sec.

The IMS B419 presents software running on the IMS T800 with a simple byte-mapped display: each pixel is represented by one byte of memory and, in order of increasing memory address, bytes are mapped to pixels on the screen in left-to-right, top-to-bottom order. The colour of a pixel is determined by the value written to the byte which represents it and by the contents of the corresponding location in the colour look-up table.

This manual describes the IMS B419-4 which is fitted with the IMS G300B. For information on the IMS B419-3 which was fitted with the IMS G300A, and for an description of the software compatibility issues, refer to the appendix at the end of this manual.

[1] Further details of the TRAM/motherboard philosophy and the full electrical and mechanical specification of TRAMs can be found in *INMOS Technical Note 29: Dual-In-Line Transputer Modules (TRAMs)* and *INMOS Technical Note 49: Module Motherboard Architecture*. The *Transputer Reference Manual* may also be required. This is available as a separate publication from INMOS.

2 IMS G300 Colour Video Controller (CVC)

The IMS G300 is a combined video timing generator (VTG) and colour look-up table (CLUT). This section describes the aspects of the IMS G300 specific to the IMS B419. Full details of the IMS G300 register map and programming can be found in the INMOS *Graphics Data Book*. In this section, the term micro-port refers to the hardware interface through which the IMS T800 programs the IMS G300.

2.1 VTG Startup Sequence and Programming

On startup, after reset, the IMS T800 must perform certain actions to select a pixel clock source and configure the IMS G300. The startup sequence is

1 Select the clock source to be either the 5MHz TRAM clock or the crystal oscillator by writing the appropriate value to the *clock select* register.

2 Assert (for at least 10μs), then deassert, the IMS G300 **Reset** by writing to the *CVC reset* register.

3 If the IMS G300's PLL is to be used, write the PLL multiplication factor (plus 32) to the IMS G300 bootstrap location. Adding 32 to the PLL multiplier sets bit 5 to enable the PLL. When using the $\times 1$ clocking scheme, this register should be written with 5.

4 Write to the IMS G300 control register to set the micro-port to word-wide mode, and disable the VTG: 0 is a suitable value. Note that the VTG must be disabled while the display timing parameters are programmed.

5 Write the display timing parameters to the IMS G300 data-path registers.

6 Write the colour look up table contents to the IMS G300.

7 Enable the VTG in master mode by writing the IMS G300 control register with bit 0 = 1. Bit 16 should be written with 1 to define CBLANK as an output. The value of the control word written is also determined by the desired pixel width (normally 8 bits/pixel).

Reading from and writing to the display timing (VTG) registers should be done only while the timing generator is disabled, otherwise the registers will not be programmed correctly. The colour look-up table contents can be re-written at any time: even while the VTG is enabled.

Details of what the display timing parameters are, and examples of how they can be determined for a particular combination of video monitor and display resolution, can be found in the INMOS *Graphics Data Book*. Normally these parameters are set by the user software as part of the initialisation sequence and do not change subsequently. However, there is nothing to prevent the user redefining the display timing parameters while the IMS B419 is being used: for example, to alter the display resolution. This can only be done while the VTG is disabled. The reprogramming sequence is

1 Write 0 to the IMS G300 control register, disabling VTG.

2 Write the new display timing parameters to the IMS G300 data-path registers.

3 Write a new value to IMS G300 control register, enabling the VTG, and selecting the correct number of bits/pixel etc.

If the PLL clock multiplication factor, or clocking scheme is to be changed, the full startup sequence described at the beginning of this section will need to be used.

2.2 CVC reset register

The IMS G300 must be reset before it can be programmed. This register allows users to reset the IMS G300 CVC from software running on the IMS T800: for example, to change the PLL clock multiplication factor. The

CVC reset register is located at #000000F0. To reset the CVC, the CVC reset register must be written with 1 for a minimum of 10μs.

CVC reset register	IMS G300 state
1	Reset
0	Enabled

Table 2.1 CVC reset register.

2.3 Pixel clock selection

The IMS G300 requires a clock to control the movement of pixel data, and generate timing signals. It has a phase-locked loop (PLL) which can generate the high frequency pixel clock from a low frequency input clock. The PLL can generate frequencies from 25MHz upwards. On the IMS B419-4, the pixel clock must be in the range 10MHz-110MHz. The IMS B419, provides a choice of clocking schemes: choosing a clocking scheme must be done partly when the IMS B419 is installed in a system, and partly by the user software whenever the system starts up. At installation time, the clocking scheme you choose to use determines whether you need to fit a crystal oscillator module to the IMS B419. At system start-up, your software may have to program a multiplication factor for the PLL and select a clock source for the PLL. The clocking schemes are all described below. Factors influencing the choice of clocking scheme are: whether the required clock is within the range acheivable with the PLL; and, if so, if it is a multiple of 5MHz.

5MHz TRAM clock and PLL The primary clocking system utilises the IMS G300's on chip phase-locked loop (PLL) to multiply the 5MHz TRAM clock to the video data rate. The multiplication factor must be an integer value between 5 and 22 to produce a video data rate in the range of 25-110 MHz. The clock select register must be written with 0 to select this mode. Bit 5 of the IMS G300B boot location must be set to enable the PLL.

Crystal oscillator and PLL The second method uses the on board crystal oscillator to drive the PLL clock input. This method is used when the required video data rate is not a multiple of 5MHz, but is within the range of the PLL. The clock select register must be written with 1. Bit 5 of the IMS G300B boot location must be set to enable the PLL.

Any oscillator frequency in the range of 5.0-9.0 MHz may be used. The crystal oscillator module is located as shown in fig A.3, and is socketed to make replacement easy. The oscillator module must be as specified in sec A.3. The resulting pixel clock should be in the range 25MHz-110MHz. The clock multiplication factor must not be less than 5.

Although all possible multiplication factors will work with all permissible input frequencies; it is recommended that, for any particular output frequency, the minimum suitable multiplication factor should be used. For example, to generate an 80MHz pixel clock you could multipy the 5MHz TRAM clock by 16, but fitting an 8MHz crystal oscillator and setting the PLL multiplication factor to 10 will produce a more stable pixel clock.

$\times$1 Mode The third method is to operate the IMS G300 in $\times$1 clock mode from the onboard crystal oscillator. This method is recommended only for use when the required pixel clock frequency is below the range of the PLL: that is, when it is in the range 10MHz-25MHz. Bit 5 of the IMS G300B boot location must be writen with 0 to disable the PLL. The clock select register must be written with 1. The clock signal in $\times$1 mode must be low for a minimum of 6ns, the maximum pixel clock frequency in this mode is approximately 80MHz. Note that in this mode, you must still write a PLL multiplication factor to the bootstrap location, even though it is not used. The value 5 is suggested.

2.3.1 Clock Select Register

The clock select register allows users to choose a pixel dot rate which may not be possible using the 5 MHz TRAM clock and PLL multiplication factors, or which is below the range of the PLL. The clock select register is located at #000000F4. On power up, or on a system reset the clock select register defaults to '0'.

PLL clock select register	Clock source
0	5MHz TRAM clock
1	Crystal Oscillator

Table 2.2 PLL mode clock source selection

2.4 IMS G300 control register

The IMS G300 has a control register which sets various operating modes. On the IMS B419 some of the bits in the control register must be set to specific values: otherwise the board will not function correctly. Other bits in the control register are user-definable. For correct operation of the IMS B419-4, the following restrictions must be observed

1 The IMS G300 must be operated in mode 1.

2 The IMS G300 must be operated in master mode.

3 The IMS G300 must be operated with the micro-port in word mode.

4 Delay value must be set to 0.

5 Black level must be set to 0.

6 CBLANK must be defined as an output.

7 The correct pixel width must be selected. This would normally be 8 bits, which requires bits 17 and 18 of the control register to be written with 1. Other pixel widths can be used: refer to the IMS G300B data sheet for detailed information.

Table 2.3 shows how the control register should be set on the IMS B419-4: refer to the INMOS *Graphics Data Book* for detailed information on the function of each bit.

Bit	Function	Write With
0	Enable VTG	
1	Generate an Interlaced or Non-interlaced display	
2	Operating mode: must be Master Mode.	0
3	Frame flyback pattern, write according to monitor spec.	
4	Digital sync format, write according to monitor spec.	
5	Analogue video format, write according to monitor spec.	
6	Reserved	0
7	Micro port mode: must be Word Mode.	0
8	Pixel port mode: must be Mode 1.	0
9-11	Delay value	0
12	Black level	0
13	Reserved	0
14	VRAM update operational	0
15	Enable/disable blanking: must be enabled	0
16	CBLANK input/output select	normally 1
17-18	Pixel width selector	11 for 8 bits/pixel
19-23	Reserved	0

Table 2.3 IMS G300 control register

2.5 Colour Look-up Table (CLUT)

The IMS G300 contains a colour look-up table of 256 locations, each 24 bits wide. 8-bit pixel values from the framestore address a location in the look-up table. The 24-bit result is used to drive the digital to analog convertors (DACs) which produce the analog video output. The look up table appears as 256 word-wide locations in the address space occupied by the IMS G300, and must be programmed by the IMS T800. The 24 bits are aligned in the 24 least significant bits of the word. Refer to the INMOS *Graphics Data Book* for details of register locations and how to program the CLUT contents.

3 Memory Map and Register Functions

The memory space may be divided into two non-contiguous areas, bitmap and workspace, so that operating systems which use automatic sizing will not trespass on the screen space. Alternatively, if the drawing program requires over 2 Mbytes and not much screen space is required, the memory can be arranged so that the VRAM is contiguous with the workspace RAM. Figure 3.1 shows how the memory is mapped into the address space of the IMS T800.

Jumper Fitted	VRAM start address
JP4	#80200000
JP5	#C0000000

Table 3.1 VRAM Start Address selection

NOTE: JP4 and JP5 **must not** be fitted at the same time, or damage may result.

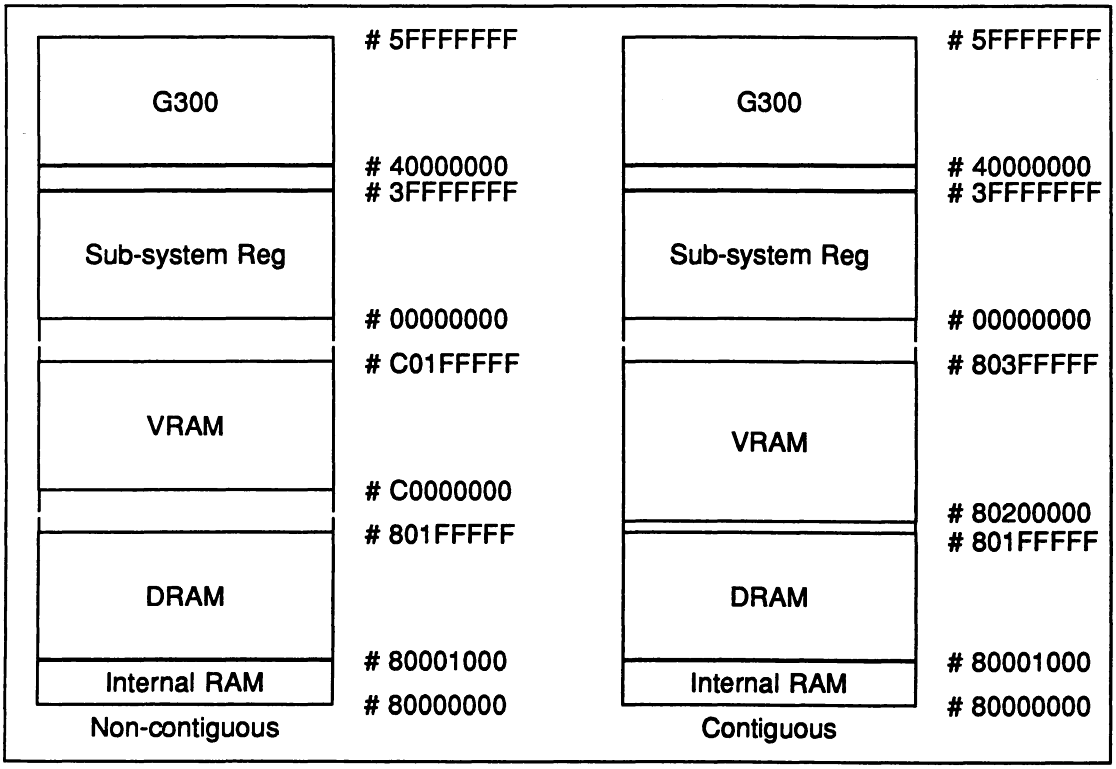

Figure 3.1 Non-contiguous and contiguous address maps

The IMS G300 is placed at a base address of #40000000 and occupies a block of 512 words. Refer to the INMOS *Graphics Data Book* for details of the IMS G300 register map and programming information. The register addresses given in the IMS G300 data sheet are offsets in words from the base address given in the above table.

3.1 SubSystem registers

The IMS B419 is able to control a network of transputers or other TRAMs by means of its subsystem port. The subsystem port consists of three signals: **SubSystemReset** and **SubSystemAnalyse**, which enable the master to reset and analyse its subsystem; and **SubSystemnotError**, which is used to monitor the error flag of the subsystem. The subsystem registers drive the subsystem reset and analyse pins and monitor the subsystem error pin. To maintain software compatibility between TRAMs, the SubSystem registers are placed at the locations shown in table 3.2.

Register		Byte address	Asserted state
SubSystemReset	(Wr only)	#00000000	1
SubSystemAnalyse	(Wr only)	#00000004	1
SubSystemError	(Rd only)	#00000000	1
CVC Reset	(Wr only)	#000000F0	1
Clock Select	(Wr only)	#000000F4	

Table 3.2 IMS B419 register map

3.2 CVC Reset and Clock Select registers

These registers are located as shown in table 3.2. They are described elsewhere in this manual.

4 Multiple Buffering and Frame Flipping

In some graphics applications, such as animation, it is useful to have at least two drawing buffers. This allows one buffer to be displayed whilst the other is being updated by the IMS T800. To prevent disturbing visual effects, the buffers should be exchanged during frame fly-back: when the IMS B419 is not actively displaying the buffer contents. The IMS G300 *top of screen* register holds the address of the pixel in the top, left-hand corner of the screen. This register is used to select the active display buffer in a multiple buffer system.

Drawing buffers must start at byte addresses which are multiples of 2048 (#800). For example if a screen size of 800×600 pixels is being used: the first drawing buffer can start at the start of VRAM (eg #C0000000 with JP5 fitted), the next can start at #C0075800 since this is the next multiple of 2048 after the end of the first buffer. The value written to the *top of screen* register is the start address of the drawing buffer minus the VRAM start addresss, divided by 2048. To continue the previous example, the *top of screen* register would be written with either 0 or 235 (#EB) to select between the two buffers.

So that software can detect frame fly-back, the **FrameInactive** signal from the IMS G300 is used to produce an event request to the IMS T800. The event request is made at the beginning of frame flyback: there is no indication of the end of frame fly-back. Note that the event request logic is only cleared by an event acknowledge from the transputer, and will continue to assert event request until the event is serviced. To ensure that the event handler remains synchronised with the start of frame fly-back, it should respond to every event.

For example, to implement the buffer flipping mechanism, the event handler should always know which is the active drawing buffer: then, it can write the top-of screen register with the correct display start address on **every** event. Thus, frame flipping would always be synchronous with the start of frame-flyback. Similarly, if there are several different tasks which may be required of the event handler, it can maintain a set of flags indicating which are to be performed on the next frame fly-back.

Appendices

A Installation and Handling

The IMS B419 is a transputer module designed to be fitted to a transputer module mother-board. Before installing the IMS B419, first make sure that the power is turned off. Although the IMS B419 can be plugged and un-plugged from the mother board many times without contact wear, care should be taken when fitting and removing the TRAM.

When fitting the IMS B419 to the mother board, ensure that all of its pins are straight, then make sure that it is the correct way round (match up the yellow triangle on the TRAM with the yellow triangle on the mother board), then line up the pins with their sockets. When you are sure that the pins are aligned, gently push the TRAM home. Excessive force is not necessary and probably means that the pins are misaligned. If vibration resistance is needed, you can bolt the TRAM in place using the M2.5 nylon bolts provided with the mother board.

To avoid bending its pins, the IMS B419 must be kept as flat as possible when being removed from the mother board. Gently ease up one end of the TRAM a little, then ease up the other end by the same amount. Continue this until the TRAM comes free from its socket.

A.1 Subsystem Pins

The IMS B419 TRAM has a *subsystem* port (section 3.1) which allows software running on the IMS B419 to reset and control other transputers and TRAMs. The signals for the subsystem port come through three extra socket pins (other than the standard TRAM pins) on the underside of the TRAM. If you wish to control other transputers or TRAMs from the IMS B419, you must install the special pin-strip in the TRAM's subsystem pin sockets: figure A.1. Some of these pin-strips are provided with the IMS B419. The TRAM is then plugged into the mother board in the same way as described above, taking care to align the subsystem pins with the corresponding holes in the mother board. Note that the subsystem pins can only be fitted when the IMS B419 is installed in a slot with subsystem capability: usually slot 0 of a mother-board.

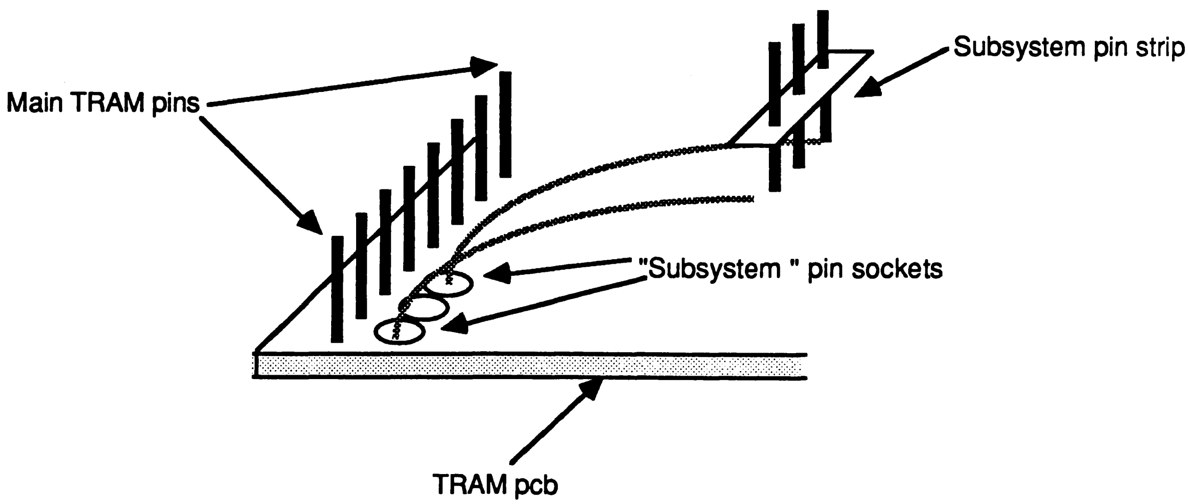

Figure A.1 Subsystem pins installation

A.2 Configuration Jumpers

Five jumper links are used to select the IMS G300 clock source and to configure the memory map of the IMS B419. Jumpers are labeled JPx, where a jumper is either installed or absent between two pin posts. The location of these is shown in figure A.3. Full details of the jumper functions can be found in the relevant sections of this manual.

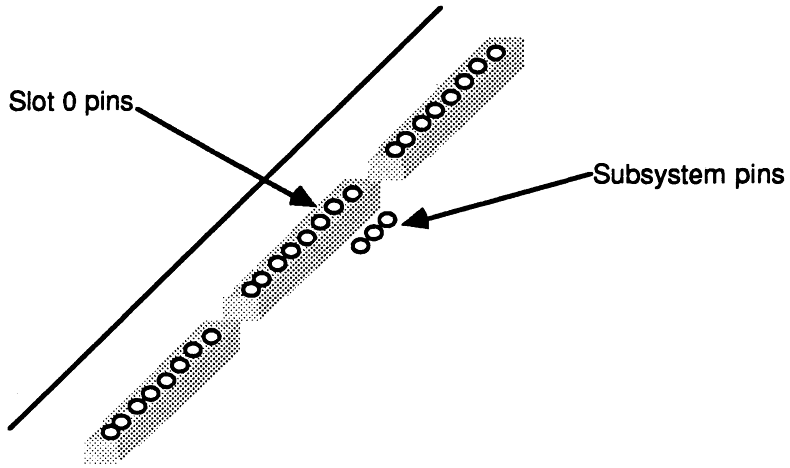

Figure A.2 Subsystem pin sockets

Jumper	Function
JP1	Always remove on IMS B419-4.
JP2	Do not fit.
JP3	Always fit.
JP4	Select contiguous VRAM.
JP5	Select non-contiguous VRAM.

Table A.1 Jumper Functions

A.3 Crystal oscillator module

A crystal oscillator module must be fitted when pixel rates which are not a multiple of the 5MHz TRAM clock are required. The oscillator module is located as shown in fig A.3, and is socketed for easy replacement. Suitable oscillator modules are available from a number of suppliers and must have the following specification:

> Output frequency in the range 5.0-9.0 MHz. 4-pin in 14-pin DIL size, TTL output, stability ±100ppm, max supply current 40mA, duty cycle 40%-60%, over a temperature 0-70 C.

A.4 External Connectors

The analogue video output signals from the IMS G300 are brought out on SMB type connectors: figure A.3. Although the video outputs are protected against ESD damage, the connectors must not be inserted or removed with the power applied as damage to the IMS G300 may result.

This type of connector employs a snap lock and require a high separation force. To avoid damage to the connectors and possibly the PCB they should be removed by pulling on the connector body with a twist action.

The *vertical sync* output provides vertical syncronisation pulses only. The *composite/horizontal sync* output provides either a composite syncronisation signal (i.e. horizontal and vertical sync pulses); or horizontal sync pulses only. This is selected by a bit in the IMS G300 control register. These signals are useful for monitors which require syncronisation signals separate from video.

The *CBLANK* connector normally outputs a video blanking signal but can also be used to input signal which will blank the IMS B419's video outputs. In order for this to work, CBLANK must be programmed as an input by writing bit 16 of the IMS G300B control register with 0.

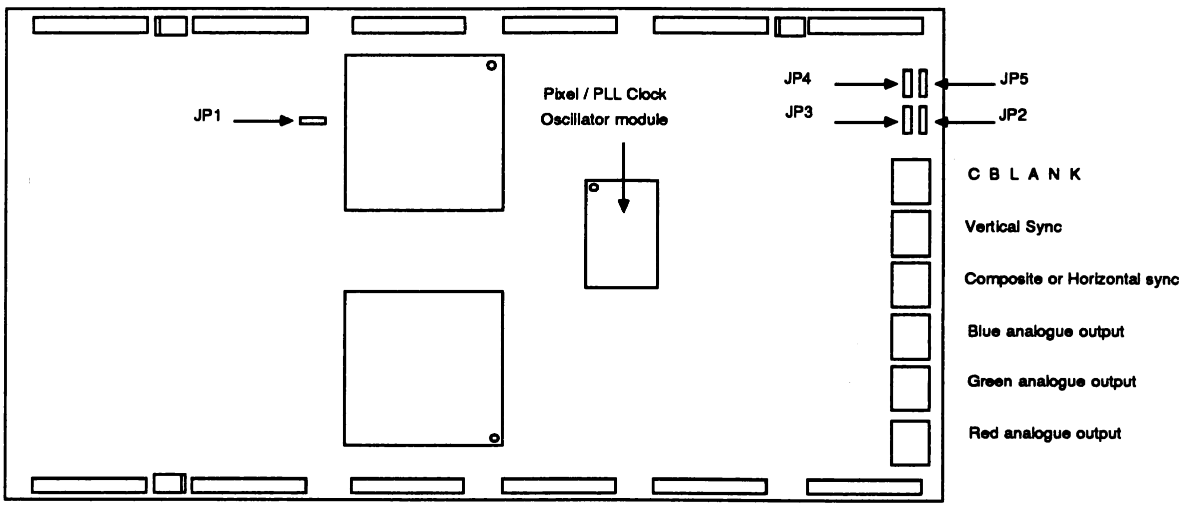

Figure A.3 Jumper positions and External connectors

B Differences in the IMS B419-3

This manual describes the IMS B419-4 which is fitted with the IMS G300B. This section describes the differences specific to the IMS B419-3 which was fitted with the IMS G300A.

B.1 Limitations

Pixel Clock Speed Boards fitted with the IMS G300A are capable of operation only between 65MHz and 110MHz (with 110MHz IMS G300A).

Pixel Width selection The IMS G300A does not allow other than 8 bits/pixel. The select bits in the control register have no effect.

PLL disable jumper The IMS G300A has no means of enabling and disabling the PLL from software. On the IMS B419-3 this selection is made by JP1. The PLL is disabled when JP1 is fitted. On the IMS B419-4, JP1 should never be fitted.

CBLANK connection The IMS G300A has no **CBLANK** connection. No connection should be made to the *CBLANK* connector (previously called the *reserved* connector) on the IMS B419-3.

B.2 Software Compatibility

Software which is written for the IMS B419-4 (IMS G300B) should be found to be compatible with the IMS B419-3 (IMS G300A). It is recommended that all new software be written for the IMS G300B. However, those parts of software which program the IMS G300A on the IMS B419-3 will need to be changed before that software will run correctly on the IMS B419-4. The following summary describes the changes which must be made.

PLL multiplier Bit 5 of the IMS G300B boot location enables and disables its PLL. It must be set (1) to enable the PLL. Hence, the boot location on the new board must be written with the required clock multiplier *plus 32*.

CBLANK connection The IMS G300B has a composite blank signal (**CBLANK**) which can be programmed to be either an input or an output. This signal is available on what was previously the *reserved* connector. Unless you are driving this signal from an external source with the intention of blanking the IMS B419's output, **CBLANK** must be programmed to be an output. This is done by writing bit 16 of the IMS G300B control register with 1.

Pixel Width The IMS G300B supports pixels of 1, 2, 4, and 8 bits. To select 8 bit pixels for compatibility with existing drawing software, bits 17 and 18 of the IMS G300B control register must both be written with 1. Refer to the IMS G300B data sheet for details of how to select other pixel widths.

C Mechanical, Electrical and Thermal Details

C.1 Operating and Storage Environment

Adequate air flow must be provided to maintain the components on the board within their operating temperature. Air flow should run parallel to the board surface, and along the length of the board.

A single board operating in static air at room temperature (and not in a card-cage) will usually not need forced air cooling. This kind of set-up should only be used for lab and development work. High reliability is not to be expected from boards which are not provided with adequate cooling.

	Operating	Storage
Temperature	+10 to +40°C ambient air	0 to +70°C
Relative Humidity	95% non condensing	95% non condensing
Thermal Shock	< 0.08°C/s	< 0.15°C/s
Altitude	−300 to +3000m	−300 to +16000m

Figure C.1 Environmental Details

C.2 Power Supply

The IMS B419 requires a power supply voltage of between 4.75V and 5.25V, with less than 50mV pk-pk noise and ripple between dc and 10MHz. The IMS B419 does not incorporate protection against incorrect power supplies. Major damage can result from operating the board outside its power supply range.

C.3 Connectors and Cable types

Good picture quality can only be obtained by using 75Ω coaxial cable for the video and sync signals. This cable, and the SMB and BNC connectors are available in most countries from third-party vendors. You may find it hard to obtain 75Ω SMB connectors: in this case, 50Ω SMB connectors may be substituted with no visible signal degradation. Note that you must still use the correct, 75Ω cable.

Cable type RG 179: 75Ω, PVC outer sheath.

SMB Dubilier/Greenpar No.B65A01G022X99 Straight connector.

SMB DUbilier/Greenpar No.B65B02G022X99 Elbow connector.

BNC Dubilier/Greenpar No.37141 D22 BN. 0.1in. diameter cable entry.

Note that INMOS does not guarantee that these part numbers are correct.

C.4 Pin descriptions

Pin	In/Out	Function	Pin No.
System Services			
Vcc, GND		Power supply and return	3,14
ClockIn	in	5MHz clock signal	8
Reset	in	Transputer reset	10
Analyse	in	Transputer error analysis	9
notError	out	Transputer error indicator (inverted)	11
Links			
LinkIn0-3	in	INMOS serial link inputs to transputer	13,5,2,16
LinkOut0-3	out	INMOS serial link outputs from transputer	12,4,1,15
LinkspeedA,B	in	Transputer link speed selection	6,7

Table C.1 IMS B419 Pin designations

Notes:

1 Signal names are prefixed by **not** if they are active low; otherwise they are active high.

2 Details of the physical pin locations can be found in Fig. C.5.

LinkOut0-3 Transputer link output signals. These outputs are intended to drive into transmission lines with a characteristic impedance of 100Ω. They can be connected directly to the **LinkIn** pins of other transputers or TRAMs.

LinkIn0-3 Transputer link input signals. These are the link inputs of the transputer. Each input has a 10kΩ resistor to **GND** to establish the idle state, and a diode to **Vcc** as protection against ESD. They can be connected directly to the **LinkOut** pins of other transputers or TRAMs.

LinkSpeedA, LinkSpeedB These select the speeds of **Link0** and **Link1,2,3** respectively. Table C.2 shows the possible combinations.

LinkSpeedA	LinkSpeedB	Link0	Link1,2,3
0	0	10 Mbits/s	10 Mbits/s
0	1	10 Mbits/s	20 Mbits/s
1	0	20 Mbits/s	10 Mbits/s
1	1	20 Mbits/s	20 Mbits/s

Table C.2 Link speed selection

ClockIn A 5MHz input clock for the transputer and CVC. The transputer synthesises its own high frequency clocks. **ClockIn** should have a stability over time and temperature of 200ppm. **ClockIn** edges should be monotonic within the range 0.8V to 2.0V with a rise/fall time of less than 8ns.

Reset Resets the transputer, and other circuitry. **Reset** should be asserted for a minimum of 100ms. After **Reset** is deasserted a further 100ms should elapse before communication is attempted on any link. After this time, the transputer on this TRAM is ready to accept a boot packet on any of its links.

Analyse is used, in conjunction with **Reset**, to stop the transputer. It allows internal state to be examined so that the cause of an error may be determined. **Reset** and **Analyse** are used as shown in figure C.3. A processor in analyse mode can be interrogated on any of its links.

notError An open collector output which is pulled low when the transputer asserts its Error pin. **notError** should be pulled high by a 10kΩ resistor to **Vcc**. Up to 10 **notError** signals can be wired together. The combined error signal will be low when any of the contributing signals is low.

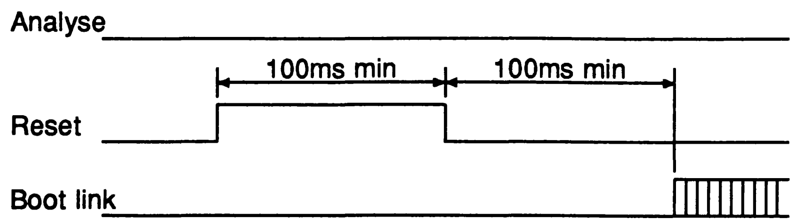

Figure C.2 Reset timing

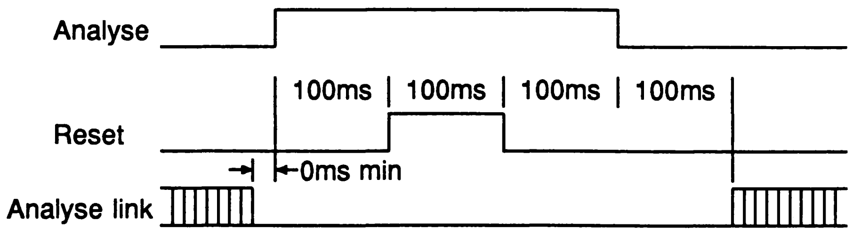

Figure C.3 Analyse timing

C.5 Specification

TRAM feature		Unit	Notes
IMS T800 transputer	1		
IMS G300 CVC	1		
200ns cycle, dual port, display RAM	2	Mbytes	
200ns cycle, workspace DRAM	2	Mbytes	
TRAM size	6		
Length	3.66	inch	
Width	6.55	inch	
Pitch between pins	3.30	inch	
Component height above PCB	9.2	mm	
Component height below PCB	3.5	mm	1
Weight	175	g	
Storage temperature	0–70	oC	
Operating temperature	10–40	oC	
Power supply voltage (Vcc)	4.75–5.25	Volt	
Power consumption (Max)	10	W	

Table C.3 IMS B419 specification

Notes:

1 This dimension includes the thickness of the printed circuit board.

C.6 Dimensions

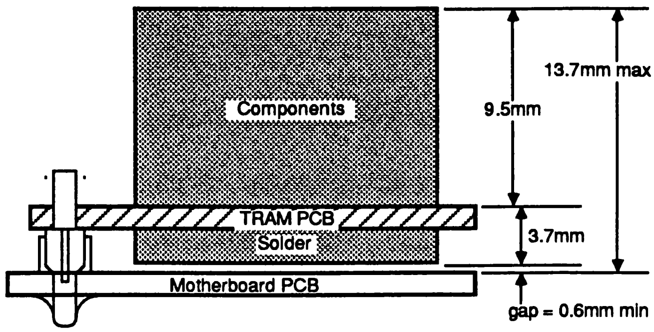

Figure C.4 IMS B419 height specification

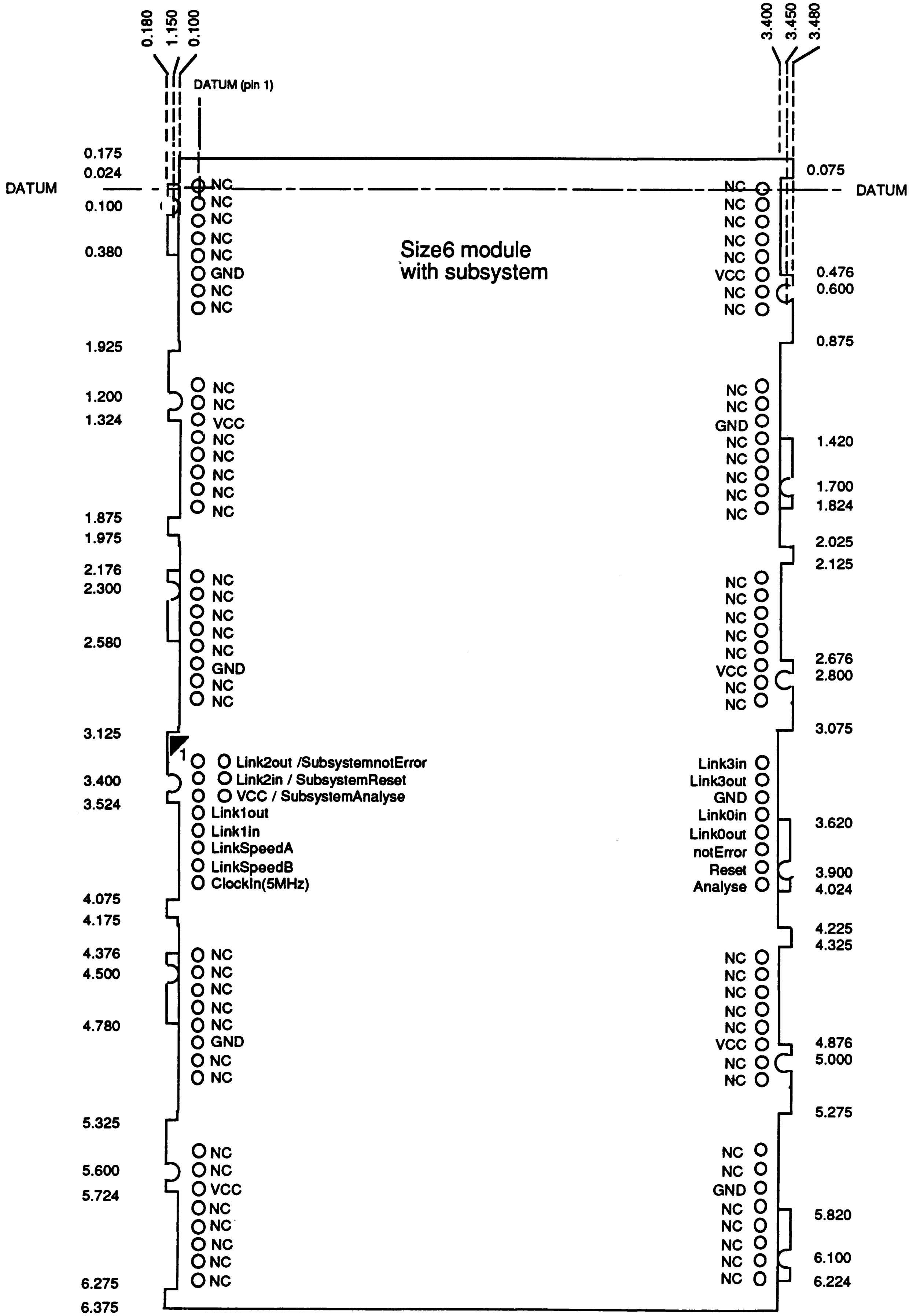

Figure C.5 Size 6 TRAM profile and pinout

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B419-4 Errata

Manual Error

The maximum pixel clock frequency available from the B419-4 is 100MHz, not 110MHz, as stated in the User Manual.

G300

Users wishing to program the G300 directly (ie not using the F003 functions) should consult the G300 Datasheet and Bug List.