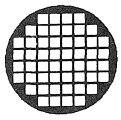

IMS B011 Transputer VMEbus board

Whilst every effort has been made to ensure the accuracy of the information given in this document, it describes a product under current development and is therefore subject to change at any time. INMOS Limited can accept no liability whatsoever for any loss or damage arising from the use of information contained herein.

The IMS B011 board has been designed by both INMOS Limited and Tadpole Technology plc, and is being manufactured by Tadpole Technology.

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The IMS B011 transputer board is a high performance parallel processor card for applications in the system level market. It performs all communications between a system bus and an array of transputers. Expansion connectors on the board are compatible with the INMOS series of evaluation boards and INMOS DIT (Dual In-line Transputer) modules. In this way the IMS B011 can provide a bridge between facilities readily available on main system buses, for example hard disc storage or industrial controllers and a large transputer array. The board is suitable for use as a main system processor, a specialised accelerator within existing systems and as a transputer development environment. The board is based around the INMOS IMS T414 32 bit transputer, and has been designed to be upgradable to the IMS T800 32 bit transputer with floating point which will become available in 1987.

1.1 Specification

Main Processor:	1 IMS T414 32 bit transputer.
Memory:	2 MB Dual ported Dynamic RAM. Parity protection.
EPROM:	4 27128 - 27512 EPROMS. Maximum 256K.
Bus Interface:	VME Bus Revision C. System Master. Bus Master/Slave. Interrupt Handler.
RS232:	2 RS232 ports with RTS/CTS handshaking
Link Adapter:	1 Ported to VME Bus
Expansion:	2 INMOS DITmodule slots INMOS Evaluation Board DIN 41612 expansion connector Site for IMS C004 programmable link switch

The IMS B011 is intended as a transputer entry into the OEM board level market. Its major design goal is to be a self-contained VME Bus master interfacing to a larger transputer array. The board can also be used as a transputer-based development environment within an existing VMEbus system.

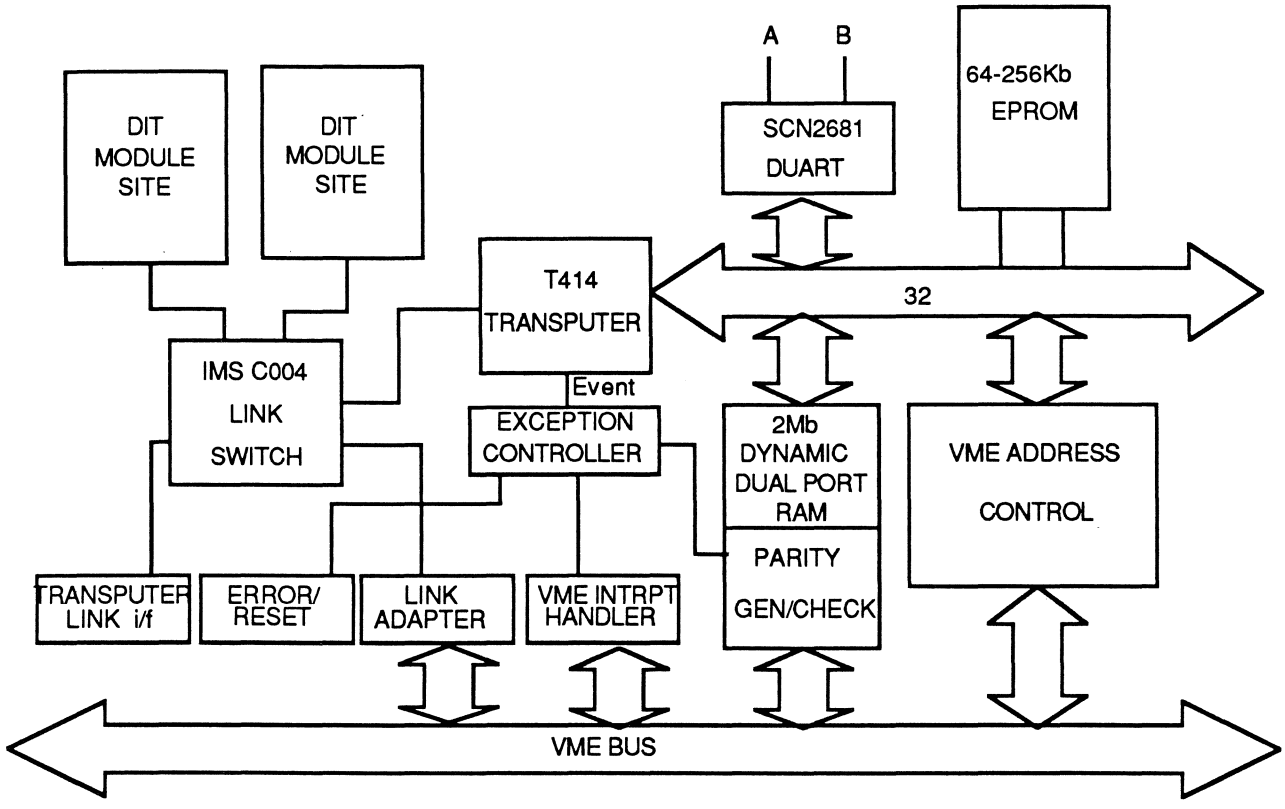


Figure 1 IMS B011 architecture

2.1 Processor

The IMS T414 is a 32 bit processor with 2Kbytes of on-chip static RAM. It is capable of addressing 4 Gbytes of memory with a maximum data rate of 25 MBytes/s. The transputer has four high speed (10 or 20Mbits/s) serial links which can be connected to transputers or via link adapters to other peripherals. The IMS T414 can be replaced by the IMS T800, a 32 bit transputer with on-chip floating point processor and 4Kbytes of internal RAM, when it becomes available.

2.1.1 Clock

The transputer clock is derived from a 5MHz oscillator which is multiplied within the transputer to drive the processing element and communication links at 20MHz.

2.1.2 Links

The transputer has four bidirectional serial links through which data can be transferred to memory using a fast DMA. The links operate independently of the processing element so that use of the links does not slow processor performance. The links have a default speed of 10 Mbits per second, which achieves a typical data transfer rate of 400Kbytes/sec between the on-chip memory of two transputers. The links can be optionally operated at speeds of 5Mbits/sec or 20 Mbits/sec, using jumpers 6,7 and 23. The speed for link 0 can be set separately from links 1,2 and 3. Note that 5 and 20 Mbits/sec cannot be selected at the same time on one transputer.

Speed Settings for Link0		
LK 6	**LK 23**	**Speed (Mbits/s)**
open	open	20
open	made	5
made	open	10
made	made	10

Speed Settings for Link123		
LK 7	**LK 23**	**Speed (Mbits/s)**
open	open	20
open	made	5
made	open	10
made	made	10

Table 1 INMOS link speed selection

2.1.3 Reset and Analyse

The transputer is reset under four circumstances: an actual board reset received from the front panel switch, on VME SYSRESET, on a VME software reset and on receipt of a DownNotReset signal from the P2 edge connector. (The P2 edge connector signals are explained fully in section 2.8 Expansion.)

At board reset the transputer Reset signal is held high while the Analyse signal is held low. This causes the transputer to perform internal reset. During reset the transputer aborts any process that was executing and any output through the INMOS links, re-initialises its memory interface and holds its INMOS link outputs to ground.

The transputer Analyse signal can be activated via the front panel switch, by the VME Analyse port or via the DownNotAnalyse signal. If the transputer receives the Analyse signal it will wait until the currently executing processes are descheduled before halting, typically 1-2 milliseconds. It can then be Reset before Analyse is removed. The memory interface is not reinitialised and refresh continues. This form of reset is intended for debugging purposes.

Once the transputer has been reset in any way it will test jumper 10 to decide its booting strategy, as outlined in Section 2.1.4.

2.1.4 Booting

The transputer can boot in two ways, from external ROM or down one of the INMOS links. At boot time the transputer examines jumper 10. If the jumper is open the transputer will boot from ROM memory. Execution begins at location #7FFFFFFE which would normally contain a backward jump to the initialisation code up to 256 bytes lower in the memory, which would then call the main program elsewhere in the ROM. The start of on board ROM is at #7FFFC000.

If jumper 10 is in place the transputer will expect to boot from an INMOS link. Booting can take place from any of the links. The transputer listens through all of the links; when it receives a byte, value two or more, this is taken to be the number of bytes to be downloaded and booting begins. First byte values of zero or one have special meanings, that are detailed in the transputer reference manual. The transputer will then load the specified number of bytes starting at location #80000048; when loading has completed control is transferred to location #80000048 to execute the newly downloaded code.

In order to be able to boot the transputer from a link when the IMS C004 Link Switch is in place, Link 0 of the IMS T414 can be jumpered optionally to enable the transputer to be booted from the VMEbus via the IMS C012 link adapter or from an external link via Link 0 of the P2 edge connector.

LK 26	LK 27	LK 28	LK 29	T414 Link 0
1-2	2-3	2-3	1-2	Link Adapter
2-3	1-2	1-2	2-3	P2 Link 0

Table 2 Transputer boot link selection

2.1.5 Events

The transputer can be made aware of changes on the board using events. Events can be generated by the parity protection circuitry on the main RAM, the SC2681 DUART device, VME Bus error, and the seven levels of VME interrupt. When an event occurs the event handler logic will place an Event Status Code at location #10000. The event code has the following format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bus Error	DUART Intr	Parity Error	VME Interrupt Level vme2	vme1	vme0	Unused	Unused

Table 3 Event status code byte

Bit 7 of the Status Code being low indicates that a VME Bus error has occured. A VME Bus error is generated when the transputer or another VME Bus master tries to access a VME address where there is no memory. If this bit is active following a read operation of a VME bus address the data read is invalid. If this bit is active following a write operation to a VME bus address it should be assumed that the write operation has not occurred. The Bus Error Bit is cleared by setting bit 5 of the DUART output port to 1, then returning the bit to 0.

Bit 6 of the Status Code being low indicates that a DUART interrupt condition is pending. The DUART can be programmed for interrupt conditions on character receipt or transmission, timer and status change on its input port. The DUART interrupt bit is cleared when the interrupt condition on the SC2681 has been resolved.

Bit 5 of the Status Code being low indicates that a parity error has occurred while the transputer has been accessing the on-board RAM array. Note that all locations must first be written before they are read; this is in order to allow the parity protection hardware to generate a valid parity bit for the word being written. To clear the parity error bit, set bit 6 of the DUART output port to 1 then reset the bit to 0.

Bits 4 to 2 of the Status Code represent the VME interrupt level (0-7) of the highest pending VME interrupt. To acknowledge the interrupt and also find the interrupt vector number the event handler must perform a software VME interrupt acknowledge cycle by reading location #A0200000. The least significant byte of the word read is the VME interrupt vector from the interrupter. See section 2.4.3 concerning the VME Interrupt Handler.

To make use of the event facility an OCCAM channel should be assigned to the transputer's event pin using the construct

```
PLACE event AT 8
```

The event handler can then use the event pin as a trigger in order to begin execution. Use the OCCAM construct

```
event ? signal
```

The event handler will then remain inactive until an event occurs. When the event occurs the event handler will be restarted within a maximum of 58 processor cycles provided no other high level processes are executing. The event handling process should read the Event Status Code and decide the appropriate action.

When the transputer event software has ensured that the interrupting source has been dealt with, and the interrupt turned off, the event done bit must be cleared to low then set high. This is in the DUART output port, bit 7.

The process that waits on the event pin should be a high priority process to ensure that it will complete within a given period. It should also be aware of all the sources of events on the board or the VME bus.

2.1.6 Memory map

Table 4 is a memory map of the IMS B011 as viewed by the IMS T414 on-board. Occam programmers should note that occam address 0 is equivalent to the transputer address #80000000. Thus addresses run from #80000000 through #FFFFFFFF, then #00000000 up to #7FFFFFFF, a signed address space.

Transputer byte address	Description
#80000000	2K transputer On-chip Static RAM
#800007FF	2MB Parity Protected DRAM Dual Ported to VME Bus
#80200000	126MB VME Bus Extended Address Space (32A/32D)
#88000000	128MB VME Bus Byte Addressable (byte 0)
#90000000	16MB VME Bus Standard Address Space (24A/32D)
#91000000	64KB VME Bus I/O Space (16A/32D)
#92000000 #98000000	16MB VME Bus Byte Adressable (byte 0) (24A/8D)
#99000000	64KB VME Bus Byte Addressable (byte 0) (16A/8D)
#9A000000 #A0200000 #A8000000	Software VME Interrupt acknowlege 128MB VME Bus Byte Addressable (byte 1) (32A/8D)
#B0000000 #B8000000	16MB VME Bus Byte Addressable (byte 1) (24A/8D)
#B9000000	

Table 4 The on-board transputer memory map

Transputer byte address	Description
#B9000000	
	64KB VME Bus Byte Addressable (byte 1) (16A/8D)
#C8000000	
	128MB VME Bus Byte Addressable (byte 2) (32A/32D)
#D0000000	
#D8000000	
	16MB VME Bus Byte Addressable (byte 2) (24A/8D)
#D9000000	
	64KB VME Bus Byte Addressable (byte 2) (16A/8D)
#E8000000	
	128MB VME Bus Byte Addressable (byte 3) (32A/8D)
#F0000000	
#F8000000	
	16KB VME Bus Byte Addressable (byte 3) (24A/8D)
#F9000000	
	64KB VME Bus Byte Addressable (byte 3) (16A/8D)
#00000000	Subsystem RESET/ERROR (bit D0)
#00000004	Subsystem ANALYSE/ERROR (bit D0)
#00008000	SCN2681 DUART device (only data bits D0-D7 valid)
#00008040	
#00010000	Event Status Code (bits D0-D7)
#7FFFC000	
	256K EPROM
#7FFFFFFF	

Table 4 (cont) The on-board transputer memory map

2.2 Main memory

The IMS B011 contains a main RAM array of 2 Mbyte constructed from 72 256 Kbit Z packaged devices. The main RAM array is parity protected: a parity bit is generated when a location is written then regenerated when the location is next read. If the parity bits do not match an error is logged. If the memory access was from the VME Bus the *BERR signal is set. If the access was by the main IMS T414 it will receive an event input. The whole memory array is dual ported to the VME Bus and is address selectable to a resolution of 2 MByte.

2.2.1 Memory architecture

The on board memory is configured as a 32 bit wide array. The IMS T414 performs 5 cycle accesses to the memory. This gives a cycle time of 250 nS at 20 MHz. On read cycles the transputer will always read a full 32 bit word from memory and internally select which bytes it requires. The dual port memory supports VME bus locking for indivisible read - modify - write (RMW) type cycles. The transputer has no means of performing indivisible cycles.

Access to the dual port memory is controlled by an arbiter which will give priority to the IMS T414. The memory control is arranged so that at the end of a transputer memory cycle any pending VME bus cycle will be granted

2.2.2 Parity protection

When writing to memory, hardware generates a parity bit for each byte of data written. During a read cycle a new parity bit is generated and checked against the existing parity bit to determine if an error has occurred. On write cycles, only the individual bytes written have parity bits updated. All internal read accesses to the memory array are 32 bits wide so during a read cycle a full 32 bit word is read and new parity bits are generated and checked against the existing parity bits. Note that parity errors are only generated during read cycles.

If a memory access by the on board IMS T414 generates a parity error an event is generated and bit 5 of the Event Status Code byte will be active. To clear this error the IMS T414 must set bit 6 of the DUART output port to 1, then reset that bit 6 to 0. See section 2.1.5 Events.

If the memory access that caused a parity error was from another VME master the IMS B011 will acknowledge the cycle with the VME BERR* signal.

On power up the parity clear bit of the DUART output port is set to 1. This ensures no on board parity checking for the IMS T414 until software specifically enables it by setting the output bit to 0.

After a power-up reset the contents of the main memory and parity protection bits are invalid. Any read access to a location at this time is liable to cause a parity error. To ensure a correct parity bit is generated for each byte, each word location must be written before it is read. This point is especially important in systems that attempt to size the amount of memory on the bus at power-up.

Parity checking can be totally disabled by removing jumper LK16.

2.2.3 VME addressing

As a Bus Master, the IMS B011 supports all 3 types of VME address space. As a Bus Slave, it supports Standard and Extended addressing. The master interface allows access to VME boards with all data bus widths, d8, d16 and d32. The address map in Table 4 above shows the areas where VME accesses are mapped.

The VME Bus appears a number of times within the memory map. Each occurrence represents a different mode of access to the Bus. For example, Extended Access allows the transputer access to a 32 bit address space using 32 bit data. The Standard and Extended Address spaces should be used to access 32 bit data; these address spaces are ideal for expansion memory or buffer space on the VME Bus.

The IMS T414 transputer has been designed with a 32 bit data path and interface: all its data transactions are performed in multiples of 32 bits. The IMS T414 can write to individual bytes within a word but must read a whole 32 bit word. Many VME based controllers use byte locations for control and status registers. In particular, certain byte locations are used as latches, so any access to them can start or stop the controller. Using the transputer, it is possible to unintentionally access a control latch when the intended register is within the same 32 bit word. Another problem is addressing VME boards which support only 8 or 16 bit data accesses. To prevent these problems a number of the VME address spaces have a data path of 8 bits external to the board whilst internally on the board they appear to the transputer to have a 32 bit data path. These different VME address spaces represent different bytes within a word in the Standard, Extended and I/O VME address spaces.

The IMS B011 dual port RAM can be configured to start on any 2 Mbyte boundary within either the standard or the extended address spaceof the VMEbus. The 8 way DIL switch SW3 is used to set the address space

and address modifier required. Table 5 below defines the function of the individual switches.

Switch SW3 - Slave decode		
Switch position	**function**	
1	A27	Compares to '1' if OFF
2	A26	Compares to '1' if OFF
3	A25	Compares to '1' if OFF
4	A24	Compares to '1' if OFF
5	A23	Compares to '1' if OFF
6	A22	Compares to '1' if OFF
7	A21	Compares to '1' if OFF
8	Address modifier	Extended address space if ON Standard address space if OFF

Table 5 VME address switch comparisons

In the standard address space only the address lines A21 to A23 are significant. In extended address space all address lines are significant. A28 to A31 are always compared to '0' in extended address space. This is performed in a PAL device which can be reprogrammed if required.

Example	
Address	**Switches to "off" on SW3**
#200000 (standard)	7, 8
#A00000 (standard)	5, 7, 8
#A00000 (extended)	5, 7
#4600000 (extended)	2, 6, 7

The address modifiers to which the IMS B011 responds as a slave are given in Table 6 below.

Address space	Address modifier decoded	Value
Extended	Supervisor Data	#0D
	User Data	#09
Standard	Supervisor Data	#3D
	User Data	#39

Table 6 Memory address modifiers

Note that the top 32 bytes of VME dual port memory are used for the link adapter status and the VMEbus Subsystem control registers (see Section 2.7). Care should be taken to avoid using these locations from the VMEbus except when communicating with the Subsystem port and the link adapter.

2.3 Serial interface and control I/O

2.3.1 Description

Two asynchronous RS232 ports are provided on the IMS B011. The ports are implemented using a 2681 DUART. This device has two RS232 ports with handshaking, counter/timer and parallel I/O bits. The counter/timer may be used to generate a periodic event for use in real-time systems. The device is clocked from a 3.6864 MHz oscillator, allowing baud rates of between 50 and 38.4K baud to be selected. Figure 2 shows the DUART architecture.

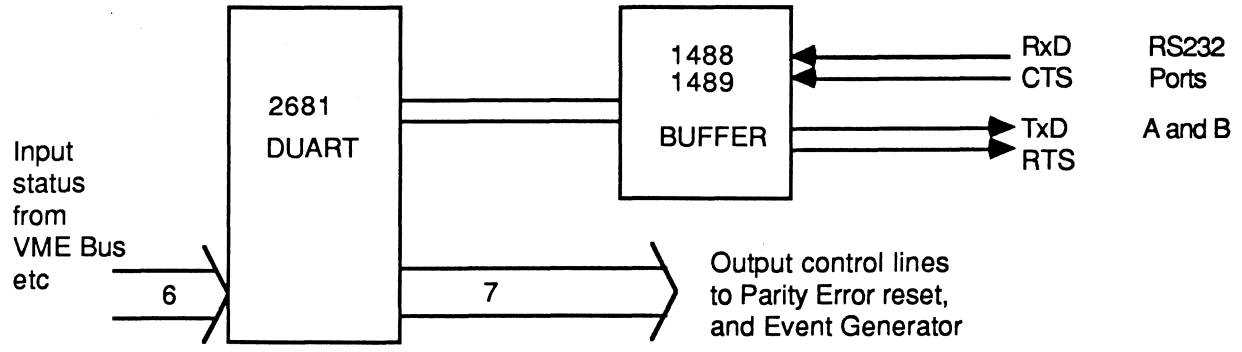


Figure 2 DUART architecture

The IMS B011 uses the DUART control lines as shown in Table 7.

PIN	Signal	Description
IP0	CTS channel A	handled automatically by 2681
IP1	CTS channel B	handled automatically by 2681
IP2	VME SYSFAIL	indicates VME system failure
IP3	VME ACFAIL	power failure to system
IP4		
IP5		
IP6		
OP0	RTS channel A	handled automatically by 2681
OP1	RTS channel B	handled automatically by 2681
OP2		
OP3	VME SYSFAIL	asserted to indicate board failure
OP4		
OP5	VME BERR reset	used to clear VME Bus Error
OP6	Parity Error reset	used to restart Parity Checking on main RAM
OP7	Event done	used to indicate event dealt with

Table 7 2681 control lines

2.3.2 Register set

The 2681 Register set is given in Table 8. The main functions of each register are described below.

Read register	Write register	Address
Mode Register A (MR1A,MR2A)	Mode Register A (MR1A,MR2A)	#00
Status Register A (SRA)	Clock Select Register A (CSRA)	#04
Reserved	Command Register A (CRA)	#08
Rx Holding Register A (RHRA)	Tx Holding Register (THRA)	#0C
Input Port Change Reg (IPCR)	Auxiliary Control Reg (ACR)	#10
Interrupt Status Reg (ISR)	Interrupt Mask Register (IMR)	#14
Counter/Timer Upper (CTUR)	Counter/Timer Upper (CTUR)	#18
Counter/Timer Lower (CTLR)	Counter/Timer Lower (CTLR)	#1C
Mode Register B (MR1B,MR2B)	Mode Register B (MR1B,MR2B)	#20
Status Register B (SRB)	Clock Select Register B (CSRB)	#24
Reserved	Command Register B (CRB)	#28
Rx Holding Register B (RHRB)	Tx Holding Register (THRB)	#2C
Reserved	Reserved	#30
Input Port	Output Port Config Reg (OPCR)	#34
Start Counter Command	Set Output Port Bits Command	#38
Stop Counter Command	Reset Output Port Bits Command	#3C

Table 8 2681 register description

The address of each register is aligned to 32 bits and is shown in Table 8 as relative to the start address for the DUART. Only data bits D0-D7 of the word are valid.

A detailed description of the programming of the 2681 device is beyond the scope of this manual and reference should be made to the Bibliography in Appendix B. The following is a brief description of the DUART register set.

Mode registers

Mode Register 1 controls RTS, mode of receive events, error and parity codes and the number of bits per character. Mode Register 2 controls the Channel mode, RTS and CTS control and the stop bit length. Device accesses normally result in read/write of Mode Register 2 but a RESET or a Reset pointer command will allow a single read or write operation to Mode Register 1.

Channel clock select registers

The Channel Clock Select register selects the baud rates of each individual channel. The baud rate for each channel may be individually set, and the transmit speed may differ from the receive speed.

Channel command registers

The Channel Command Register is used to issue a command or commands to the DUART device. Commands available include error reset functions, break functions and the enabling/disabling of the individual channel transmitter/receivers.

Channel status registers

The Channel Status registers allow the on-board processor to read status information about the DUART device. Status conditions reported include Received Break, line communication errors and the transmitter and receiver status.

Output port configuration register

The 2681 devices include input and output ports which may be used for RS232 control or general purpose I/O functions. The OPCR programs the usage of the various output port bits.

Auxiliary control register

The Auxiliary Control Register programs the on-chip baud rate generator, and the conditions that cause the input port to generate events.

Input port change register

This register contains the current state, and any change of state on the input port pins for the DUART device.

Interrupt status register

The Interrupt Status Register indicates the current status of the various conditions which can cause an interrupt on the 2681 device. These include Input Port Change, Receiver ready or full, and Transmitter ready. It is an interrupt condition on the 2681 which will eventually generate an Event on the transputer.

Interrupt mask register

The Interrupt Mask register allows the programmer to decide at any time which of the various interrupting conditions will actually cause an Event request to be generated.

Counter/timer registers

These registers control the counter and timers in the DUART device.

2.3.3 I/O ports

Input port

The 2681 Input Port is a 7 bit general purpose port. The IMS B011 uses this port to monitor various board status bits as shown in Table 9. Bits 0 and 1 are used as the CTS inputs for the two serial channels and are handled automatically by the 2681 device. Bit 2 indicates the state of the VME SYSFAIL signal; this signal is set by any VME Board in a system that has suffered a failure catastrophic to the rest of the system, or that has failed its start up test. Bit 3 indicates the state of the VME ACFAIL signal that may be set by any VME Board in the system that can detect a power failure.

2681 system status input port			
Bit	**Signal**	**Input pin high**	**Input pin low**
0	CTSA	CTS asserted	CTS deasserted
1	CTSB	CTS asserted	CTS deasserted
2	SYSFAIL	Normal	VME System fail
3	ACFAIL	Normal	Power fail
4			
5			
6			

Table 9 2681 input port

A read of the Input Port register will give a bit value of 0 if the corresponding input pin is Low, and a value of 1 if the input pin is high.

Output port

The 2681 Output Port is an 8 bit general purpose port. This port is used to control various system functions. Bits 0 and 1 are used as the RTS outputs for the RS232 ports. Bit 3 of the port can activate the VME SYSFAIL signal which can be used to alert other boards within a VME system that a fault has occurred. Bit 5 of the port is used to reset the VME BERR (Bus Error) signal which will occur if the on board transputer attempts to access unpopulated VME memory locations. Bit 6 is used to reset the parity detection circuitry that protects the on-board DRAM. Bit 7 is used to indicate that an event has been serviced, setting then clearing the bit will reset the event handling circuitry enabling detection of new events.

2681 System control output port			
Bit	**Signal**	**Output pin high**	**Output pin low**
0	RTSA	RTS asserted	RTS deasserted
1	RTSB	RTS asserted	RTS deasserted
2			
3	SYSFAIL	SYSFAIL asserted	SYSFAIL deasserted
4			
5	BERR-RST	Reset VME BERR	-
6	PERR-RST	Reset parity error	-
7	EVENT-DONE		Signal event handled

Table 10 2681 output port

Note that the OPCR register programs the port output bits to be the inverse of the contents of the Output Port Register.

2.3.4 RS232 outputs

The two RS232 channels are brought out to the 26 pin header P3 from which the signals can be taken off the board. See Table 11. Some of the RS232 signals are also taken to pins 19 to 26 on row C of the P2 edge connector (see section 2.8 Expansion).

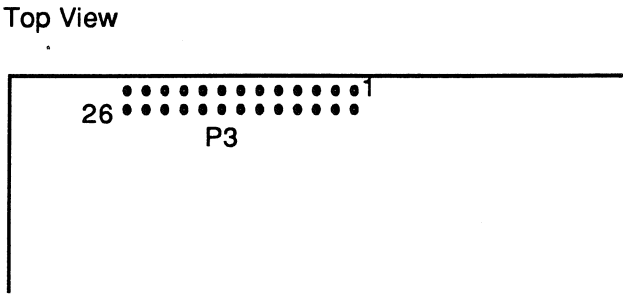


Figure 3 RS232 headers

B011 PIN	RS232 PIN	SIGNAL	SENSE	B011 PIN	RS232 PIN	SIGNAL	SENSE
1	1	NC	No connect	14	1	NC	No connect
2		NC		15		NC	
3	2	TxDA	Output	16	2	TxDB	Output
4		NC		17		NC	
5	3	RxDA	Input	18	3	RxDB	Input
6		NC		19		NC	
7	4	RTSA	Output	20	4	RTSB	Output
8		NC		21		NC	
9	5	CTSA	Input	22	5	CTSB	Input
10		NC		23		NC	
11	6	NC		24	6	NC	
12		NC		25		NC	
13	7	GND	Ground	26	7	GND	Ground

Table 11 RS232 connections

2.4 VME interface

The IMS B011 card supports the latest Rev C Specification of the VME system bus. The card is a full VME System Master, with 32 bit address and 32 bit data capability. The dual port memory also acts as a 32 bit VME slave device, allowing other bus masters to access the on-board DRAM area. For a full specification of the VME bus please refer to the bibliography at the end of this manual. The main features of the VME bus are:

- high performance bus for 32 bit systems
- 32 bit address and data bus
- compact double Eurocard format
- maximum bus bandwidth of 40MB /second
- industry standard support

This section describes the VME System and Control options and explains how to set the IMS B011 board functions.

Function	Section
VME System Master	2.4.1
VME Bus Master	2.4.2
VME Slave	2.4.4
VME Interrupt Handler	2.4.3

Table 12 IMS B011 bus functions

2.4.1 System master

The IMS B011 may act as the VME System Master, residing in slot 0 of the bus. Jumpers are provided to enable the System Master function, as shown in Table 13. The position of the jumpers is shown in Figure 4.

System master function	Enable	Disable
IMS B011 drives SYSRESET*	MAKE LK20	OPEN LK20
IMS B011 System Master	MAKE LK19	OPEN LK19

Table 13 VME System Master functions

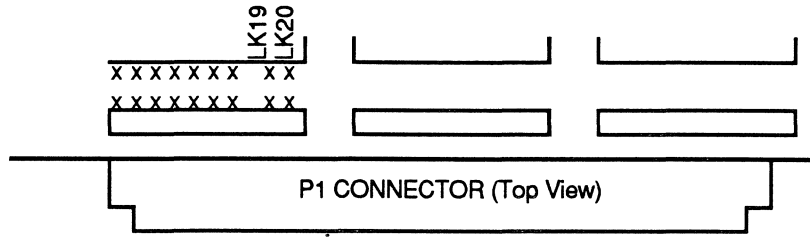


Figure 4 System Master link positions

SYSCLK*

The IMS B011 provides a 16MHz buffered SYSCLK* signal for the VME bus. The drive capability of the SYSCLK* signal is 64mA.

SYSRESET*

The IMS B011 drives the SYSRESET* line LOW (asserted) on power-up for 500mS. It also drives it when the board is reset using the front panel switch. Using the reset switch on the front panel will reset ALL the boards in a VME system if LK 20 is in place.

Bus timer

The IMS B011 provides the VMEbus timer functions. All bus cycles are monitored and any cycle which has not terminated after approximately 14mS will be detected by the IMS B011 and will be terminated by the assertion of the BERR* signal.

Priority bus arbiter with Bus Clear

The IMS B011 has a full four level bus arbiter. It drives the 4 bus grant lines and monitors the bus exchange control lines. Arbitration is performed using a simple priority scheme. If a low priority card has the bus and a higher priority request is received, the IMS B011 will assert BCLR* to request the present Bus Master to relinquish control of the bus, and will then grant the bus to the high priority requester.

IACK* daisy chain driver

The IMS B011 drives the Interrupt Acknowledge Daisy Chain down the bus. The IACKIN*/IACKOUT* daisy-chain is passed on by each card on the bus. Any card slot without a card installed should have the daisy chain strapped across on the backplane. The IMS B011 may be installed as a normal bus master/slave (not in slot 0) without jumper changes. The IACKIN*/IACKOUT* daisy chain will then be propagated in the normal way by the IMS B011.

2.4.2 VME bus master

The IMS B011 is a full bus master and is capable of accessing the VME address spaces as defined in Table 14 below. The address modifier is determined in a given cycle by the state of the 6 VME address modifier signals AM0* - AM5*. The address modifiers for the IMS B011 card are automatically generated in hardware. Since the IMS T414 does not support supervisor/user states or program/data status the IMS B011 always provides a supervisor data type address modifier. The IMS B011 does not support block move modes.

Address modifier	Bus access type
#3D	Standard Supervisory Data Access
#2D	Short Supervisory Access
#0D	Extended Supervisory Data Access

Table 14 VME Address Modifiers

Address space accesses

All accesses to the bus can use the full 32 bit data bus. Provision has been made to allow access to VME bus boards which are less than 32 bits wide. On write cycles the transputer byte write strobes are used to determine what width of cycle to perform. The transputer always performs external 32 bit reads and internally selects the byte(s) it requires. To read a single byte from a VME card the special byte read areas of VME access must be used. See Section 2.2.4 above. Standard (24 bit) and Short (16 bit) Address Spaces all have a similar provision.

The physical address which the IMS B011 asserts on the bus will be different from the address generated by the IMS T414. The top 5 address lines will be always driven low. This allows the IMS B011 to address up to 126 Mbytes of A32 memory.

Bus arbitration

The IMS B011 Bus Requester uses a Release on Request (ROR) or a Release When Done (RWD)algorithm for determining when to give up the VME bus. This is selected by jumper LK17. The bus request and grant levels are set by on-board jumper options. The bus grant input level must be set to the same value as the bus request level. There are a total of 4 levels available (Level 3 is the highest priority). LK 5 selects the Bus Request Level and LK 18 sets the Bus Grant Level. The jumper patterns for grant and request are detailed below.

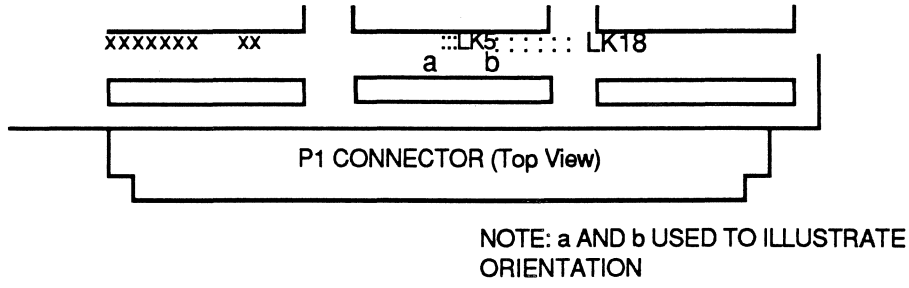


Figure 5 Bus Grant and Request jumper positions

Jumper patterns for the Bus Request level (LK5):

```
 x  x--x          Level 3        x  x  x          Level 2
 x  x  x                         x--x  x
a                               a

 x--x  x          Level 1        x  x  x          Level 0
 x  x  x                         x  x--x
a                               a
```

Jumper patterns for the Bus Grant level (LK18):

```
 x  x  x  x  x--x                x  x  x  x--x  x
 :     :  :        Level 3       :     :        :   Level 2
 x  x  x  x  x--x                x  x  x  x--x  x
b                               b

 x  x--x  x  x  x                x--x  x  x  x  x
 :        :     :  Level 1             :  :     :   Level 0
 x  x--x  x  x  x                x--x  x  x  x  x
b                               b
```

Figure 6 Bus Request/Grant level jumper patterns

2.4.3 Interrupt handler

The IMS B011 is a full VME Interrupt Handler, supporting all seven bus interrupt levels. It is possible to disable any of the interrupt levels using the jumpers LK14. Removing a jumper will disable the relevant interrupt level.

Jumper No	Interrupt level
8-7	7
9-6	6
10-5	5
11-4	4
12-3	3
13-2	2
14-1	1

Table 15 VME interrupts

When the board receives an interrupt it will generate a transputer event. Event handling software should read the Event Status Code to determine if the event was a VME interrupt and its level, which is contained in bits 2-4 of the status byte. VME interrupts are accompanied by an interrupt vector to identify the interrupt source. To find the vector and acknowledge that the board has received an interrupt software must read the relevant location in Table 16. The least significant byte contains the interrupt vector.

Address	Interrupt Level
#A020001C	7
#A0200018	6
#A0200014	5
#A0200010	4
#A020000C	3
#A0200008	2
#A0200004	1

Table 16 VME interrupt acknowledge locations

2.4.4 VME bus slave

The IMS B011 acts as a 24A or 32A/32D Slave on the VME bus. The IMS B011 acts as a VME slave when Bus Master accesses the on-board dual port memory array or the link adapter. The on-board memory may be situated at any position in the Standard or Extended address space using SW3. The memory switches and options are described fully in Section 2.2 above.

SYSFAIL*

On power-up or a hard reset the IMS B011 will assert the VME SYSFAIL* signal. This will also light the SYSFAIL* LED on the frontpanel. The signal is cleared by writing to the DUART output port (Section 2.3) to signify that the card is on-line and running.

2.5 EPROM

The IMS B011 contains 4 PROM sockets which can house 27128, 27256, and 27512 family EPROMS. This gives a maximum PROM size of 256 Kbytes.

The memory space occupied by the EPROM is determined by the setting of jumpers LK12 and LK13, as shown in Table 17.

LK 13	LK 12	Size
1-2	1-2	27128
1-2	2-3	27256
2-3	2-3	27512

Table 17 EPROM sizing

2.6 Link adapter

The IMS B011 has an IMS C012 Link Adapter which is ported onto the VME Bus as a VME Slave. A link adapter provides a byte wide parallel interface to an INMOS serial link. An overview of the IMS C012 is given here. For a more detailed description see the bibliography in Appendix B. The link from the IMS C012 may be connected to either the IMS C004 site link 3 or, by jumper selection, link 0 of the on board transputer. It can operate at 10 or 20Mbits/s, selectable by jumper LK25 as shown in Table 18.

LK 25	Speed
Make 1-2	20 MBits/s
Make 2-3	10 MBits/s

Table 18 Link adapter speed select

2.6.1 Link adapter registers

The IMS C012 Link adapter has four byte wide registers.

Register	Description	Address
Input Data	Holding register for data received from the link	#1
Output Data	Holding register for data to be sent on the link	#3
Input Status	Control for input data	#5
Output Status	Control for output data	#7

Table 19 Link adapter register set

Output data and input data

These registers hold a byte of data that is to be sent or has been received from the link.

Input status

Bit 0 of the input status register is set to 1 when data has been received on the link. The bit is reset to 0 when the data has been read from the input data register by a Master on the VMEbus.

Output status

Bit 0 of the output status register is set to 1 when the link adapter is ready to send a byte on the serial link. When a byte is written to the output data register, bit 0 of the output status register becomes 0. The bit is set to 1 when the byte of data has been successfully transmitted down the link.

Addressing

The link adapter registers appear in the top 8 bytes of the dual port RAM. To calculate the VME base address of the link adapter add #1FFFF8 to the VME base address of the dual port memory. The register addresses given in Table 19 are all relative to the VME base address of the link adapter.

Example		
VME Base address of RAM	#2200000	(34 Mb)
VME Base address of L.A.	#23FFFF8	
Input data	#23FFFF9	
Output data	#23FFFFB	
Input Status	#23FFFFD	
Output Status	#23FFFFF	

2.7 Control registers

The IMS B011 has three control registers dual ported to the VME Bus. They are transputer Error, Reset and Analyse. The registers are all one byte wide and appear at the start of the top 32 bytes of dual ported memory.

Reset

Writing a 1 to this register, base VME address plus #1FFFE3, resets the on-board IMS T414 and asserts Reset on the P2 edge connector Subsystem socket and the DITmodule sites. Writing 0 to the register deasserts the reset signal allowing the IMS T414 to bootstrap.

Analyse

Writing a 1 to this register, base VME address plus #1FFFE7, asserts the Analyse signal to the on-board IMS T414, the P2 edge connector Subsystem socket and the DITmodule sites. Writing a 0 to the register deasserts the signal.

Error

The error status of the board is echoed in the least significant bit of this register addressed at base VME address plus #1FFFE3. When the bit becomes 1 an error has occurred. The error bit is reset when the IMS B011 is reset.

2.8 Expansion

The DIN 41612 P2 edge connector performs two functions: the middle row of pins provides VME address bus signals A24 to A31 and data bus signals D16 to D31 as well as +5V and GND pins; the outer two rows of pins are compatible with the edge connectors used on several other members of the INMOS range of evaluation boards.

Table 20 shows the pinout of the P2 connector. Row B is as defined in the VMEbus specification (see bibliography). Rows A and C provide extra +5V and GND pins, four INMOS links and Up, Down and Subsystem signals, which allow interconnection and control of transputer boards as explained below. Most of the signals from the two RS232 ports are also brought out to the P2 connector.

2.8.1 Links

Of the four links on the P2 connector links 1, 2 and 3 are connected directly to the IMS C004 link switch site, as shown in Table 21. P2 Link 0 can be connected to the link switch site or to link 0 of the transputer, depending on the setting of jumpers LK26 to LK29, as described in section 2.1.4 Booting.

2.8.2 Up, Down and Subsystem

The Up, Down and Subsystem signals provide transputer system control so that it is possible to initialize and analyse errors in an arbitrarily large system of evaluation boards. This control is independent of the serial links between boards.

One board can control a subsystem of an arbitrary number of boards by connecting its Subsystem socket to the Up socket of the next board. Each of the boards in a subsystem can itself control a further subsystem, as in the hierarchy of boards in Figure 7. A cable is supplied with the IMS B011 which may be used to connect its Up, Down or Subsystem socket to other boards.

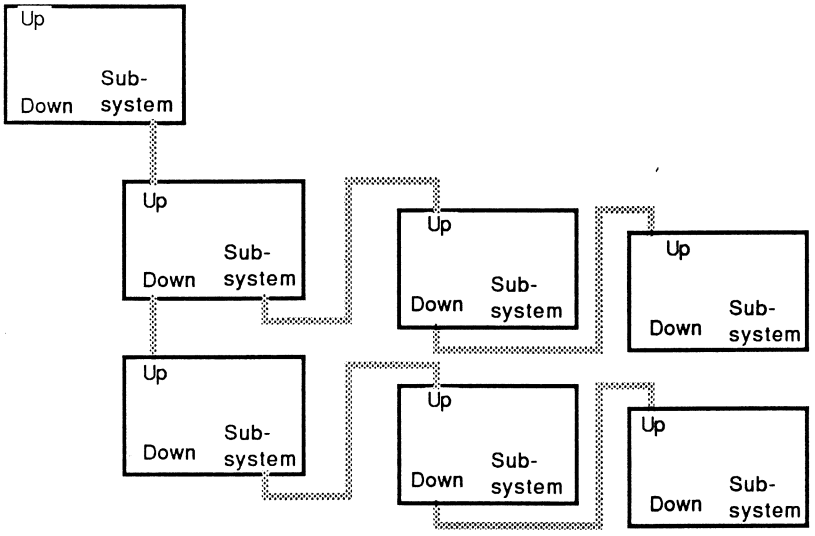


Figure 7 Hierarchy of boards

Each of the sockets includes the signals notReset, notAnalyse and notError. The notReset and notAnalyse signals flow in the direction of the arrows in Figure 8. The notError signal flows in the reverse direction from Down to Up and indicates that an error has occurred on this board or on a board further down the chain. All the inputs are biased so that if a socket is not used the signals it receives are in their inactive state. The Subsystem notError signal is not propagated Up because the board controlling the subsystem should deal with the error.

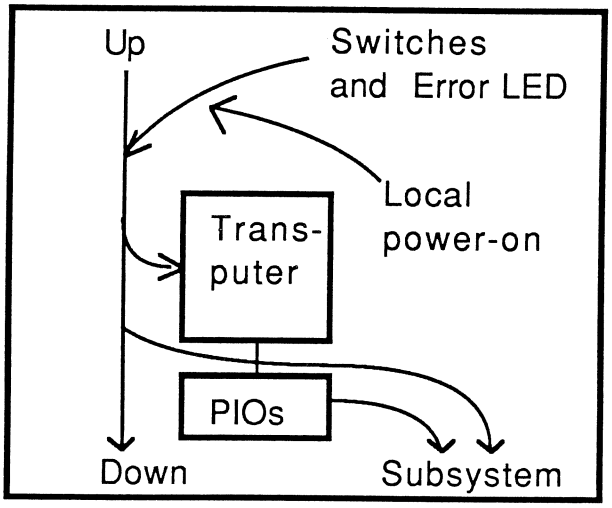


Figure 8 Direction of Reset, Analyse and Error

The pin-out of the P2 connector is shown in Table 20.
Blank indicates no connect.

Pin Number	Row C	Row B	Row A
1	GND	VCC	GND
2	VCC	GND	VCC
3		RESERVED	
4	VCC	A24	VCC
5	GND	A25	GND
6		A26	
7	GND	A27	GND
8		A28	
9	LinkOut[0]	A29	LinkOut[1]
10	LinkIn[0]	A30	LinkIn[1]
11	GND	A31	GND
12		GND	
13	GND	VCC	GND
14		D16	
15	LinkOut[2]	D17	LinkOut[3]
16	LinkIn[2]	D18	LinkIn[3]
17	GND	D19	GND
18		D20	
19	TxA	D21	
20	RxA	D22	
21	GND	D23	
22	TxB	GND	Subsystem Reset
23	RxA	D24	Subsystem Analyse
24	GND	D25	Subsystem Error
25	RTS B (output)	D26	GND
26	CTS A (input)	D27	
27		D28	
28	UpReset	D29	DownReset
29	UpAnalyse	D30	DownAnalyse
30	UpError	D31	DownError
31	GND	GND	GND
32	GND	VCC	GND

Table 20 P2 edge connector pinout

2.8.3 Programmable link switch (IMS C004)

Most of the INMOS links on the board are passed through the IMS C004 site. This allows each user to tailor the board to his particular application. The IMS C004 programmable link switch allows software configuration of link connections. In the absence of an IMS C004 a wirewrap header is provided to facilitate the hardwiring of links.

Link	Patch panel ref	C004 connection (provisional)
Transputer		
T414 Link0In		No Connection
T414 Link0Out		No Connection
T414 Link1In	E1	Link 0 Out
T414 Link1Out	B2	Link 0 In
T414 Link2In	E3	Link 1 Out
T414 Link2Out	B3	Link 1 In
T414 Link3In	J2	ConfigLinkOut
T414 Link3Out	H3	ConfigLinkIn
Link Adapter		
C012 LinkIn	(D1)	(Link 3 Out) *
C012 LinkOut	(C4)	(Link 3 In)
Module 1		
Link0In	C1	Link 4 Out
Link0Out	A2	Link 4 In
Link1In	B1	Link 5 Out
Link1Out	B4	Link 5 In
Link2In	C2	Link 6 Out
Link2Out	A4	Link 6 In
Link3In	C3	Link 7 Out
Link3Out	C5	Link 7 In
Module 2		
Link0In	B9	Link 8 Out
Link0Out	C8	Link 8 In
Link1In	C9	Link 9 Out
Link1Out	B8	Link 9 In
Link2In	D8	Link 11 Out
Link2Out	A9	Link 10 In
Link3In	A10	Link 10 Out
Link3Out	A8	Link 11 In
P2 Expansion		
Link0Out	(D1)	(Link 3 Out) *
Link0In	(C4)	(Link 3 In)
Link1Out	D10	Link 13 Out
Link1In	B7	Link 13 In
Link2Out	E8	Link 14 Out
Link2In	A7	Link 14 In
Link3Out	E9	Link 15 Out
Link3In	B6	Link 15 In

Table 21 INMOS links connection list

* denotes either/or - see section 2.1.4 Booting

2.8.4 INMOS DITmodules

The INMOS range of DIT (Dual In-line Transputer) modules consists of daughter boards that house extra transputers along with memory or application specific circuitry. They can be used as building blocks in the construction of powerful parallel processing systems. The IMS B011 has sites for two DITmodules:

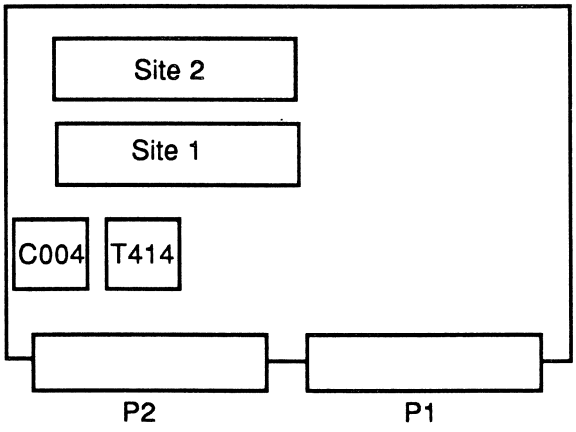


Figure 9 DITmodule sites

The DITmodules are self contained and only draw power from the motherboard. They communicate by four INMOS Links to each site. The pinout of the sites is:

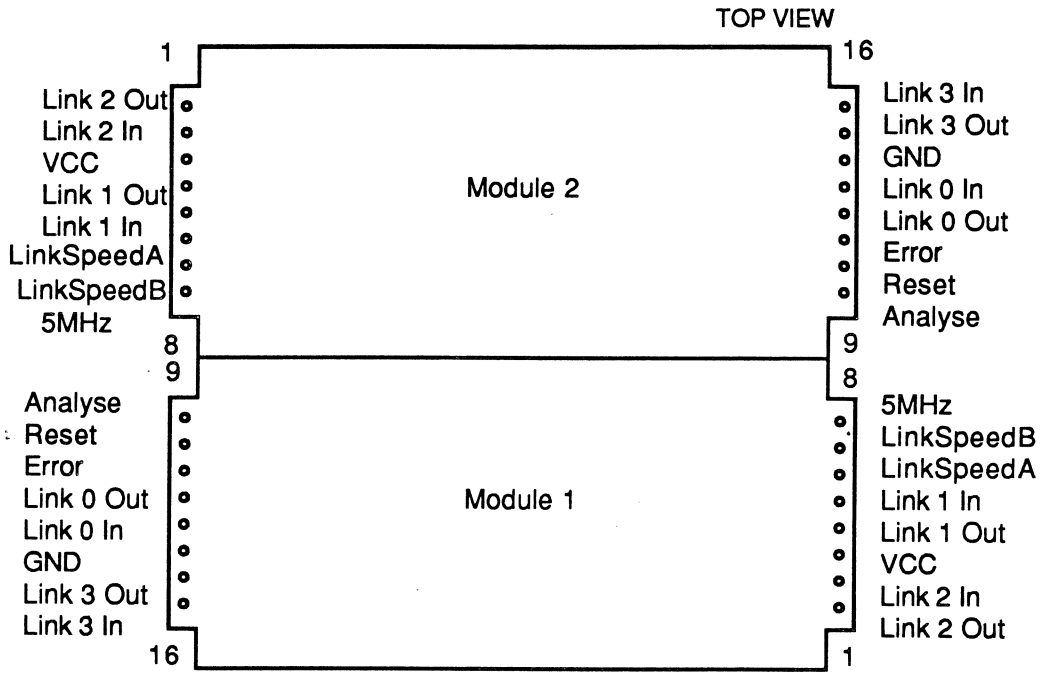


Figure 10 DITModule site pinouts

The LinkSpeedA and LinkSpeedB pins control the speed of the module's links. When LinkSpeedA and LinkSpeedB are both low the links operate at 10Mbits/s. When they are both high the links operate at 20Mbits/s. The link speed is controlled by jumpers LK1, 2, 3 and 4.

Default Jumper and Switch Settings

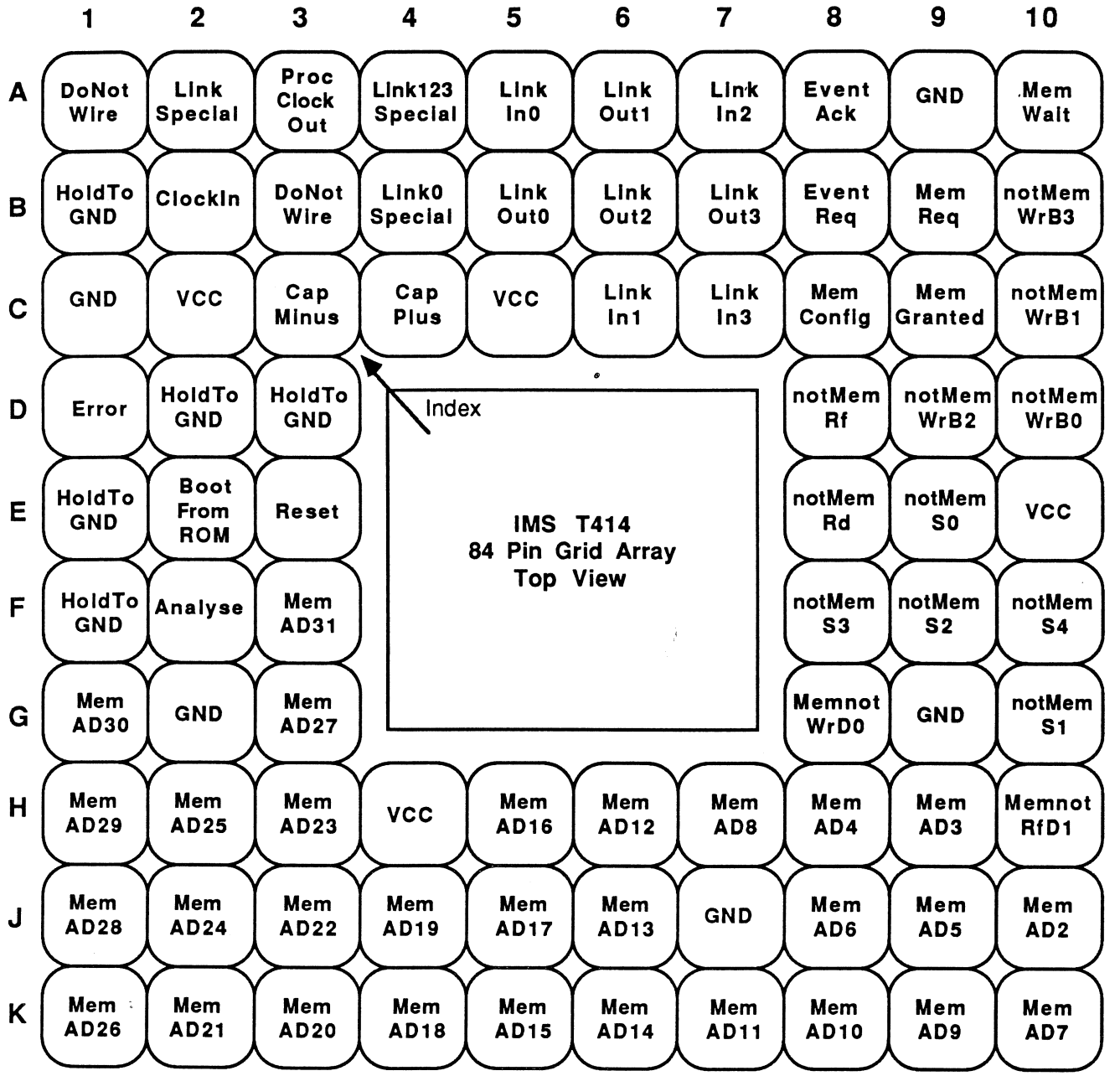
Jumper no	Default position	Comments
LK1	1-2	Mod1 LinkSpeedA (Default = 20Mbits/s)
LK2	1-2	Mod1 LinkSpeedB
LK3	2-3	Mod2 LinkSpeedA
LK4	2-3	Mod2 LinkSpeedB
LK5	See Figure 6	Bus Request level (Default = 3)
LK6	OPEN	Transputer L0 special (See Table 1)
LK7	OPEN	Transputer L123 special
LK8	CLOSED	Reserved for T800 use
LK9	CLOSED	Reserved for T800 use
LK10	CLOSED	Closed = BootFromLink Open = BootFromROM
LK11	CLOSED	T414 Memory Configuration Closed = internal (AD4) Open = external
LK12	1-2	EPROM size, see Table 17
LK13	1-2	"
LK14	OPEN	No VME ints handled (see Table 15)
LK15	OPEN	C004 speed select (Default = 20Mbits/s)
LK16	CLOSED	Parity Enabled (Open = Disabled)
LK17	OPEN	ROR Requester (Closed = RWD)
LK18	See figure 6	Bus grant level 3
LK19	OPEN	NOT system master
LK20	OPEN	Do NOT drive SYSRESET*
LK21	CLOSED	Reserved for T800 use
LK22	CLOSED	Reserved for T800 use
LK23	OPEN	Transputer link special (See Table 1)
LK24	CLOSED	Reserved for T800 use
LK25	1-2	Link Adapter speed (20Mb/s)

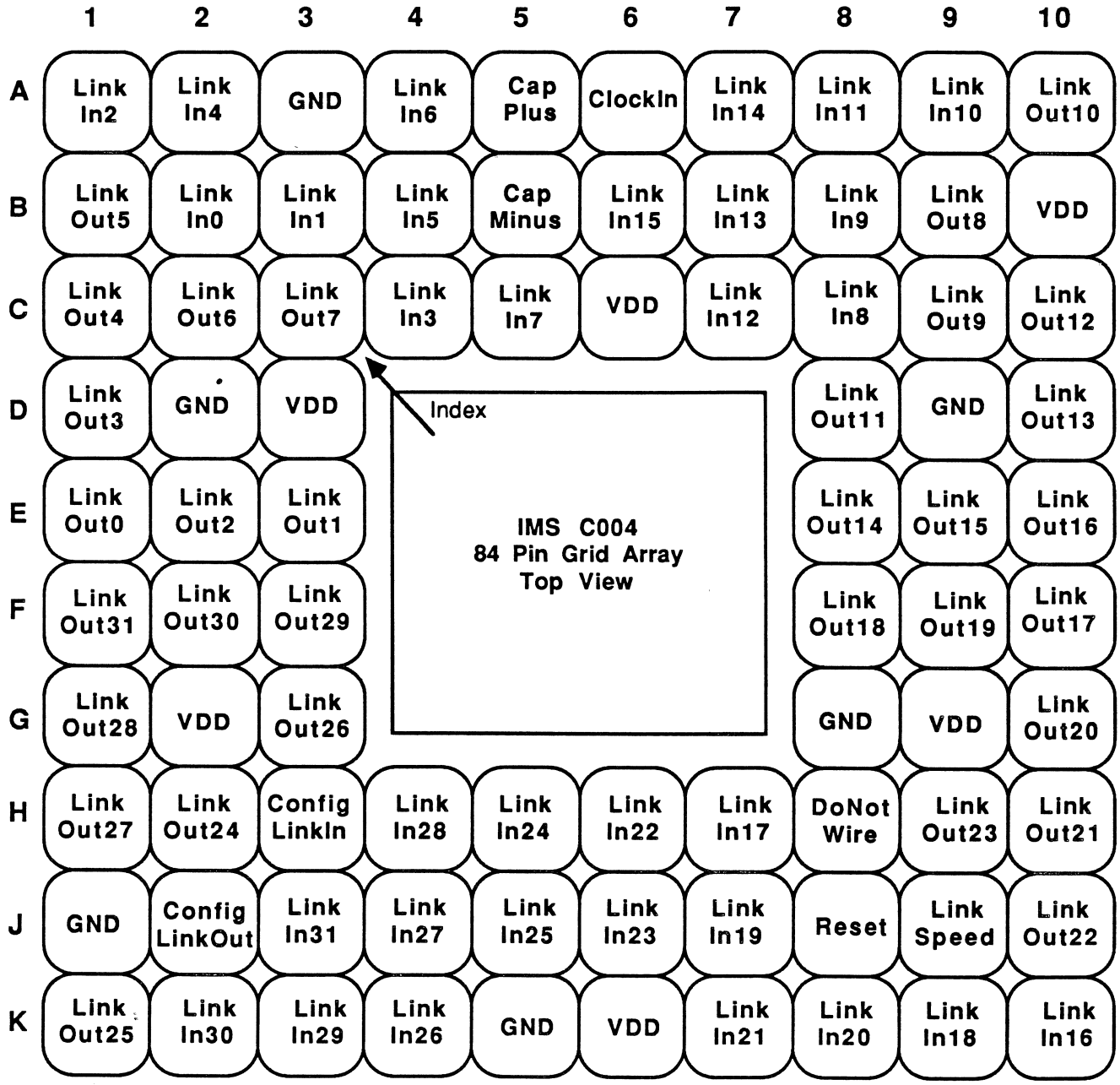
Switch no.	Position	Comment
SW1 1	ON	Slave VME address #A00000
SW1 2	ON	
SW1 3	ON	
SW1 4	ON	
SW2 5	OFF	
SW2 6	ON	
SW2 7	OFF	
SW2 8	OFF	Standard Address Space

Transputer IMS T414 Engineering Data sheet
INMOS document number 42 1078 XX.

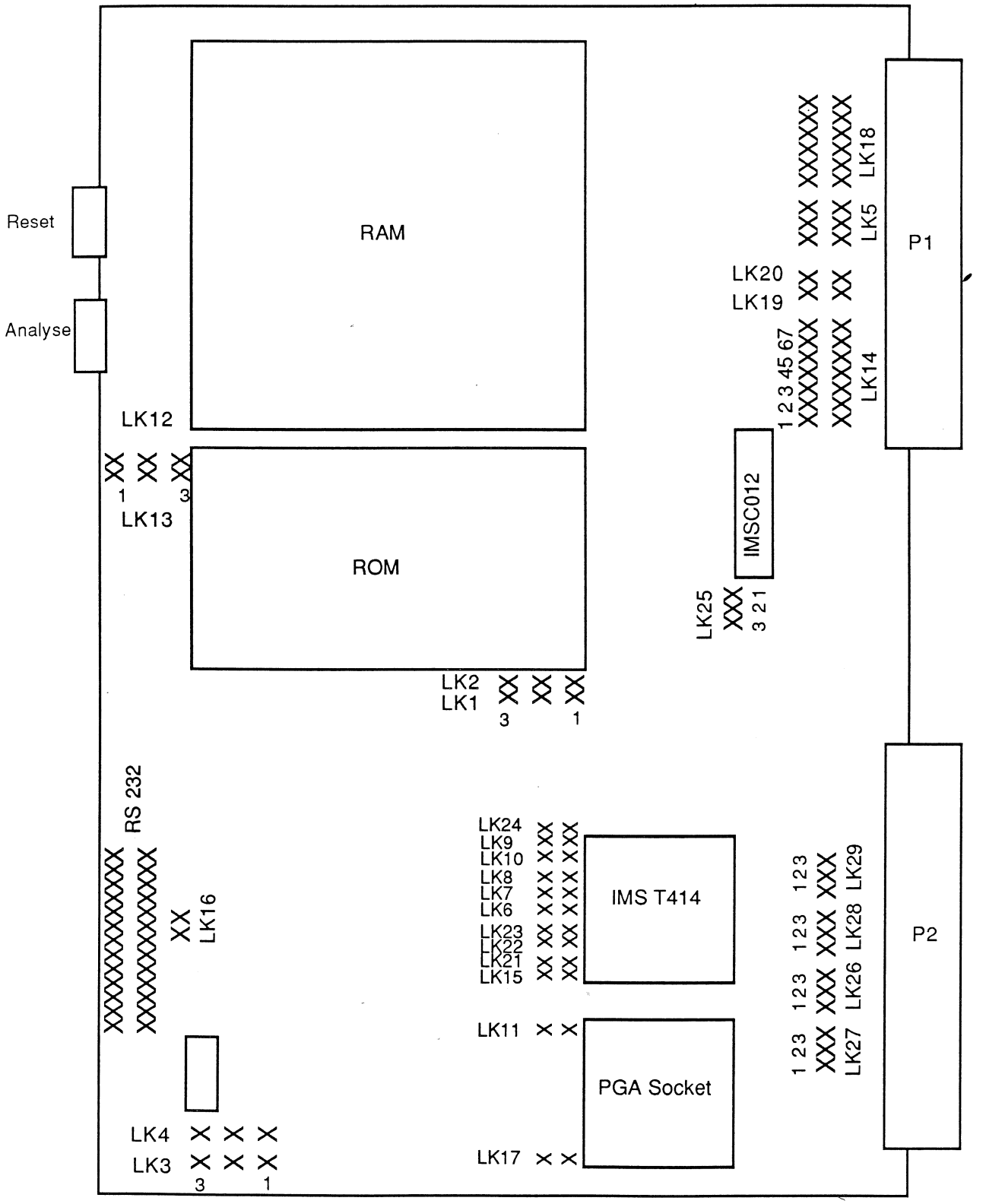
SCN2681 Mullard Dual Asynchronous Receiver/Transmitter SCN2681
Data Sheet - purple binder Tab 12
Mullard August 1983

VME VMEbus Specification Manual Rev C. No SMMAN6000
Signetics 1985

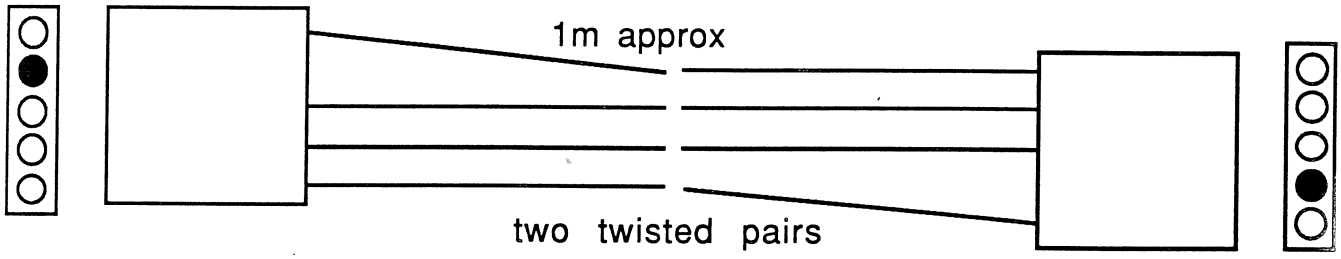

1 2 3 4 5 6 7 8 9 10
A DoNot Wire | Link Special | Proc Clock Out | Link123 Special | Link In0 | Link Out1 | Link In2 | Event Ack | GND | Mem Wait
B HoldTo GND | ClockIn | DoNot Wire | Link0 Special | Link Out0 | Link Out2 | Link Out3 | Event Req | Mem Req | notMem WrB3
C GND | VCC | Cap Minus | Cap Plus | VCC | Link In1 | Link In3 | Mem Config | Mem Granted | notMem WrB1
D Error | HoldTo GND | HoldTo GND | notMem Rf | notMem WrB2 | notMem WrB0
E HoldTo GND | Boot From ROM | Reset | notMem Rd | notMem S0 | VCC
F HoldTo GND | Analyse | Mem AD31 | notMem S3 | notMem S2 | notMem S4
G Mem AD30 | GND | Mem AD27 | Memnot WrD0 | GND | notMem S1
H Mem AD29 | Mem AD25 | Mem AD23 | VCC | Mem AD16 | Mem AD12 | Mem AD8 | Mem AD4 | Mem AD3 | Memnot RfD1
J Mem AD28 | Mem AD24 | Mem AD22 | Mem AD19 | Mem AD17 | Mem AD13 | GND | Mem AD6 | Mem AD5 | Mem AD2
K Mem AD26 | Mem AD21 | Mem AD20 | Mem AD18 | Mem AD15 | Mem AD14 | Mem AD11 | Mem AD10 | Mem AD9 | Mem AD7
Index
IMS T414
84 Pin Grid Array
Top View


1 2 3 4 5 6 7 8 9 10
A Link In2 | Link In4 | GND | Link In6 | Cap Plus | ClockIn | Link In14 | Link In11 | Link In10 | Link Out10
B Link Out5 | Link In0 | Link In1 | Link In5 | Cap Minus | Link In15 | Link In13 | Link In9 | Link Out8 | VDD
C Link Out4 | Link Out6 | Link Out7 | Link In3 | Link In7 | VDD | Link In12 | Link In8 | Link Out9 | Link Out12
D Link Out3 | GND | VDD | Link Out11 | GND | Link Out13
E Link Out0 | Link Out2 | Link Out1 | Link Out14 | Link Out15 | Link Out16
F Link Out31 | Link Out30 | Link Out29 | Link Out18 | Link Out19 | Link Out17
G Link Out28 | VDD | Link Out26 | GND | VDD | Link Out20
H Link Out27 | Link Out24 | Config LinkIn | Link In28 | Link In24 | Link In22 | Link In17 | DoNot Wire | Link Out23 | Link Out21
J GND | Config LinkOut | Link In31 | Link In27 | Link In25 | Link In23 | Link In19 | Reset | Link Speed | Link Out22
K Link Out25 | Link In30 | Link In29 | Link In26 | GND | VDD | Link In21 | Link In20 | Link In18 | Link In16
Index
IMS C004
84 Pin Grid Array
Top View

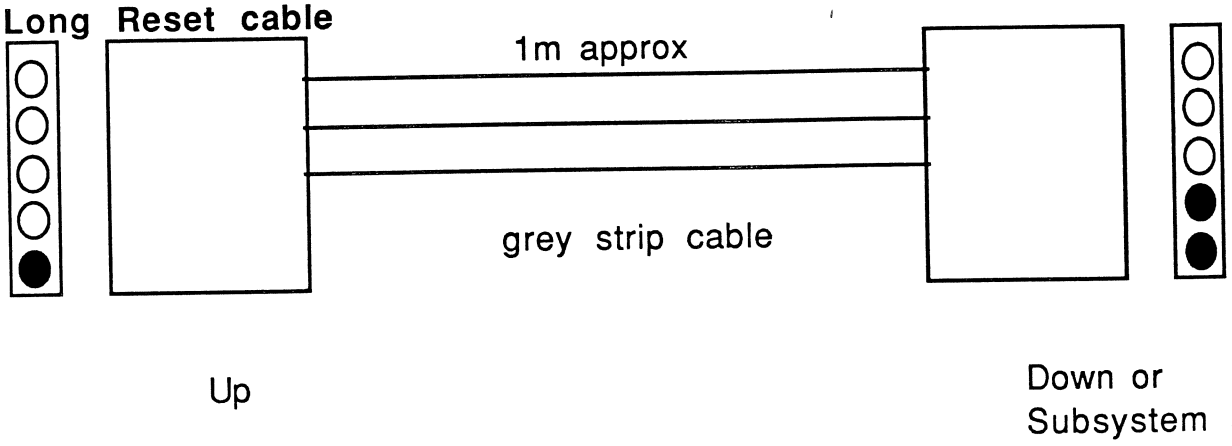
TOP VIEW

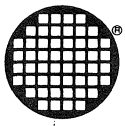

Reset
Analyse
RAM
ROM
LK12
LK13
LK2
LK1
LK25
IMSC012
LK20
LK19
LK18
LK5
LK14
P1
P2
RS 232
LK16
LK24
LK9
LK10
LK8
LK7
LK6
LK23
LK22
LK21
LK15
IMS T414
LK11
PGA Socket
LK17
LK4
LK3
LK29
LK28
LK26
LK27

Long Link cable



Long Reset cable





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