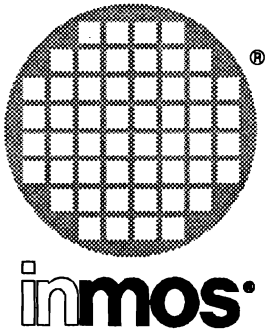

GRAPHICS DATABOOK

Second Edition 1990

INMOS is a member of the SGS-THOMSON Microelectronics Group

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INMOS document number: 72 TRN 204 01

Printed at Redwood Press Limited, Melksham, Wiltshire

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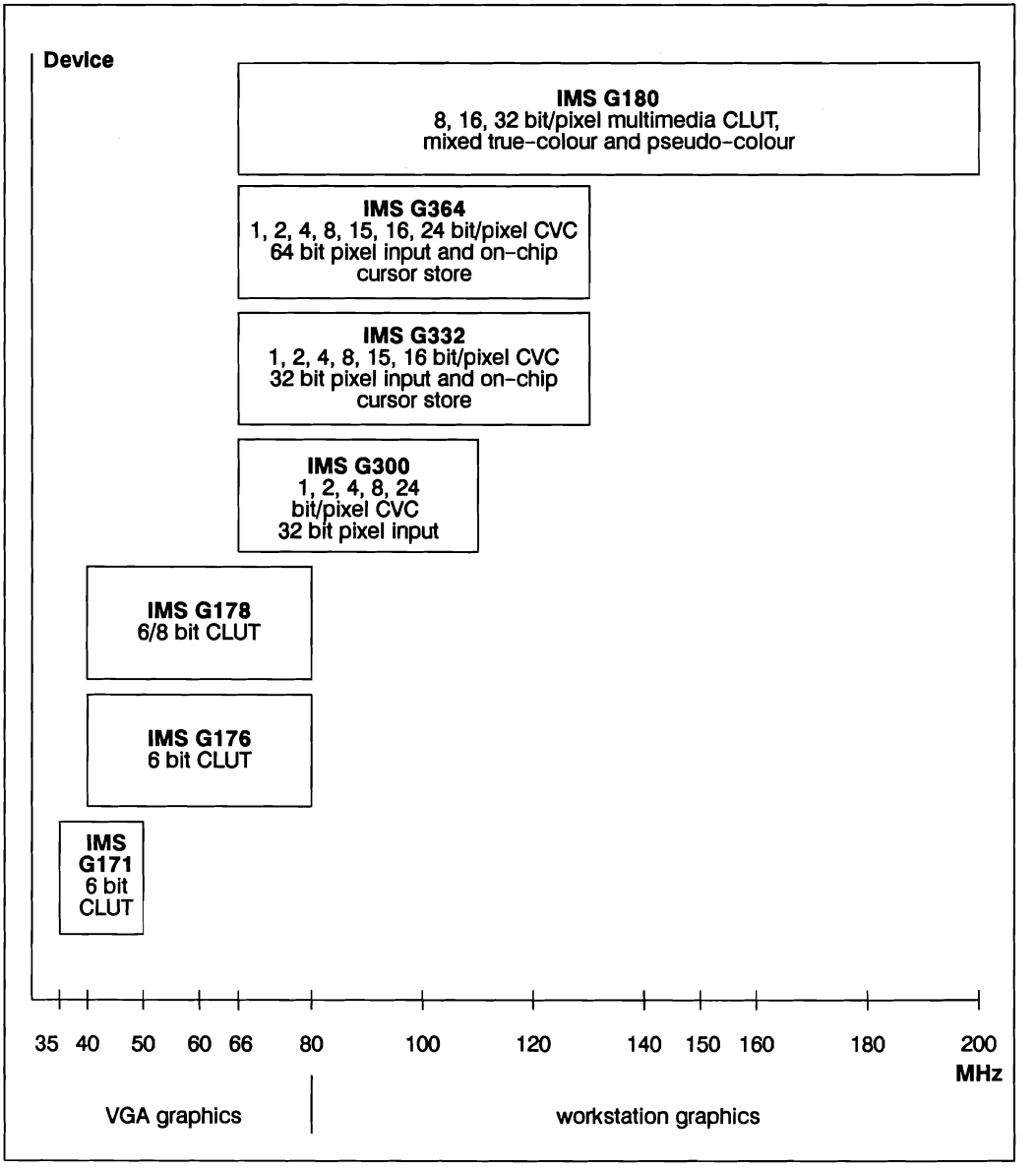
Preface

Graphics processing is a significant area of application for INMOS devices. The INMOS Graphics Databook has been published to provide comprehensive information regarding the current range of INMOS graphics devices.

The databook comprises an INMOS overview, engineering data and applications information for the INMOS IMS G171, G176 and G178 Colour Look-Up Tables (CLUTs), the INMOS IMS G300, G332 and G364 Colour Video Controllers (CVC) and the INMOS G180 high performance CLUT.



Applications of the INMOS graphics family

The INMOS family of colour look-up tables provide the analogue output stages for colour graphic systems. The device consists of a high-speed random access store or look-up table, three DACs, a pixel word mask and a microprocessor interface.

The INMOS family of colour video controllers provide all necessary functions for controlling real time operation of a raster scan video system, using dual ported DRAMs. The devices integrate all video timing and control circuitry, bit map to screen refresh management, colour expansion and gamma correction (via a look-up table) and digital to analogue conversion into a single device. An on-chip phase-locked loop and pixel multiplexer means that all pixel and clock inputs to the CVC are at low frequency TTL levels.

The INMOS IMS G180 CLUT provides the output stages for very high resolution mixed true-colour and pseudo-colour graphics systems. The device combines a versatile pixel multiplexer together with three independent colour channels, each comprising two look-up tables, an overlay table and a high performance video DAC. The device also performs internal clock acceleration so that a TTL clock (at the same rate as pixel data) can be supplied. It can be configured to various pixel formats including a mode to easily mix 24 bit true-colour and 8 bit pseudo-colour images on the same screen (picture in picture).

In addition to graphics devices, the INMOS product range also includes transputer products, digital signal processing devices and fast SRAMs. For further information concerning INMOS products please contact your local SGS-THOMSON sales outlet.

INMOS

1.1 Introduction

The SGS-THOMSON Microelectronics Group is a major supplier of a wide range of semi-conductor devices and commands leading market positions in many product areas. The recent acquisition of INMOS has strengthened SGS-THOMSON's portfolio. INMOS, based in the UK, manufactures microprocessors called transputers, colour graphics devices, digital signal processing devices and very fast SRAMs. Operating in the same way as all divisions of the SGS-THOMSON Microelectronics Group, INMOS services its customers through the corporate SGS-THOMSON sales network.

INMOS is a recognised leader in the design and development of high-performance integrated circuits and is a pioneer in the field of parallel processing. Components are designed and manufactured to satisfy the most demanding of current processing applications and also provide an upgrade path for future applications. Current designs and development will meet the requirements of systems in the next decade. Computing requirements essentially include high-performance, flexibility and simplicity of use. These characteristics are central to the design of all products.

INMOS has a consistent record of innovation over a wide product range and, together with its parent company SGS-THOMSON Microelectronics, supplies components to system manufacturing companies in the United States, Europe, Japan and the Far East. As developers of the transputer, a unique microprocessor concept with a revolutionary architecture and the occam parallel processing language, the standard has been established for the future exploitation of the power of parallel processing.

This databook concentrates on the INMOS graphics product lines, those of VGA compatible Colour Look-Up Tables, Colour Video Controllers and very high performance Colour Look-Up Tables all of which are aimed at colour graphics systems.

In 1985 INMOS launched the first Colour Look-Up Table (CLUT) and soon established a wide customer base. Minimal enhancements resulted in the introduction of the IMS G171 in 1986. This device rapidly became the industry standard and was adopted by IBM for incorporation into the IBM PS/2 range of PCs. The IMS G171 is currently available in a 28 pin DIP package and at speeds up to 50MHz. A high speed version of the IMS G171, designated the IMS G176, was then released in 1987. This device is available in 28 pin DIP and both 32 and 44 pin PLCC at speeds currently up to 66MHz, (but up to 80MHz in Q1 1991). A version of the IMS G171 with higher colour resolution is also available, designated the IMS G178, it has selectable 6- or 8-bit DACs, providing a total colour choice of over 16 million colours. It is available at speeds up to 80MHz and in both 32 and 44 pin PLCC packages.

In 1989 INMOS launched the first Colour Video Controller (CVC), the IMS G300. This device found immediate success and has been designed into many different systems. The IMS G332 and IMS G364, launched in 1990, build on the success of the IMS G300 architecture and were designed in response to customer requests following much consultation. The CVC integrate all video timing and control circuitry, bit map to screen refresh management, a colour expansion and gamma correction look-up table and digital to analogue conversion into a single chip.

In addition to extending the CLUT and CVC ranges INMOS has also diversified into very high performance CLUTs with the IMS G180. The IMS G180 is a combined true-colour and pseudo colour look-up table intended for high resolution true-colour systems. Integrating all three colour channels, multilplexed pixel ports and a phase-locked loop, the device requires no high frequency inputs.

The SGS-THOMSON Microelectronics Group is constantly upgrading, improving and developing its product range and is committed to maintaining a global position of innovation and leadership.

1.2 Production

INMOS products are currently manufactured at Newport (UK) with additional facilities available at Carrollton (USA).

Advanced manufacturing equipment is used in these facilities to produce high performance devices, some consisting of up to one million transistors. Wafer steppers, plasma etchers and ion implanters form the basis of fabrication.

1.3 Quality and reliability

A description of the SGS-THOMSON Microelectronics approach to Quality and Reliability is included later in this databook. The subject is comprehensively detailed in the SGS-THOMSON Microelectronics Quality and Reliability publication SURE 5. This program is applied totally to INMOS products.

1.4 Future developments

1.4.1 Research and development

The SGS-THOMSON Miroelectronics Group has achieved technical success based on a position of leadership in products and process technology in conjunction with substantial R&D investment, which in 1989 represented 19% of sales, well above the estimated worldwide average of 15% for the top ten semi-conductor manufacturers.

1.4.2 Process developments

New process technologies are continuing to be developed for next generation products. Work is now taking place to scale down current technologies while new sub-micron CMOS technologies are being brought into production.

Graphics overview

2.1 The advancing graphics market

Recent years have seen graphics systems playing an increasingly important role in computer technology. The potential for future growth is expanding as the power of computer graphics hardware increases. Business systems, Graphics Design, Animation, Desktop publishing, CAD/CAM Workstations and Medical Imaging are just some of the application areas. The benefits offered to so many systems are likely to ensure continued and increasing demand for graphics and graphical interfaces for many years to come. Better communication of information, better user productivity and the introduction of computer systems to a wider non-technical audience are just some of the reasons behind the increasing importance of computer graphics. The growing volumes for graphics-based systems and the advances in silicon technology have both contributed to reducing costs of such systems and thus fuelling further increases in performance.

The trend towards higher resolutions, more colours and faster screen updates has spawned improved technology in computer graphics hardware. The need for high data rates in graphics systems was a major push in the development of fast DRAMs for example. Fast access modes such as page and nibble mode were the first steps in the quest to increase bandwidth, and now dual port video DRAM's with their on-chip serial shift registers are the most popular component for building high speed frame buffers.

One other significant component which has helped to enhance the performance of todays graphics systems is the colour palette or Colour Look-Up Table (CLUT). This is the device which converts the high-speed digital pixel data into the analogue signals required to drive an analogue colour monitor.

2.2 CLUTs and colour representation

With the developments in the performance of graphics systems has come the requirement to display many more colours on the screen. Increased resolutions demand a wider total range of colours, thus giving the subtle degrees of shading that the resolution makes possible. The bit-mapped method of storing a raster-scan image means that the more information about any pixel that has to be stored (e.g. its colour and intensity) the more memory it requires in the frame buffer. In a true-colour system, a single bit per pixel obviously gives a black and white display - each pixel is either on or off. Three bits per pixel (one for each colour gun) gives only eight crude colours, totally inadequate for serious graphics work. Increase this to say 8 bits per gun (24 bits per pixel) and you have a total colour range of over 16 million, which is more appropriate for the fine shading required by the solids modelling and CAD/CAE applications of today.

However, there is a price to pay. If a reasonable range of colours is provided, the overall memory requirement soon becomes prohibitively large, as does the processing power required to manipulate this data. For example, if each pixel in a 1K x 1K display used 8 bits to describe the intensity of each colour gun the overall memory requirement would be 3Mbytes. The main problem with this would be the cost, but it would also be difficult for a drawing processor to manipulate this amount of data quickly enough to avoid annoying delays whilst the screen is being updated.

The colour look-up table, or pseudo-colour approach is to store a much smaller amount of data for each pixel, and to use this data to reference a location in a colour table. The table which contains the colour definitions then provides a larger amount of data to describe the particular colour required. The colour definitions stored in the table can be changed by the host processor according to the particular application. Typical CLUTs can accomadate up to 256 colours in a table or 'palette' at any one time, with each entry in the table being perhaps 18 or 24 bits wide. An 18 bit wide colour value (6 bits for each for red, green and blue) provides a choice from a total range of 264,144 colours, whilst a 24 bit colour value increases the choice to over 16 million shades.

The key factor in the colour look-up table solution is the availability of an enormous range of possible colours, but the acceptance that for a particular application, only a smaller sub-set of those colours will ever need to be displayed on the screen at any given time. Someone developing a flight simulator program may desire a large number of earth tones, predominantly greens and browns, with which to render his land-

scape; a solid modelling application may require various shades of one colour to give objects the illusion of depth, shape or illumination; a portrait library forming part of a security database may require only skin tones to portray human faces. The aesthetics and ergonomics of colour selection are also well catered for by the Colour Look-Up Table solution. Choosing a range of colours which are both pleasing and safe to look at for long periods can be important for, say, PCB layout where the designer may spend many hours looking at hundreds of fine lines packed closely together.

2.2.1 Where does a CLUT fit into a graphics system ?

Modern bit-mapped graphic displays work by building up a complete image from a two-dimensional array of picture elements or *pixels*. Each picture element defines the colour of its respective point on the screen. The number of pixels across one line and down one column of the image defines the *screen resolution* of the system.

Generally the image is stored pixel-by-pixel in a *frame store* built from RAM. For every pixel a code is stored to represent the colour of that pixel (in the case of a monochrome system this will be just a representation of the intensity). If a colour graphics system allocates n bits of data for each pixel then clearly each pixel can be displayed as one of 2^n colours. 8-bit pixels, for example, allow 256 possible colours, 24-bit pixels allow approximately 16 million colours.

In a VGA system the task of turning digital pixels into analogue red, green and blue signals to feed to a colour monitor is the function performed by a Colour Look-Up Table or *CLUT*.

CLUTs use the digital pixel as an address into a table of *colour values*. For an eight bit pixel there will be 256 entries in this table, one for each colour. Each entry in the colour table is divided into three components, one each for the red, green and blue intensity components of that colour. In the case of the IMS G171 and G176 each intensity value is a 6 bit number and so the total colour value contains 18 bits.

Whilst the number of locations in the colour table determines the number of available colours on the screen at any one time, it is the size of each entry in the colour table which determines the total number of colours from which the choice can be made. If there are 18 bits in each colour value, then the colour value may be chosen from 2^{18} or 256K possible colours. However since there are only 256 locations in the colour table only 256 of these are available for display at any given time. The choice is therefore 256 from 256K colours.

Once a colour value has been fetched from the location addressed by the pixel address it is split into its three components and fed to three DACs to convert the red, green and blue values to analogue form. The analogue signals generated by the DACs are then driven out of the CLUT to the monitor. It is the resolution of the DAC which determines the *colour resolution* of the system. The 6-bit DACs in the G171 for example allow 2^6 or 64 different intensity levels for each of the red, green and blue components of a pixel. 4-bit DACs would allow 16 levels and 8-bit DACs would allow 256 levels.

2.3 The INMOS CLUT history

By drawing on its previous experience with high-speed memory devices, INMOS introduced its first CLUT in 1985. The first example, the IMS G170, provided a palette of 256 colours, from a total range of over 256K colours. Additional features such as the implementation of composite sync on the outputs, a pixel mask register and compatibility with industry video signal standards made it an instant success, offering a cheaper yet better performance option to many of the existing hybrid solutions. The current INMOS family of CLUTs provides a range of speed, functionality and cost. Further members of the family are under development.

The success of these parts can be judged by their rapid uptake by many of the industry's biggest colour graphics users, the greatest testament being their use by IBM in the range of PS/2 machines for their VGA graphics systems.

2.3.1 The INMOS VGA compatible CLUT range

The INMOS family of VGA compatible CLUT products currently extends to 4 members with further products under development. Those available now offer a range of different functionality, packaging and maximum pixel rates as summarised below:

Part Number	Pixel Rates	DAC Resolution	Package
IMS G171	35, 50	6 bits	28 pin DIP
IMS G176	40, 50, 66, 80	6 bits	28 pin DIP, 32 pin PLCC, 44 pin PLCC
IMS G176L	50	6 bits	28 pin DIP, 32 pin PLCC, 44 pin PLCC
IMS G178	40, 50, 66, 80	6/8 bits	32 pin PLCC, 44 pin PLCC

The IMS G171 is the device used by IBM in all PS/2 machines, so is fully VGA compatible.

The IMS G176 is upwardly compatible with the IMS G171 and is therefore ideal for use in PS/2 VGA compatible systems.

The IMS G176L is a power-down version of the IMS G176 and has been designed to have a guaranteed standby power supply current of less than 10mA. It is ideal for battery powered machines such as lap-top and note-book Computers.

The IMS G178 is upwardly compatible with the IMS G176, and adds the option of 8 bit video DACs as well as the ability to generate composite video signals. It is ideal for advanced VGA graphics systems.

2.3.2 Choosing your device – functionality

For most medium-high resolution colour displays it is accepted that 6-bit DAC resolution is sufficient. This gives a total colour choice of 262,144 colours which can be programmed into the CLUT. For very high resolution applications such as CAD/CAE workstations where 3-D solid modelling requires ultra-smooth shading, INMOS provides the IMS G178. This has 8-bit DAC resolution, giving a total colour choice of over 16 million colours, but can also be switched back to offer compatibility with 6-bit DAC application software. The range of colour video controllers and the IMS G180 all have an 8-bit DAC resolution.

The provision of horizontal and vertical synchronization signals to a monitor are required to indicate the end of a line or frame of display information. These sync signals can be provided on a separate wire to the monitor or superimposed onto the analogue video signals to give Composite Video (see Glossary of Terms.) The choice of method is largely dependent on the type of monitor used. Some are switchable to operate on either scheme. This superimposition of video and sync signals can be performed internally on the IMS G170 or G178 devices.

On parts with read-back the contents of the colour table may be read as well as written, i.e. the microprocessor interface is bi-directional. This is used mainly for self-testing purposes, and also avoids any need to keep a shadow copy of the colour table when one application is 'switched out' to make way for another application requiring a different colour selection. The IMS G171, G176 and G178 all provide this facility.

2.3.3 Choosing your CLUT– speed selection

A first-pass calculation for the pixel data rate required can be obtained by multiplying:

$$\text{Horizontal Resolution} \times \text{Vertical Resolution} \times \text{Frame Refresh Rate}$$

$$H_{RES} \times V_{RES} \times F_{RSH}$$

eg. $480 \times 320 \times 60\text{Hz} = 18.5\text{MHz}$

However, as the desired resolution increases the amount of time which the monitor spends in horizontal and vertical blanking (while the electron beam retraces to the start of the line or frame) becomes significant. Since this reduces the actual time available for pixel refreshing, the pixel data rate must increase accordingly. These blanking parameters are a function of the particular monitor used. To display higher resolution images a better quality monitor is required which has shorter retrace times.

If Horizontal Blanking Time = H_{BLK}

Vertical Blanking Time = V_{BLK}

Time taken per second in blanking:

$$T_{BLK} = (V_{RES} \times F_{RSH} \times H_{BLK}) + (F_{RSH} \times V_{BLK})$$

So time remaining for pixel refreshing:

$$T_{RFH} = 1 - T_{BLK}$$

Pixels to be refreshed per second:

$$P_{RFH} = V_{RES} \times H_{RES} \times F_{RSH}$$

Therefore the pixel data rate required:

$$= \frac{P_{RFH}}{T_{RFH}} = \frac{V_{RES} \times H_{RES} \times H_{RSH}}{1 - F_{RSH}[(V_{RES} \times H_{BLK}) + V_{BLK}]}$$

In this way the actual maximum pixel data rate required for the particular application and monitor used can be calculated, and the appropriate device selected.

2.3.4 Colour Video Controllers

Historically, high-performance graphics systems were often implemented using graphics specific processors as the drawing engines which provide CRT control signals, perform bit-map operations and take some of the more computationally intensive tasks away from the host processor by the implementation of a set of hard-wired primatives. However, there is a danger with casting drawing algorithms in silicon. With graphics algorithms continually changing, any drawing primative that is hard-wired into the silicon becomes expensive and time-consuming to replace. As the host processor is isolated from the graphics bus, there is also the danger that the host processor may become restricted by the often inferior capacity of the drawing engine to connect to the bit-map. The trend now therefore is for drawing algorithms to remain in software, running on a general-purpose processor, or if performance dictates - several processors.

The new Colour Video Controller (CVC) range from INMOS supports this system architecture by providing all of the necessary functions for controlling real time operations of a graphics system. The facilities provided are designed to isolate the host processor from the constraints of the real time system without in any way interfering with the ability of the processor to specify and manipulate screen data and leads the way into flexible and truly upgradable graphics systems.

The Colour Video Controller can interface to any standard processor and to any monitor. The device integrates an 8-bit CLUT, a fully programmable video timing generator (VTG), a phase-locked loop (PLL) and an intelligent memory interface to support video DRAMs, all on a single device. It offers a solution to the real-time problems of bit-mapped graphics systems and interfaces to the host processor, frame store and monitor with the minimum of external circuitry.

The support of dual-ported Video DRAMs is essential for high performance systems to allow the maximum drawing band width between processor and bitmap. The CVC handles all the bitmap to screen operations, including screen refresh, address generation (interlaced or non-interlaced) video synchronisation and colour conversion. Whilst many video controllers have claimed to support Video DRAMs effectively, the INMOS Colour Video Controller is the first to allow seamless mid-line updates of the screen, thus allowing the bit-map to be configured to any shape of display. Screen sizes are no longer restricted to multiples of the serial shift register length, so wastage of the bit-map is eliminated.

Multisync monitors available now address the problem of interfacing to a variety of systems with different CRT timing signal outputs, yet this could be seen as addressing the problem from the wrong direction. Expensive multisync monitors are partly a solution to the limitations of the graphics controller device which provides only fixed or limited programmability of their timing signals. The Colour Video Controller on the

other hand, approaches the problem from the other direction by providing a fully programmable video timing generator, allowing the analogue outputs to be configured to support any monitor or a selection of studio television standards – all within software. Thus by simply reprogramming the VTG registers in the CVC, a graphics board can be designed which has the ability to drive a range of colour displays.

It is important, when considering a video data conversion system, to chose a monolithic approach. Having all three DACs and the video timing generator on the same chip greatly reduces the problems usually encountered with separate chip solutions such as those associated with matching DAC linearity and pixel timing on the screen.

The CVC performs pixel data multiplexing and on-chip clock multiplication by the use of a phase-locked loop, so that there are no video rate digital signals or clocks external to the chip. This minimises the need for high-speed digital design, all external components can be low-cost CMOS or TTL; radiated emissions are kept low, giving easy compliance with Federal Communications Commisions regulations, and design times and production costs are held to a minimum.

The other advanced features supported by each member of the CVC range is summarised below.

- The IMS G300 CVC supports 1, 2, 4 and 8 bit pseudo colour pixels as well as providing a gamma corrected 24-bit per pixel full-colour mode.
- The IMS G332 CVC supports 1, 2, 4 and 8 bit pseudo colour pixels as well as providing gamma corrected 15- and 16-bit true-colour pixels. It also provides an on-chip cursor store and is able to support interleaved banks of Video DRAMs.
- The IMS G364 CVC supports 1, 2, 4 and 8 bit pseudo colour pixels as well as providing gamma corrected 15- and 16-bit true-colour pixels and gamma corrected 24-bit full-colour pixels. It also provides an on-chip cursor store and is able to support interleaved Video DRAMs. This device has a 64-bit pixel bus and is particularly suitable for Intel i860 based systems.

The Colour Video Controller family is a further example of INMOS' successful and innovative approach to chip design and demonstrates INMOS' commitment to remain the dominant force in the growing graphics market place.

2.3.5 High-Performance CLUTs

It is clear from the developments at the leading edge of graphics systems research that the graphics market will continue to demand higher pixel and colour resolutions, more functional integration, and faster speeds, and yet all at suitably competitive prices.

The IMS G180 Combined True Colour and Pseudo Colour Look-Up Table is designed to meet these requirements and to provide the high-end system designer with a large amount of integrated functionality, whilst leaving enormous flexibility for the designer to tailor the system for his particular application. The IMS G180 provides a single chip solution for any high resolution true-colour application such as true-colour workstations, multimedia graphics systems, interactive real-time video and graphics and digital video editing and manipulation.

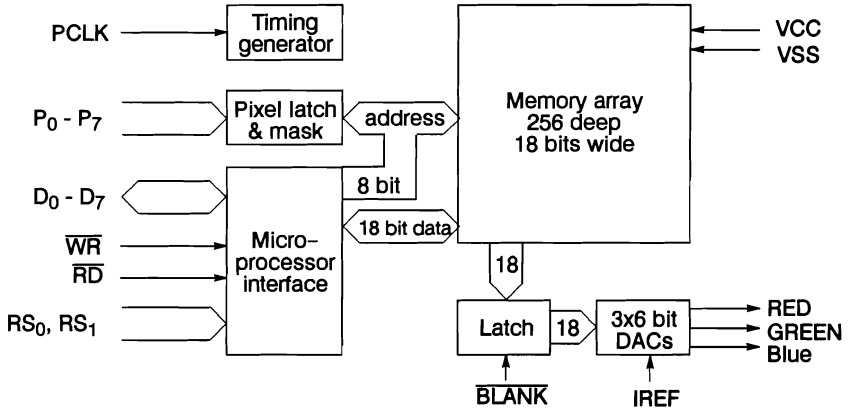
The device integrates all three colour channels as well as a programmable pixel multiplexer and a phase-locked loop. Each of the three colour channels is independent and contains a pseudo-colour look-up table for colour expansion, a gamma correcting table, an overlay look-up table and a high-speed video DAC. The provision of pixel multiplexing and matching clock multiplication provides a solution where all inputs to the CLUT are at low-frequency TTL levels.

The device can be configured to work with a range of pixel sizes: 8-bit pseudo colour, 16-bit true colour or 32-bit mixed pixel (24-bits full-colour and 8-bits pseudo colour). True colour and pseudo colour images can easily be switched between independent ports on a pixel by pixel basis, where various compositing modes are supported to select the desired pixel.

All these features make the IMS G180 an ideal component for the next generation of high performance colour graphics systems, and shows INMOS' ongoing commitment to this sector. With this and other devices under development INMOS intends to maintain its reputation as an innovative and quality supplier of VLSI devices.

IMS G171
High performance CMOS colour look-up table

Designed to be compatible with IBM PS/2, VGA graphics systems



FEATURES

- Compatible with the RS170 video standard
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun, composite blank.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V±10% power supply.
- Low power dissipation, 880mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL package.

DESCRIPTION

The IMS G171 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters (designed to drive into a doubly terminated 75Ω line) and bi-directional microprocessor interface into a single 28 pin package.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G171 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

3.1 Pin designations

3.1.1 Pixel interface

Signal	Pin	I/O	Signal name	Description
PCLK	13	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
$P_0 - P_7$	5–12	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the colour look-up table.
$\overline{BLANK}$	16	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.

3.1.2 Analogue interface

Signal	Pin	I/O	Signal name	Description
RED GREEN BLUE	1 2 3	0 0 0		These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. The number of current sources active is controlled by the 6 bit binary value applied to each DAC.
IREF	4	I	Reference current	The reference current drawn from VCC via the IREF pin determines the current sourced by each of the current sources in the DACs.

3.1.3 Microprocessor Interface

Signal	Pin	I/O	Signal name	Description
$\overline{WR}$	25	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	15	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	26,27	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
$D_0 - D_7$	17-24	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G171 under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register selected and will go to a high impedance state.

3.1.4 Power supply

Signal	Pin	Signal name	Description
VCC	28	Power supply	Digital and analogue supply pads are bonded out to a single pin. The package contains a high-frequency decoupling capacitor between VCC and VSS to ensure a high quality analogue supply.
VSS	14	Ground	

3.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
				There is a single Address register within the IMS G171. This register can be accessed through either register select 0,0 or register select 1,1
0	0	8	Address (write mode)	Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to register 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the colour look-up table addressed and then increments the Address register. A read from register 0,0 is identical to a read from 1,1.
0	1	18	Colour Value	The Colour Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits (D_0–D_5) are used. When a byte is read only the least significant six bits contain information – the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up table specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operation of the IMS G171 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P_0–P_7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed, via that interface.

3.2 Device description

The IMS G171 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 × 18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18 bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G171. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation and flashing objects. The pixel mask register is directly in the pixel stream, thus operations on the contents of the mask register should be synchronised to the pixel stream.

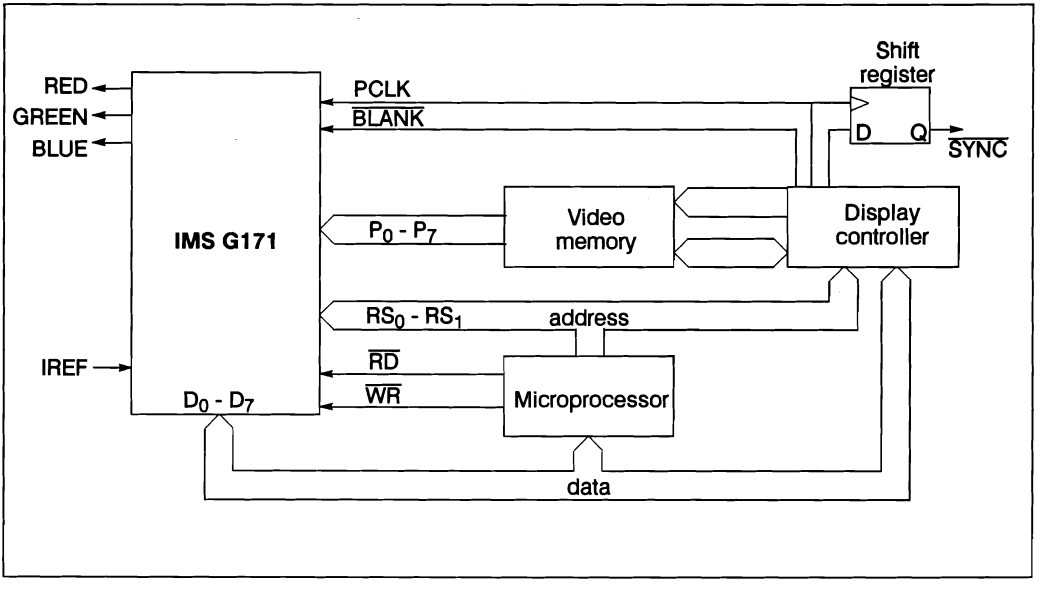


Figure 3.1 Typical IMS G171 application

3.2.1 Video path

Pixel address and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analogue outputs after three further rising edges of Pixel Clock (see figure 3.2).

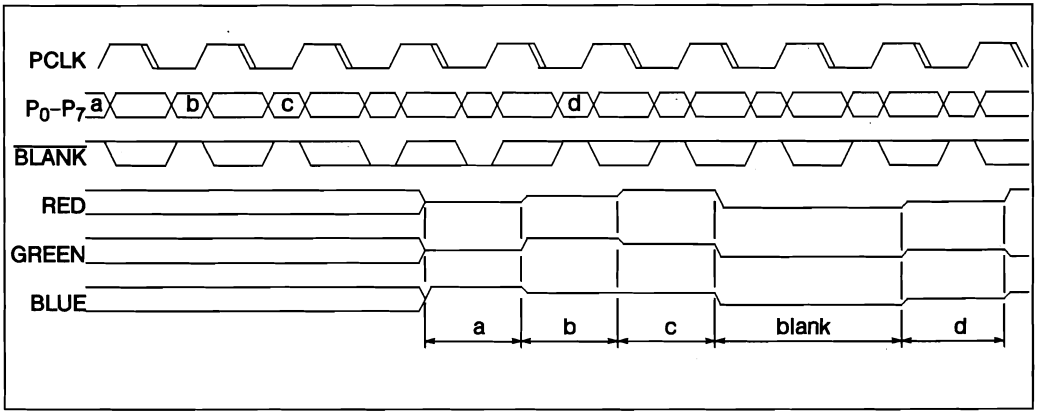


Figure 3.2

3.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 9.07 mA when driving a doubly terminated 75Ω load . This corresponds to an effective DAC output loading $R_{EFFECTIVE}$ of 37.5Ω.

The $\overline{BLANK}$ input to the IMS G171 acts on all three of the analogue outputs. When the $\overline{BLANK}$ input is low a binary zero is applied to the inputs of the DACs. The expression for calculating IREF with various peak white voltage/output loading combinations is given below:

$$IREF = \frac{V_{PEAKWHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note that for all values of IREF and output loading:

$$V_{BLACKLEVEL} = 0$$

3.2.3 Microprocessor Interface

Below are listed the three microprocessor interface registers within the IMS G171 and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address registers.

3.2.4 Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

3.2.5 Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

3.2.6 Asynchronous look-up table access

Accesses to the Address and Colour Value registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G171. Internal logic synchronizes data transfers, between the look-up table and the Colour Value register, to the Pixel Clock in the period between the microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers to take place.

3.2.7 The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is independent of the Address and Colour Value registers. Operations on the Pixel Mask register are required to be synchronous to the pixel stream. The requirements for Pixel Mask register synchronisation are described in section 3.4.8.

3.3 Electrical specifications

3.3.1 Absolute maximum ratings*

Symbol	Parameter	Min.	Max.	Units	Notes
VCC	DC supply voltage		7.0	volts	
	Voltage on input and output pins	−1.0	VCC + 0.5	volts	
TS	Storage temperature	−55	125	°C	
TA	Ambient temperature under bias	−40	85	°C	
PDmax	Power dissipation		1	W	
	Reference current	−15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VCC	Positive supply voltage	4.5	5.0	5.5	volts	2
VSS	Ground		0		volts	
VIH	Input logic '1' voltage	2.0		VCC+0.5	volts	
VIL	Input logic '0' voltage	−0.5		0.8	volts	3
TA	Ambient operating temperature	0		70	°C	4
IREF	Reference current	−7.0		−10	mA	5

Notes

1 All voltages are with respect to VSS unless otherwise specified.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (tCHCH) or 10ns, whichever is the smaller value.

4 With a 400 linear ft/min transverse air flow.

5 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
ICC	Average power supply current		160	mA	4, IMS G171-50
ICC	Average power supply current		150	mA	4, IMS G171-35
VREF	Voltage at IREF input (pin 4)	VCC−3	VCC	volts	
IIN	Digital input current (any input)		±10	μA	5,6
IOZ	Off state digital output current		±50	μA	5,7
VOH	Output logic '1'	2.4		volts	IO = −5mA
VOL	Output logic '0'		0.4	volts	IO = 5mA

Notes

1 All voltages are with respect to VSS unless otherwise specified.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). ICC is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 VCC = max, VSS $\leq$ VIN $\leq$ VCC.

6 On digital inputs, pins 5-13, 15, 16, 25-27.

7 On digital input/output, pins 17-24.

3.3.3 DAC characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
	Resolution	6		bits	
VO(max)	Output voltage		1.5	volts	IO≤10mA
IO(max)	Output current		−21	mA	VO≤1V
	Full scale error		±5	%	4
	DAC to DAC correlation error		±2	%	5
	Integral linearity error		±0.5	LSB	6
	Rise time (10% to 90%)		8	ns	7
	Full scale settling time		20	ns	7,8,9, IMS G171-50
	Full scale settling time		28	ns	7,8,9, IMS G171-35
	Glitch energy		200	pVsec	7,9

Notes

1 All voltages are with respect to VSS unless otherwise specified.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = −9.07mA.

4 Full scale error from the value predicted by the design equations.

5 About the mid point of the distribution of the three DACs measured at full scale deflection.

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

7 Load = 37.5Ω + 30pF with IREF = −9.07mA.

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

3.3.4 AC test conditions

Input pulse levels	VSS to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure 3.3

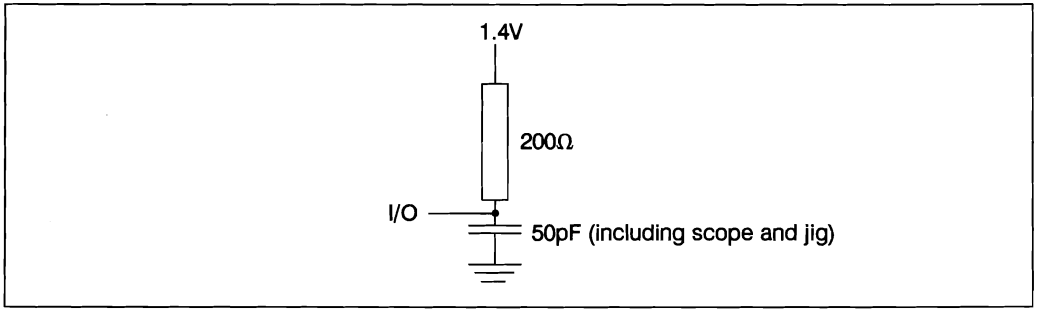


Figure 3.3 Digital output load

3.3.5 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable D_0–D_7

4 BLANK $\leq$ VIL(max) to disable RED, GREEN and BLUE.

3.3.6 Video operation (figure 3.4)

Symbol	Parameter	All Max.	35MHz Min.	50 MHz Min.	Units	Notes
tCHCH	PCLK period	10000	28	20	ns	
ΔtCHCH	PCLK jitter	±2.5			%	1
tCLCH	PCLK width low	10000	9	6	ns	
tCHCL	PCLK width high	10000	7	6	ns	
tPVCH	Pixel address set-up time		5	4	ns	2
tCHPX	Pixel address hold time		5	4	ns	2
tBVCH	$\overline{BLANK}$ setup time		5	4	ns	
tCHBX	$\overline{BLANK}$ hold time		5	4	ns	
tCHAV	PCLK to valid DAC output	30	5	5	ns	3
ΔtCHAV	Differential output delay	2			ns	4
	Pixel clock transition time	50			ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

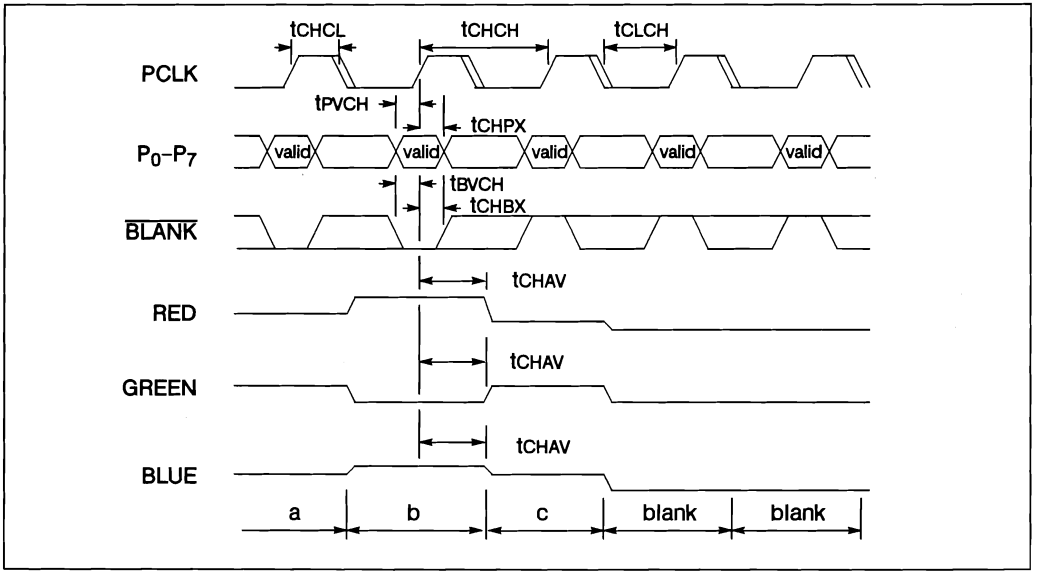


Figure 3.4 Video operation

3.3.7 Microprocessor Interface operation (figures 3.5)

Symbol	Parameter	All Max.	35MHz Min.	50 MHz Min.	Units	Notes
tWLWH	$\overline{WR}$ pulse width low		50	50	ns	
tRLRH	$\overline{RD}$ pulse width low		50	50	ns	
tSVWL	Register select setup time		15	10	ns	
tSVRL	Register select setup time		15	10	ns	
tWLSX	Register select hold time		15	10	ns	
tRLSX	Register select hold time		15	10	ns	
tDVWH	Write data setup time		15	10	ns	
tWHDX	Write data hold time		15	10	ns	
tRLQX	Output turn-on delay		5	5	ns	
tRLQV	Read enable access time	40			ns	
tRHQX	Output hold time		5	5	ns	
tRHQZ	Output turn-off delay	20			ns	1
tWHWL1	Successive write interval		τ1	τ1	ns	3
tWHRL1	Write followed by read interval		τ1	τ1	ns	3
tRHRL1	Successive read interval		τ1	τ1	ns	3
tRHWL1	Read followed by write interval		τ1	τ1	ns	3
tWHWL2	Write after colour write		τ1	τ1	ns	2,3
tWHRL2	Read after colour write		τ1	τ1	ns	2,3
tRHRL2	Read after colour read		τ2	τ2	ns	2,3
tRHWL2	Write after colour read		τ2	τ2	ns	2,3
tWHRL3	Read after read access write		τ2	τ2	ns	2,3
	Write/Read enable transition time	50			ns	

Notes

1 Measured $\pm$200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 $\tau 1 = (3 \times tCHCH)$, $\tau 2 = (6 \times tCHCH)$

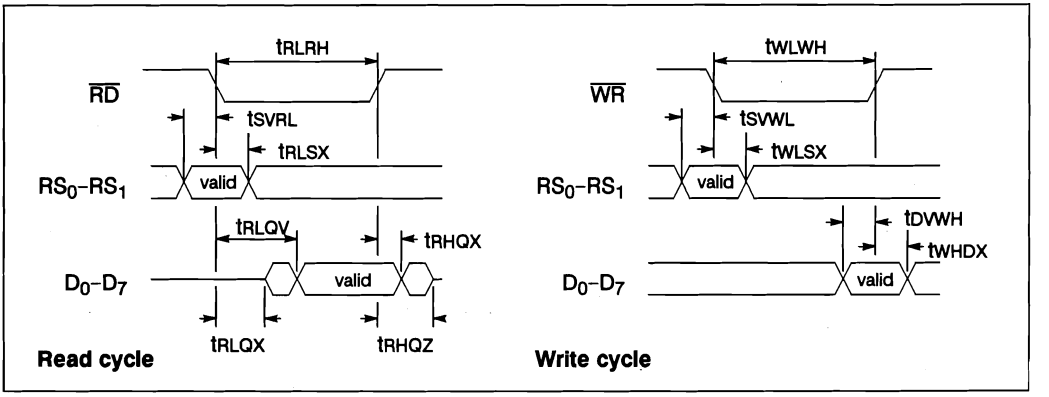


Figure 3.5 Basic read/write cycles

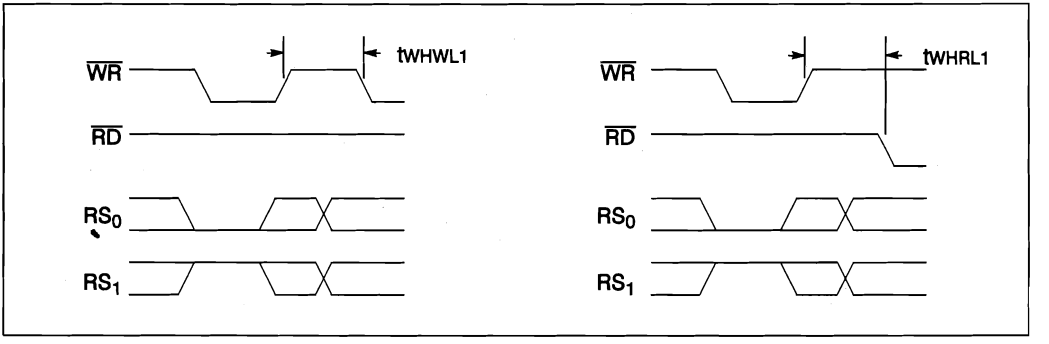


Figure 3.6 Write to pixel mask register followed by any access

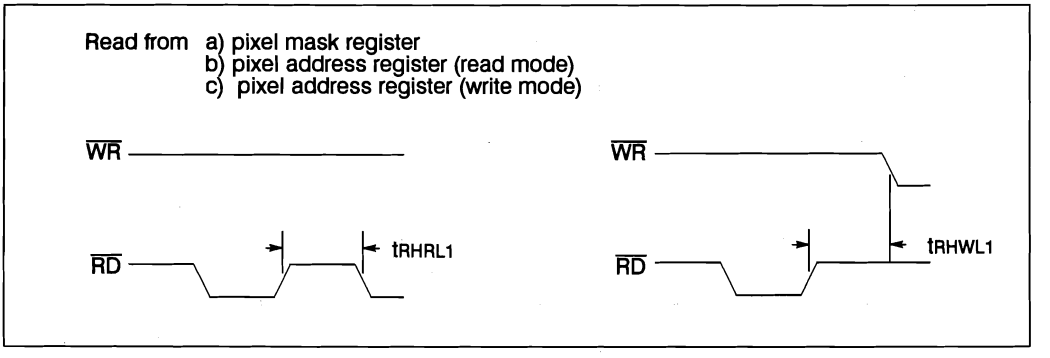


Figure 3.7 Read from register followed by any access

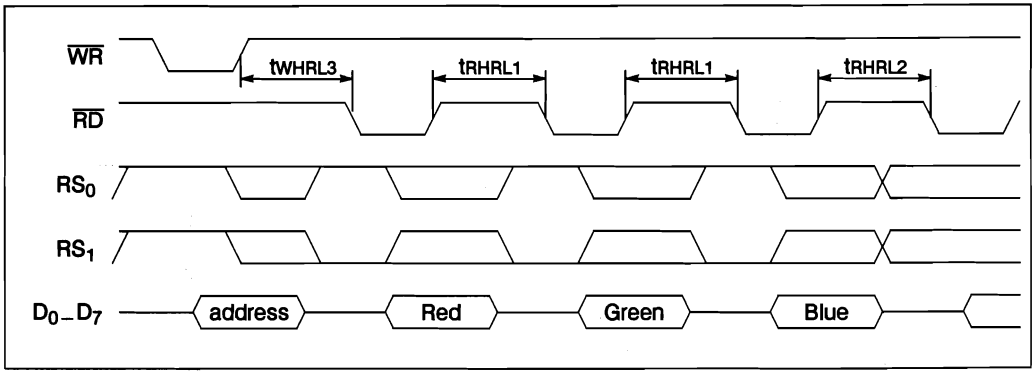


Figure 3.8 Colour value read followed by any read

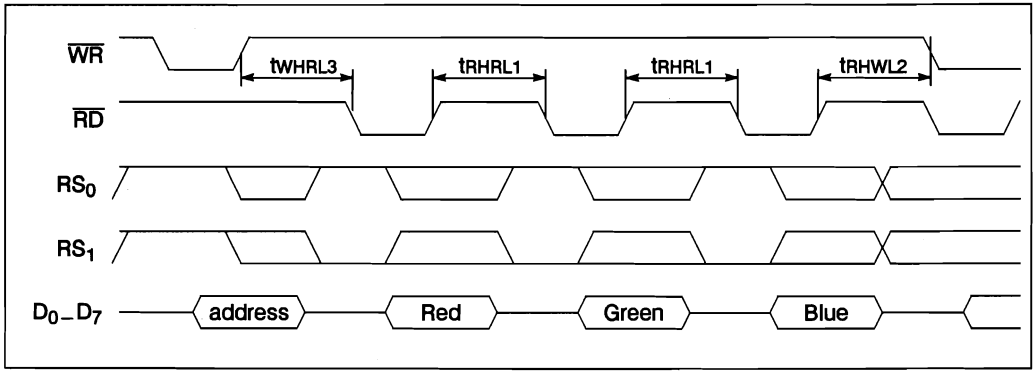


Figure 3.9 Colour value read followed by any write

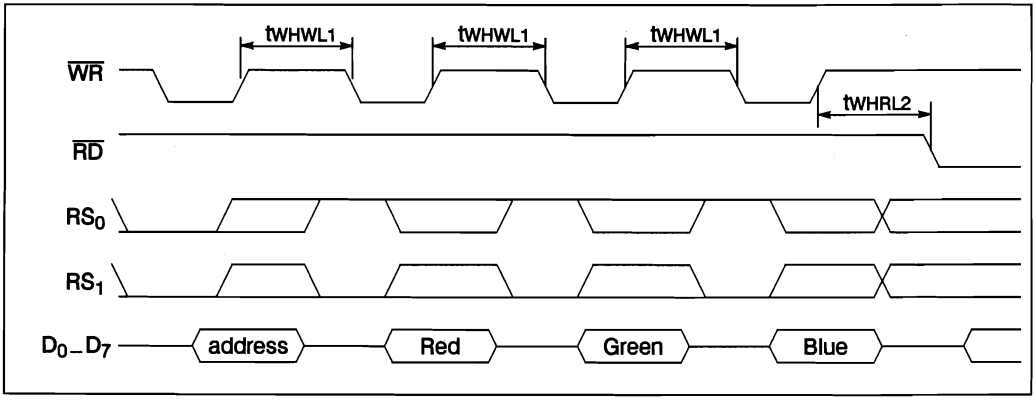


Figure 3.10 Colour value write followed by any read

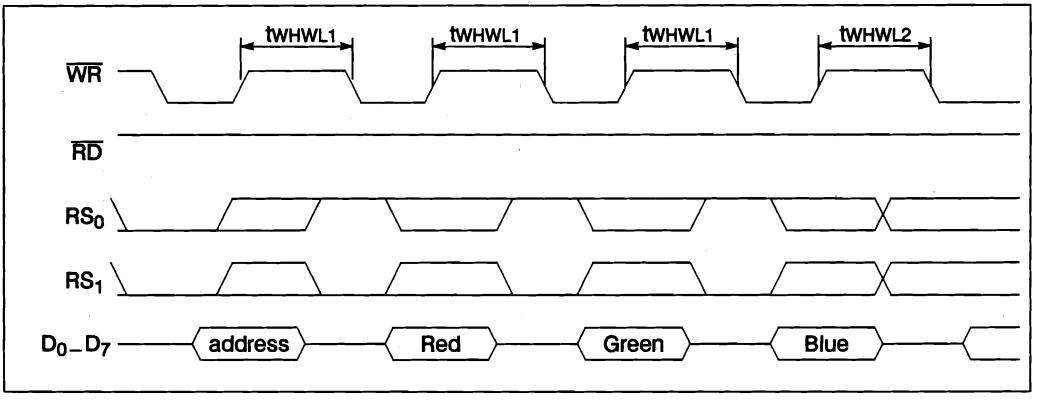
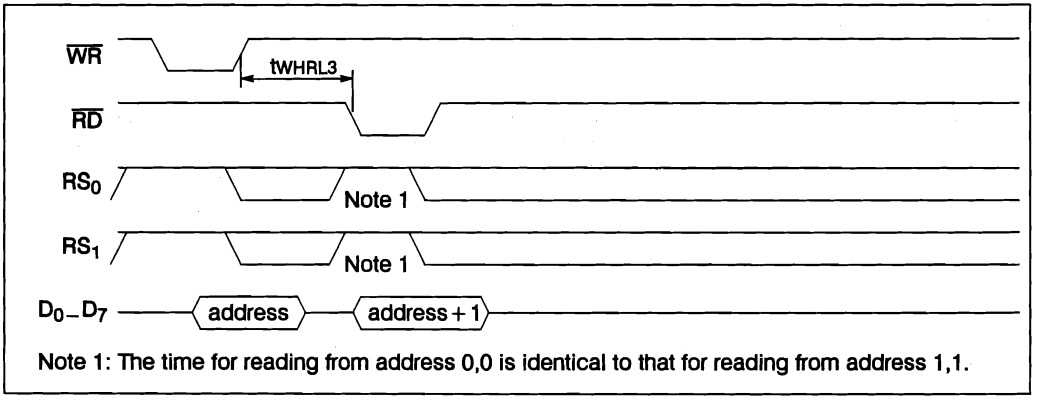
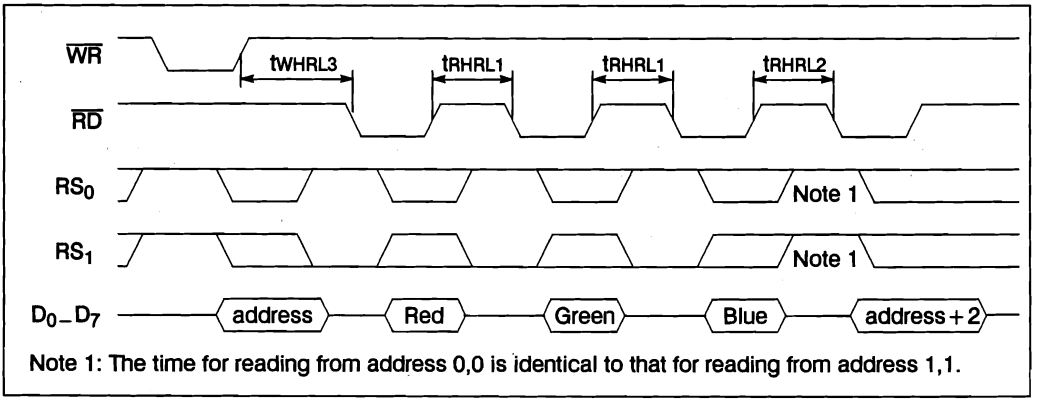


Figure 3.11 Colour value write followed by any write



Note 1: The time for reading from address 0,0 is identical to that for reading from address 1,1.

Figure 3.12 Write and read back address register (read mode)



Note 1: The time for reading from address 0,0 is identical to that for reading from address 1,1.

Figure 3.13 Read colour value then the address register (read mode)

3.4 Designing with the IMS G171

3.4.1 Board layout – general

The IMS G171 is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G171. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

3.4.2 Power supply decoupling

To supply the transient currents required by the IMS G171 the impedance in the decoupling path between VCC and VSS should be a 0.1 μF high frequency capacitor in parallel with a larger tantalum capacitor with a value between 22μ F and 47μF. An inductance may be added in series with the positive supply to form a low pass filter and so further improve the power supply local to the IMS G171.

The combination of series impedance in the ground supply to the IMS G171 and transients in the current drawn by the IMS G171 will appear as differences in the VSS voltages to the IMS G171 and to the digital devices driving it. To minimise this differential ground noise the impedance in the ground supply between the IMS G171 and the digital devices driving it should be minimised.

3.4.3 Analogue output – line driving

The DACs in the IMS G171 are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G171 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good signal fidelity, RF techniques should be observed. The PCB trace connecting the IMS G171 to the off board connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect from the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus, a double terminated DAC output will rise faster than any singly terminated output.

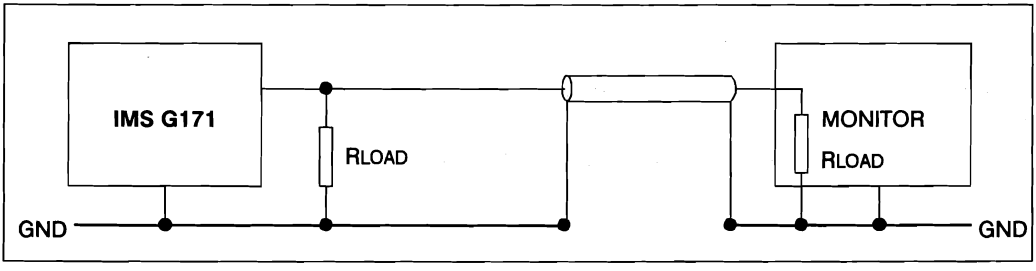


Figure 3.14 Double termination

Buffered signal

If the IMS G171 is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

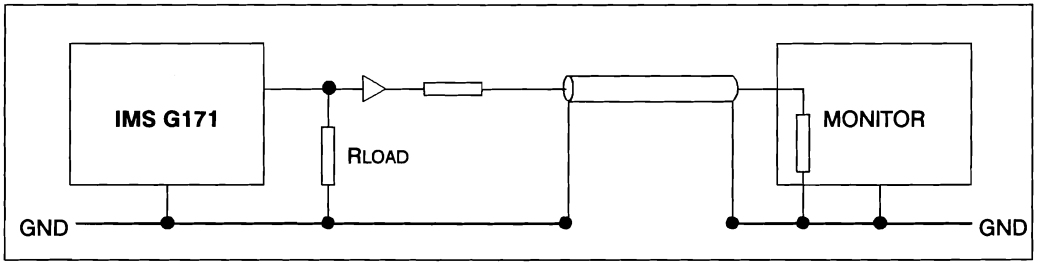


Figure 3.15 Buffered signal

3.4.4 Analogue output – protection

CMOS devices are susceptible to damage from from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G171 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G171 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection devices (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figure 3.17).

3.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G171 behave like low impedance transmission lines driven from a low impedance source and terminated with a high impedance. In accordance with transmission line principles signal transitions will be reflected from the high impedance input to the IMS G171. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a value around 100Ω will be required. Because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

3.4.6 Current reference – design

To ensure that the output current of the DACs is predictable and stable with temperature variations an active current reference is recommended. Figure 3.16 shows four designs of current reference.

Figure 3.16(d) shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of VCC.

Figures 3.16(a)-(c) are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuit 3.16(b) and 3.16(c) the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 3.16(c)).

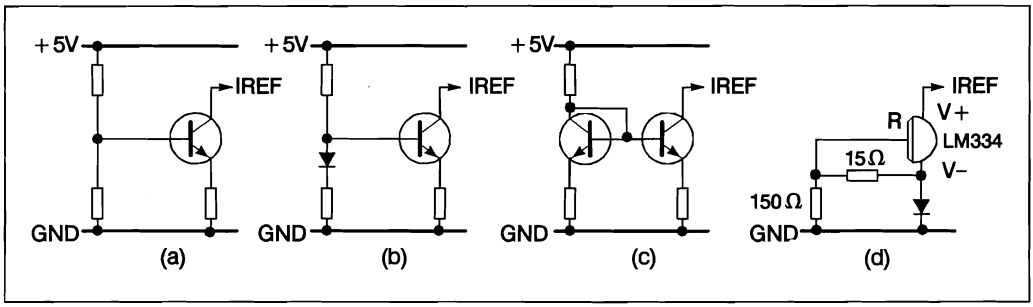


Figure 3.16

3.4.7 Current reference – decoupling

The DACs in the IMS G171 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capacitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VCC. This will enable the current reference to track both low and high frequency variations in the supply.

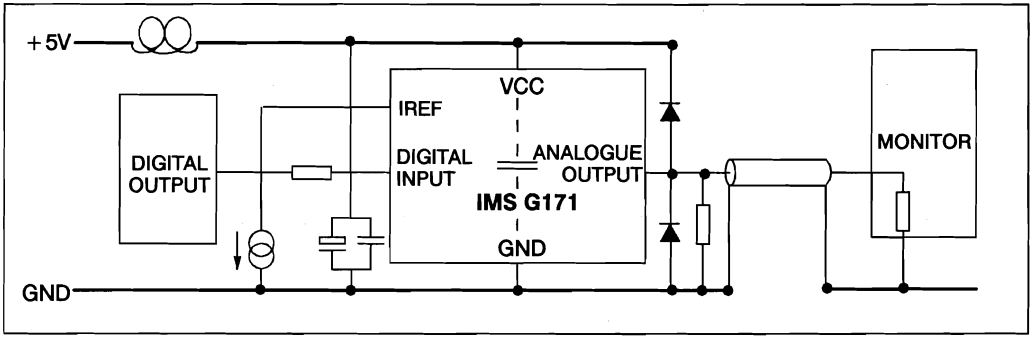


Figure 3.17 Circuit incorporating suggested design features

3.4.8 Pixel Mask register synchronisation

Each pixel address used as an address into the colour look-up table is masked by the Pixel Mask register. If the contents of the Pixel Mask register are modified asynchronously to PCLK there is a possibilty that the data held within the Pixel Mask register will change at such an instant as to corrupt the address applied to the look-up table as it is being latched.

If the Pixel Mask register is only initialised once on power up the synchronisation precautions described below need not be taken, it is sufficient simply to ensure that the colour look-up table is initialised after the

Pixel Mask register. The synchronous properties of the Pixel Mask register in no way affect the ability to update the look-up table asynchronously,

If the Pixel Mask register is to be updated on a regular basis, asynchronously to PCLK, corruption of the look-up table contents will inevitably occur. To prevent such corruption the update of the mask register should occur at a time which ensures that the internal pixel mask value is not changing between values as it is being sampled. This requires that certain timing constraints synchronising $\overline{WR}$ to PCLK are met (see table 3.1).

The circuit given in figure 3.18 should be suitable for systems with pixel rates up to 35 MHz. The synchronisation circuity required for systems working above 35MHz may be more complex.

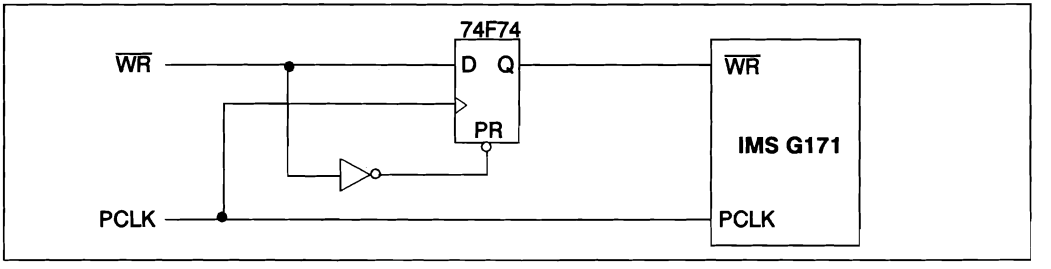


Figure 3.18

Symbol	Parameter	All Max.	35MHz Min.	50 MHz Min.	Units	Notes
t_{WLCH}	$\overline{WR}$ Ilegal transition window	12	1	1	ns	1,2
t_{DVWL}	Data setup time		15	15	ns	2
t_{WHDX}	Data hold time		15	10	ns	

Table 3.1 Pixel mask register synchronisation

Notes

1 $\overline{WR}$ should not change from high to low within the window delimited by the minimum and maximum times specified.

2 This parameter need only be observed if modifications of the value held in the Pixel Mask register are required to occur synchronously to the pixel stream.

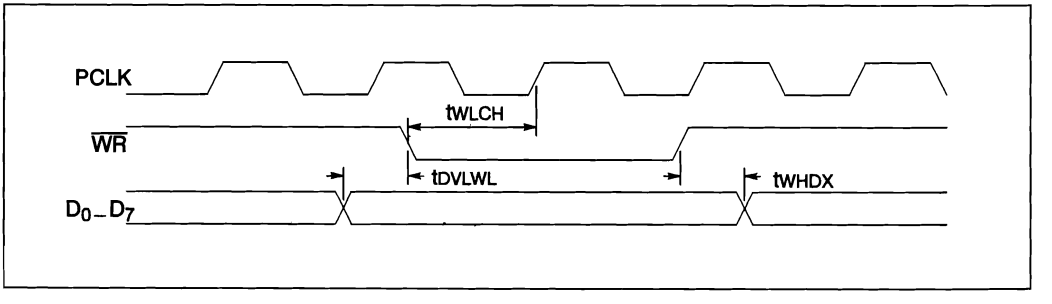


Figure 3.19 Pixel mask register synchronisation.

3.5 Package specifications

3.5.1 28 pin dual-in-line package

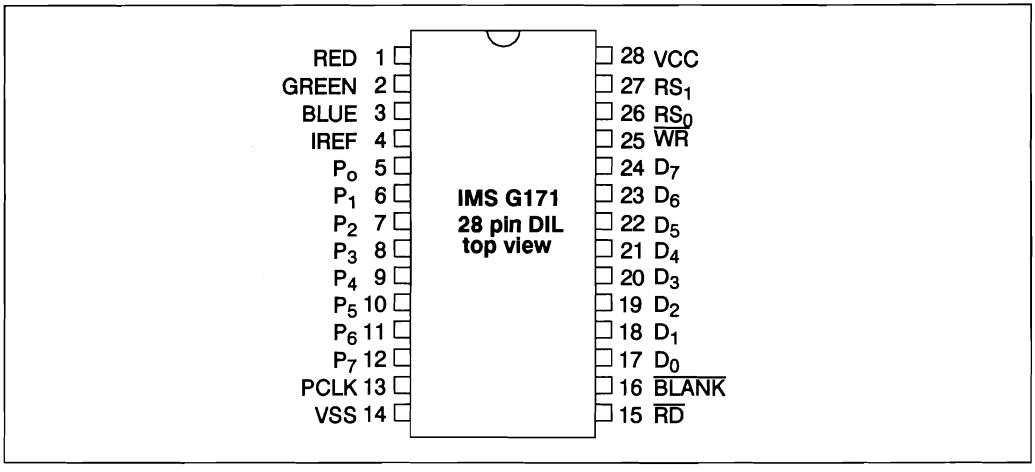


Figure 3.20 IMS G171 28 pin dual-in line package pinout

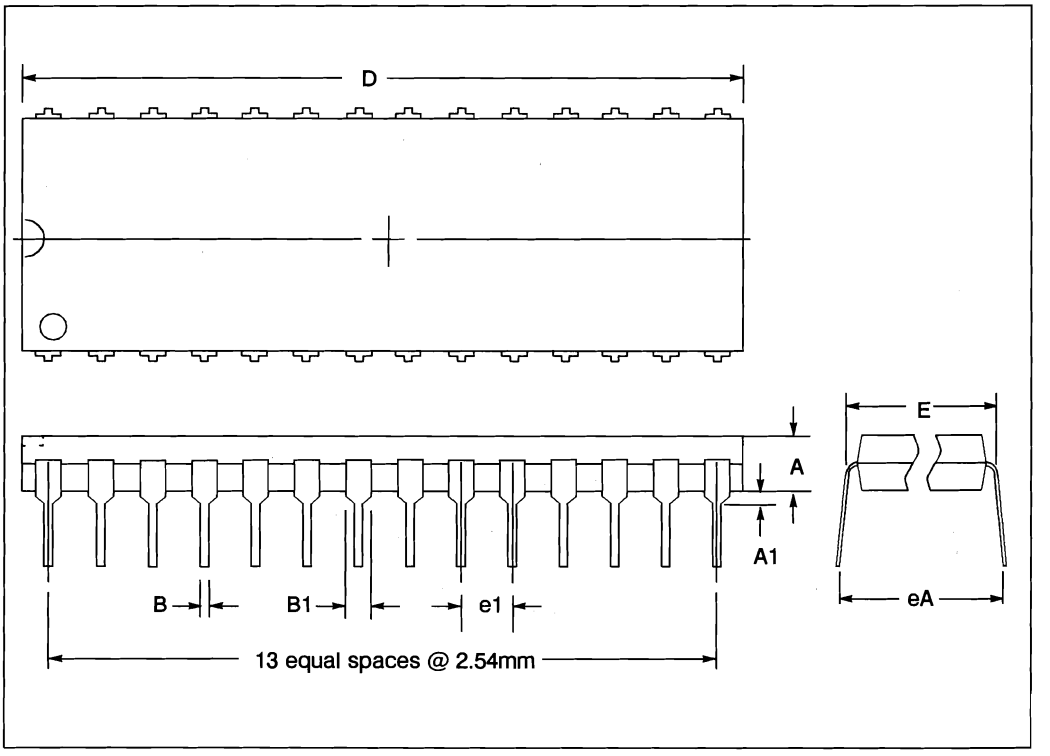


Figure 3.21 28 pin plastic dual-in-line package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	3.556	4.064	0.140	0.160	
A1	0.508		0.020		
B	0.305		0.012		
B1	1.524		0.060		Typical
D	36.449	37.211	1.435	1.465	
E	15.164	15.316	0.597	0.603	
e1	2.286	2.794	0.090	0.110	
eA	15.848	16.644	6.240	0.655	

Table 3.2 28 pin plastic dual-in-line package dimensions

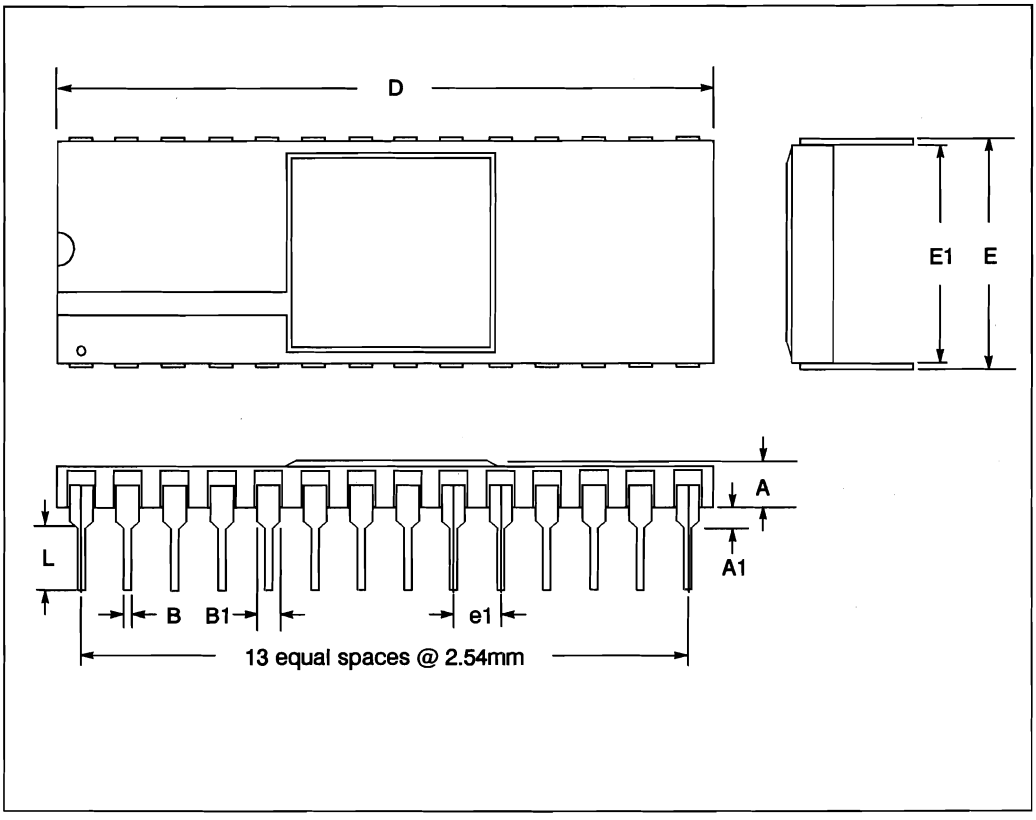


Figure 3.22 28 pin ceramic dual-in-line package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	2.237	2.695	0.088	0.106	
A1	1.016	1.524	0.040	0.060	
B	0.406	0.508	0.016	0.020	
B1		1.524		0.060	
D	35.204	35.916	1.386	1.414	
E	15.240	15.748	0.600	0.620	
E1		15.494		0.610	
e1	2.540		0.100		Nominal
L	3.048		0.120		

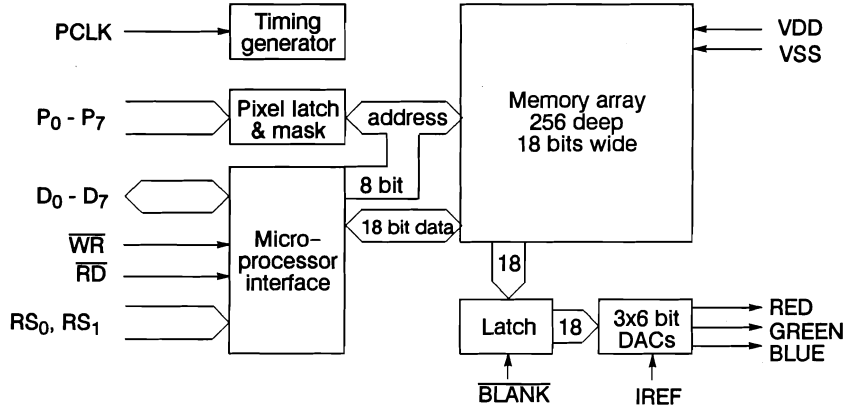
Table 3.3 28 pin ceramic dual-in-line package dimensions

3.5.2 Ordering information

Device	Clock rate	Package	Part number
IMS G171	35 MHz	Plastic DIP	IMSG171P-35C
IMS G171	50 MHz	Plastic DIP	IMSG171P-50S
IMS G171	35 MHz	Ceramic DIP	IMSG171S-35C

IMS G176
IMS G176L
High performance CMOS colour look-up table

Designed to be compatible with IBM PS/2, VGA graphics systems



FEATURES

- Compatible with the RS170 video standard.
- Pixel rates up to 66MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun.
- Composite blank on all three channels.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- Up to 8 bits per pixel.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V power supply.
- Low power dissipation, 950mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL or 32 pin or 44 pin Plastic LCC.
- Pin compatible with IMS G171.
- Power down capability.

DESCRIPTION

The IMS G176/L integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 28 pin DIL, 32 pin or 44 pin PLCC package. The IMS G176L is a power down version of the IMS G176.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite blank signals can be generated on all three outputs.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G176 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

4.1 Pin designations

4.1.1 Pixel Interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
PCLK	13	14	40	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
P_0-P_7	5-12	6-13	32-39	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the colour look-up table.
$\overline{BLANK}$	16	20	7	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.

4.1.2 Analogue Interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
RED BLUE GREEN	1 2 3	2 3 4	25 26 27	O O O		These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. The number of current sources active is controlled by the 6 bit binary value applied.
IREF	4	5	28	I	Reference current	The reference current drawn from VDD (or AVDD) via the IREF pin determines the current sourced by each of the current sources in the DACs.

4.1.3 Microprocessor Interface

Signal	Pin number			I/O	Signal name	Description
	DIL	PLCC				
		32	44			
$\overline{WR}$	25	29	16	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	15	19	6	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	26,27	30,31	17,18	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
D_0–D_7	17–24	21–28	8–15	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G176/L under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.

4.1.4 Power supply

Signal	Pin number			Signal name	Description
	DIL	PLCC			
		32	44		
VDD	28			Power supply	Digital and analogue supply pads are bonded out to a single pin on the DIL package. The package contains a high-frequency decoupling capacitor between VDD and VSS to ensure a high quality analogue supply.
VDD		17	4,21,22	Digital supply	Digital and analogue supply pads are bonded out separately on the PLCC package to give highest possible noise immunity. Due to package size limitations the decoupling capacitor capacitor must be provided externally (see section on 'Power supply decoupling')
AVDD		32	20	Analogue supply	
VSS	14	16	3	Ground	

4.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
0	0	8	Address (write mode)	There is a single Address register within the IMS G176/L. This register can be accessed through either register select 0,0 or 1,1 Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to register 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the look-up table addressed and then increments the Address register. A read from register 0,0 is functionally equivalent to a read from 1,1.
0	1	18	Colour Value	The Colour Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits D_0–D_5 are used. When a byte is read only the least significant six bits contain information – the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operations of the IMS G176/L for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P_0–P_7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed via that interface.

4.2 Device description

The IMS G176/L is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 × 18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18 bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 66 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G176/L. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation, overlays and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

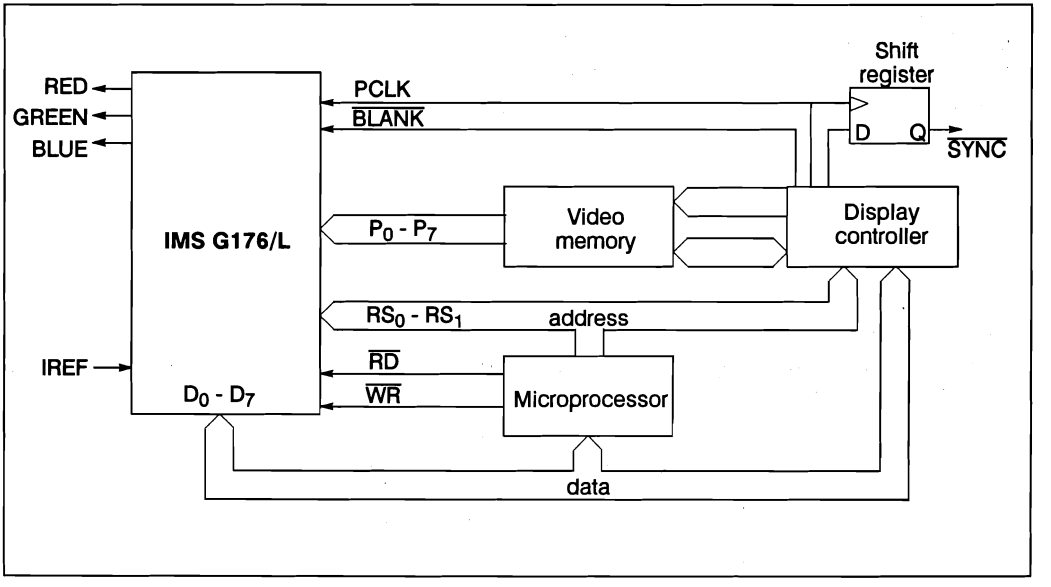


Figure 4.1Typical IMS G176/L application

4.2.1 Video path

P_0–P_7 and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analogue outputs after three further rising edges of Pixel Clock (see figure 4.2).

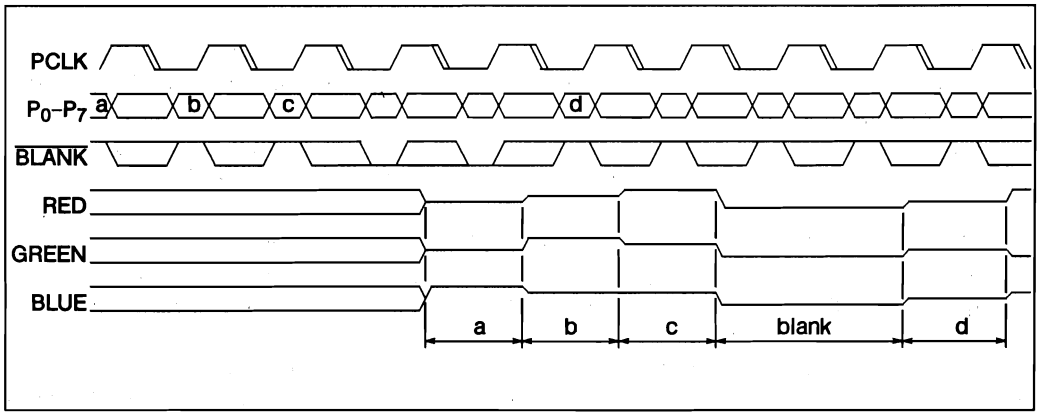


Figure 4.2

4.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 9.07 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The $\overline{BLANK}$ input to the IMS G176/L acts on all three of the analogue outputs. When the $\overline{BLANK}$ input is low a binary zero is applied to the inputs of the DACs.

The expression for calculating IREF with various peak white voltage/output loading combinations is given below:

$$IREF = \frac{V_{PEAKWHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note that for all values of IREF and output loading:

$$V_{BLACK\ LEVEL} = 0$$

4.2.3 Microprocessor Interface

Below are listed the three microprocessor interface registers within the IMS G176/L and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address register.

Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous microprocessor interface access

Accesses to all registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G176/L. Data transfers between the look-up table and the Colour Value register and modifications to the Pixel Mask register are synchronised to the Pixel Clock by internal logic. This is done in the period between microprocessor accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers or modifications to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is completely independent of the Address and Colour Value registers.

4.3 Electrical specifications

4.3.1 Absolute maximum ratings *

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	VSS-1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	-55	,125	°C	
TA	Temperature under bias	-40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	-15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VDD	Positive supply voltage	4.50	5.0	5.50	volts	2,3,IMS G176/L-40/50
VDD	Positive supply voltage	4.75	5.0	5.25	volts	2,3,IMS G176/L-66
VSS	Ground		0		volts	
VIH	Input logic '1' voltage	2.0		VDD+0.5	volts	3
VIL	Input logic '0' voltage	−0.5		0.8	volts	4
TA	Ambient operating temperature	0		70	°C	5
IREF	Reference current	−7.0		−10	mA	6

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 These voltage ranges apply equally for AVDD and VDD when using the PLCC packaged device.

4 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

5 With a 400 linear ft/min transverse air flow.

6 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
IDD	Average power supply current		190	mA	4, IMS G176/L-66
IDD	Average power supply current		160	mA	4, IMS G176/L-50
IDD	Average power supply current		155	mA	4, IMS G176/L-40
VREF	Voltage at IREF input (pin 4)	VDD−3	VDD	volts	5
IIN	Digital input current (any input)		±10	μA	6,7
IOZ	Off state digital output current		±50	μA	6,8
VOH	Output logic '1'	2.4		volts	IO = −5mA
VOL	Output logic '0'		0.4	volts	IO = 5mA

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). IDD is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 These voltages apply equally for AVDD and VDD when using the PLCC packaged device.

6 VDD = max, VSS $\leq$ VIN $\leq$ VDD.

7 On digital inputs (P_0–P_7, PClk, $\overline{RD}$, $\overline{BLANK}$, $\overline{WR}$ and RS_0–RS_1).

8 On digital input/output (D_0–D_7).

4.3.3 Power down

The IMS G176L is a 'power-down' version of the IMS G176. It is designed to support the lap-top market which requires the colour look-up table to dissipate minimal power when not in use.

Symbol	Parameter	Min.	Max.	Units	Notes
IDDSB	Standby power supply current		10	mA	1-5

Notes

1 All voltages with respect to VSS unless otherwise stated.

2 Table 4.1 defines the conditions required to guarantee IDD standby.

3 PCLK should be held DC low as specified in table 4.1.

4 $\overline{RD}$ should be held high as specified in table 4.1 to prevent the data pins (D0-D7) from driving and therefore drawing supply current. If, however there is no external load resistance between D0-D7 data pins and GND or VDD, then taking $\overline{RD}$ low will have no detrimental effect on IDD standby.

5 The voltage on any pin shall not be greater than VDD or less than VSS.

Pin name	Required value	Units	Notes
RED	$\geq$0 and $\leq$VDD	V	
GREEN	$\geq$0 and $\leq$VDD	V	
BLUE	$\geq$0 and $\leq$VDD	V	
IREF	<10	µA	
P0-P7	<0.2	V	
PCLK	<0.2	V	
RD	>VDD-0.2	V	
BLANK	<0.2 or >VDD-0.2	V	
D0-D7	<0.2	V	
WR	>VDD-0.2	V	
RS0	<0.2 or >VDD-0.2	V	
RS1	<0.2 or >VDD-0.2	V	
VDD	4.5<VDD<5.5	V	

Table 4.1 Conditions to guarantee IDD standby

4.3.4 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1,2,3)
	Resolution	6			bits	
VO(max)	Output voltage			1.5	volts	IO≤10mA
IO(max)	Output current			−21	mA	VO≤1V
	Full scale error			±5	%	4
	DAC to DAC correlation error			±2	%	5
	Integral linearity error			±0.5	LSB	6
	Rise time (10% to 90%)			6	ns	7, IMS G176/L-66
	Rise time (10% to 90%)			8	ns	7, IMS G176/L-40/50
	Full scale settling time			15.3	ns	7,8,9, IMS G176/L-66
	Full scale settling time			20	ns	7,8,9, IMS G176/L-50
	Full scale settling time			25	ns	7,8,9, IMS G176/L-40
	Glitch energy		120		pVsec	7,9

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = -9.07mA.

4 Full scale error from the value predicted by the design equations.

5 About the mid point of the distribution of the three DACs measured at full scale deflection.

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

7 Load = 37.5Ω + 30pF with IREF = -9.07mA.

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

4.3.5 AC test conditions

Input pulse levels	VSS to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure NO TAG

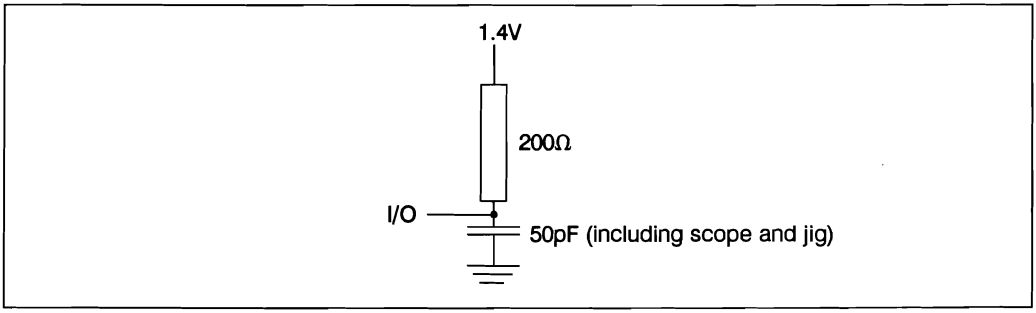


Figure 4.3Digital output load

4.3.6 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable D_0–D_7

4 BLANK $\leq$ VIL(max) to disable RED, GREEN and BLUE.

4.3.7 Video operation (figure 4.4)

Symbol	Parameter	All Max.	40 MHz Min.	50 MHz Min.	66 MHz Min.	Units	Notes
tCHCH	PCLK period	10000	25	20	15.1	ns	
ΔtCHCH	PCLK jitter	±2.5				%	1
tCLCH	PCLK width low	10000	9	6	5	ns	
tCHCL	PCLK width high	10000	7	6	5	ns	
tPVCH	Pixel address set-up time		5	4	3	ns	2
tCHPX	Pixel address hold time		5	4	3	ns	2
tBVCH	$\overline{BLANK}$ setup time		5	4	3	ns	
tCHBX	$\overline{BLANK}$ hold time		5	4	3	ns	
tCHAV	PCLK to valid DAC output	30	5	5	5	ns	3
ΔtCHAV	Differential output delay	2				ns	4
	Pixel clock transition time	50				ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

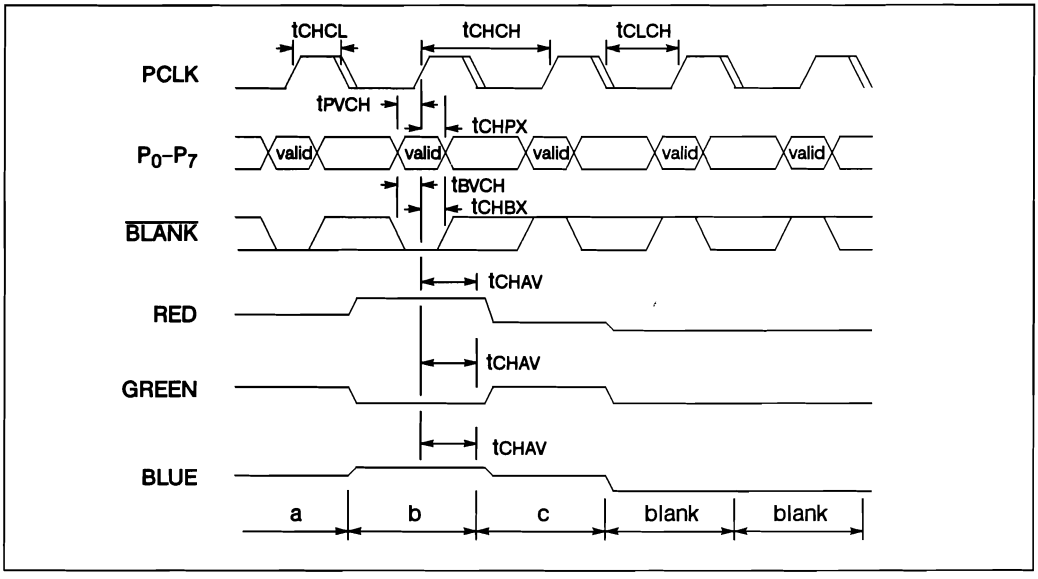


Figure 4.4 Video operation

4.3.8 Microprocessor interface operation

Symbol	Parameter	All	40 MHz	50 MHz	66 MHz	Units	Notes
		Max.	Min.	Min.	Min.		
tWLWH	$\overline{WR}$ pulse width low		50	50	50	ns	
tRLRH	$\overline{RD}$ pulse width low		50	50	50	ns	
tSVWL	Register select setup time		15	10	10	ns	
tSVRL	Register select setup time		15	10	10	ns	
tWLSX	Register select hold time		15	10	10	ns	
tRLSX	Register select hold time		15	10	10	ns	
tDVWH	Write data setup time		15	10	10	ns	
tWHDX	Write data hold time		15	10	10	ns	
tRLQX	Output turn-on delay		5	5	5	ns	
tRLQV	Read enable access time	40				ns	
tRHQX	Output hold time		5	5	5	ns	
tRHQZ	Output turn-off delay	20				ns	1
tWHWL1	Successive write interval						
tWHRL1	Write followed by read interval						
tRHRL1	Successive read interval						
tRHWL1	Read followed by write interval		4xtCHCH +30ns			ns	2
tWHWL2	Write after colour write						
tWHRL2	Read after colour write						
tRHWL2	Write after colour read						
tRHRL2	Read after colour read		6xtCHCH +40ns			ns	2
tWHRL3	Read after read address write						
tCYC	Write/Read cycle time		6xtCHCH +40ns			ns	2,3
	Write/Read enable transition time	50				ns	

Notes

1 Measured ±200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the microprocessor port are internally synchronised to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the microprocessor port being specified in terms of pixel clock periods.

In the case of the IMS G176/L the minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is 6×tCHCH +40ns.

For example, in the case of a 25MHz system the pixel clock period (tCHCH) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

$$6 \times 40ns + 40ns = 280ns$$

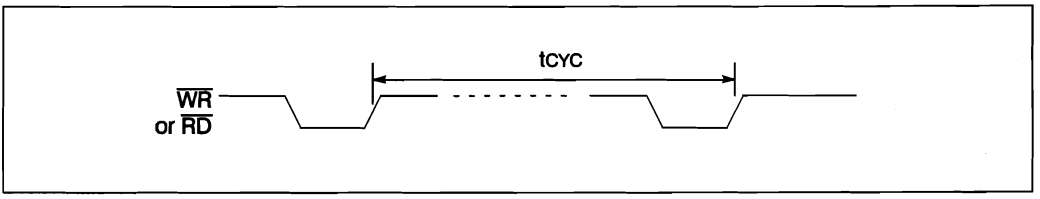


Figure 4.5 Write/Read cycle time

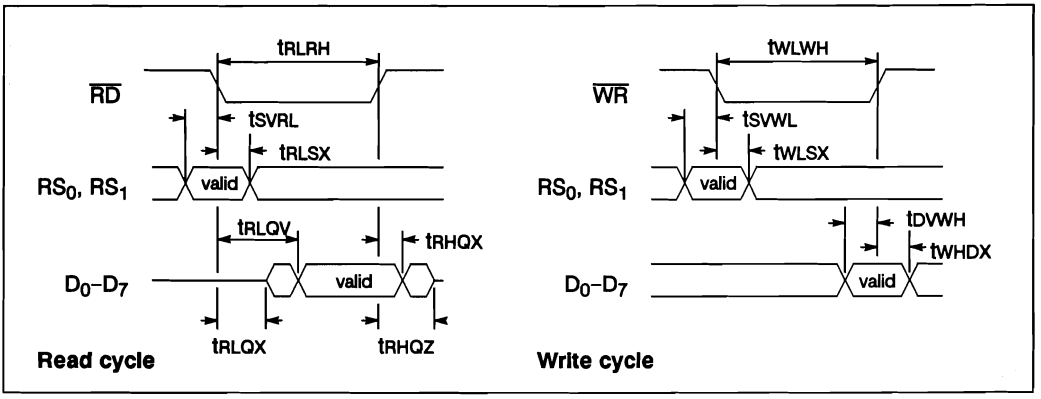


Figure 4.6 Basic read/write cycles

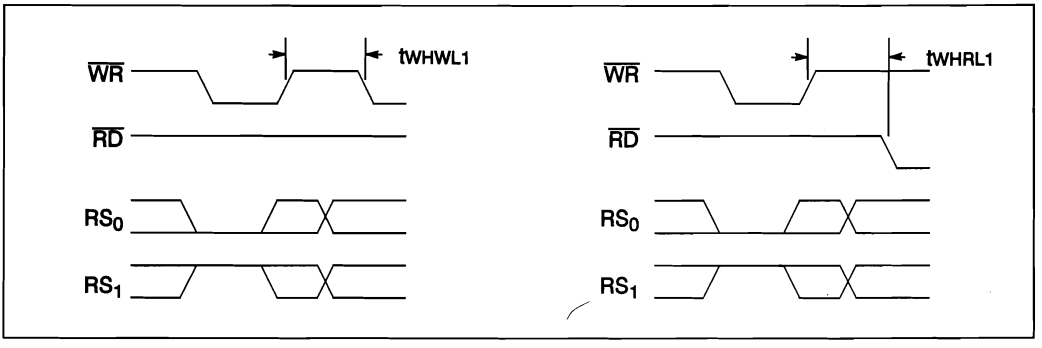


Figure 4.7 Write to pixel mask register followed by any access

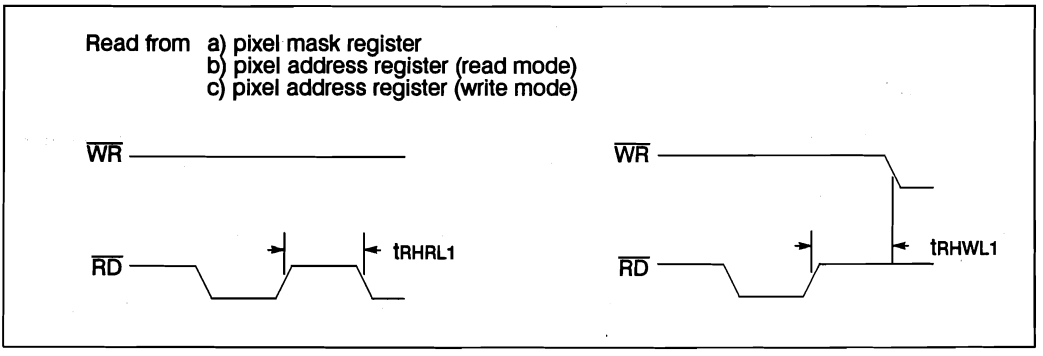


Figure 4.8 Read from register followed by any access

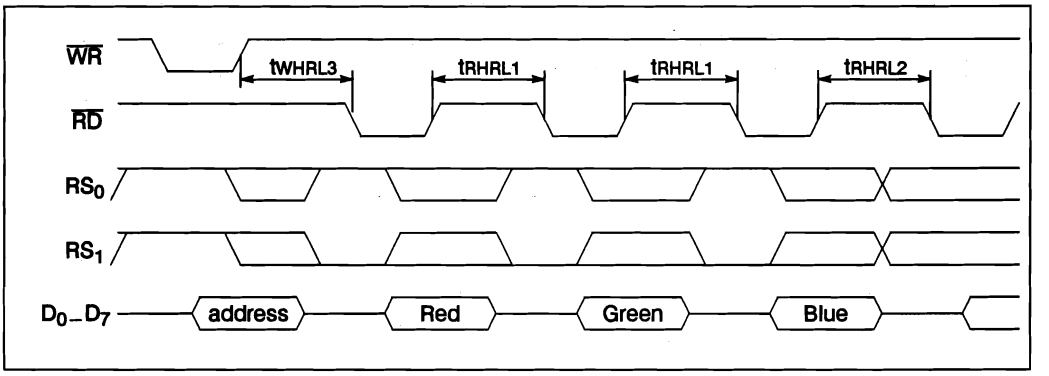


Figure 4.9 Colour value read followed by any read

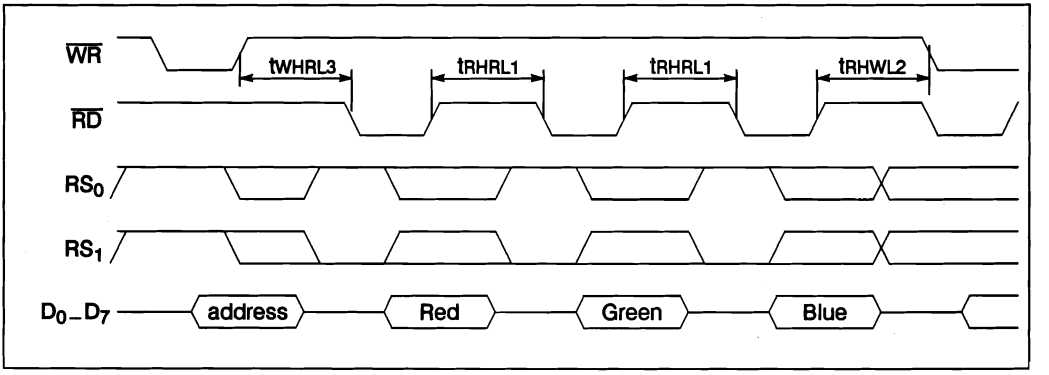


Figure 4.10 Colour value read followed by any write

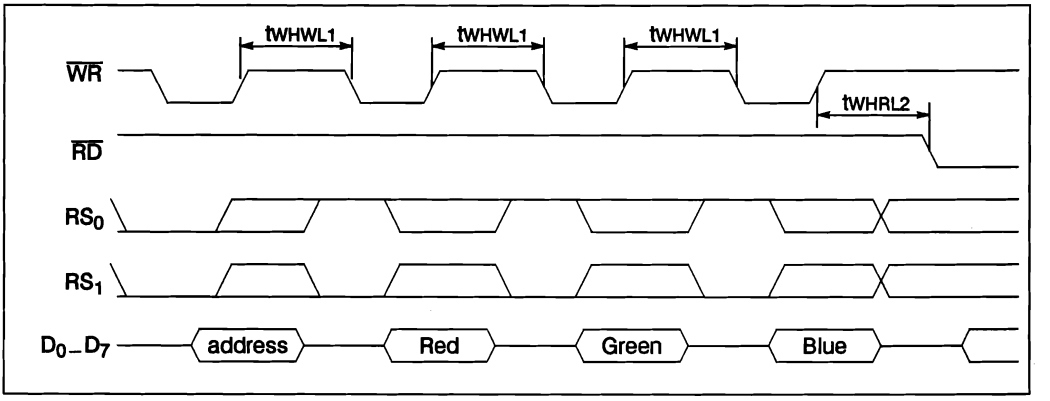


Figure 4.11 Colour value write followed by any read

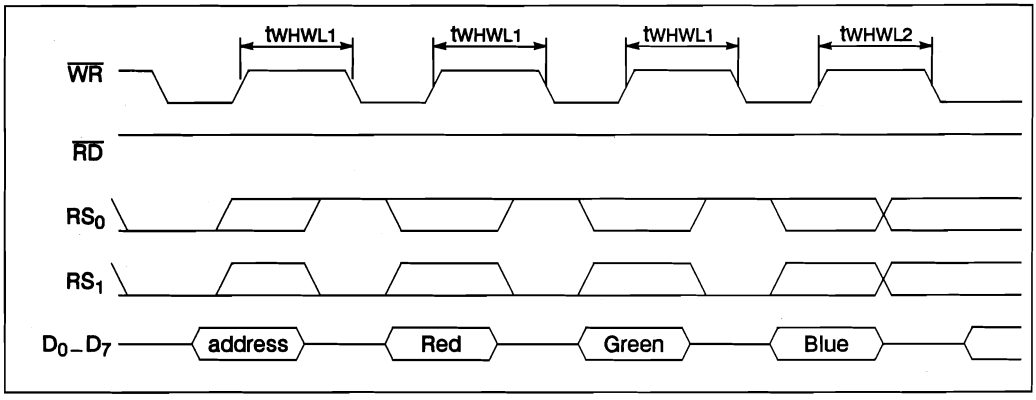


Figure 4.12 Colour value write followed by any write

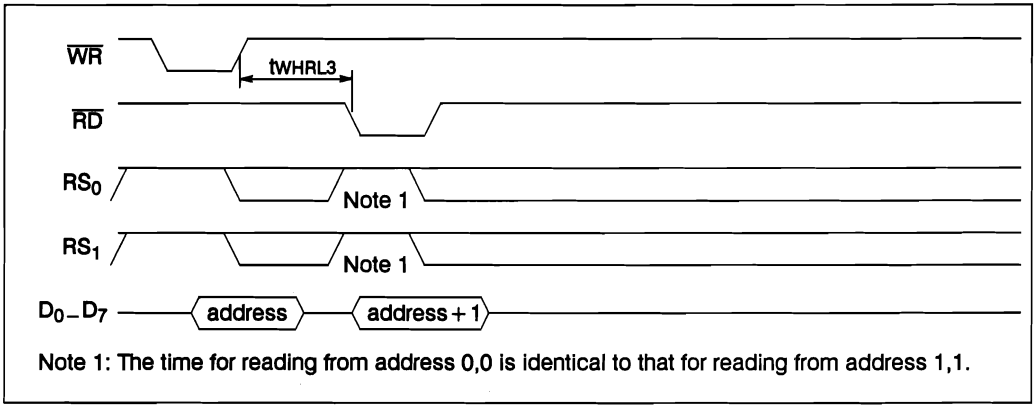


Figure 4.13 Write and read back address register (read mode)

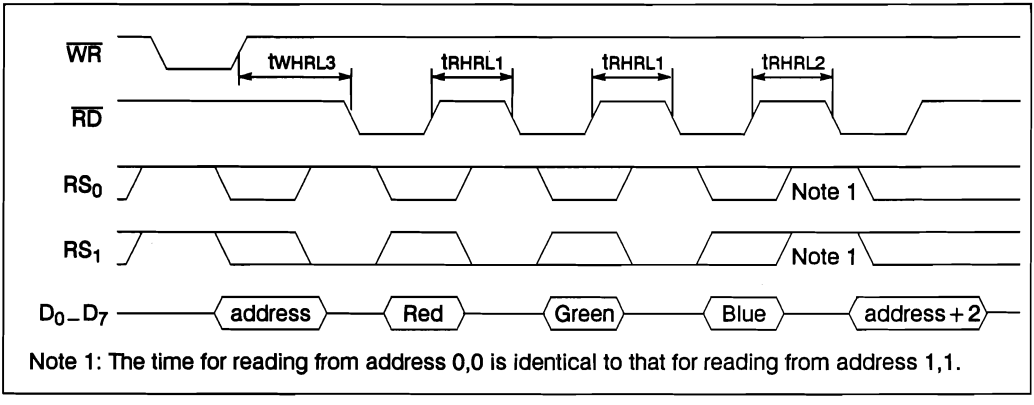


Figure 4.14 Read colour value then the address register (read mode)

4.4 Designing with the IMS G176/L

4.4.1 Board layout – general

The IMS G176/L is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G176/L. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

4.4.2 Power supply decoupling

The DACs in the IMS G176/L are referenced to the positive power supply, so are fairly insensitive to ground supply noise. To ensure that switching noise generated by the digital sections of the IMS G176/L is not transmitted to the DAC circuitry, independent analogue and digital +5V supplies are provided on-chip.

When packaged in a PLCC, the analogue and digital supplies are bonded out to separate pins. It is recommended that a high frequency capacitor of around 100nF (preferably a chip capacitor) should be placed as close as possible to the package between VDD and VSS. A large tantalum capacitor (between 22μF and 47μF) should also be placed in parallel with this high-frequency capacitor. AVDD should be connected to the positive power plane by the smallest impedance path possible, e.g. a via right next to a pin (see figure 4.18).

In the DIL package both the analogue and digital supplies are bonded out to a single pin (VDD). Again it is recommended that a high-frequency 100nF capacitor in parallel with a large tantalum capacitor are provided externally to ensure a high quality analogue supply (see figure 4.19).

An inductor may also be added in series with the positive supply (AVDD and or VDD) to form a low-pass filter and so further improve the power supply local to the IMS G176/L (figure 4.18).

4.4.3 Analogue output – line driving

The DACs in the IMS G176/L are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G176/L and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good signal fidelity, RF techniques should be observed. The PCB trace connecting the IMS G176/L to the offboard connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus, a double terminated DAC output will rise faster than any singly terminated output.

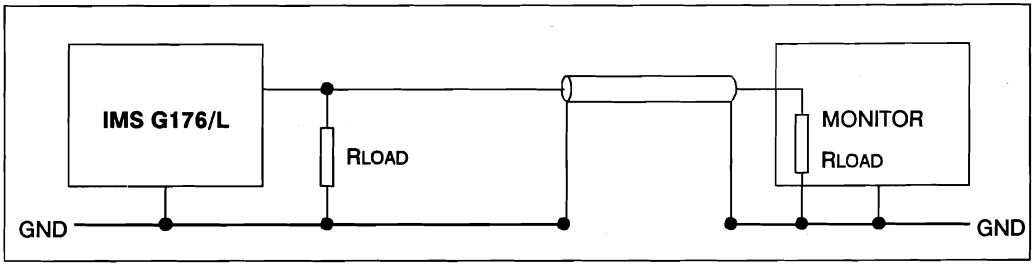


Figure 4.15 Double termination

Buffered signal

If the IMS G176/L is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

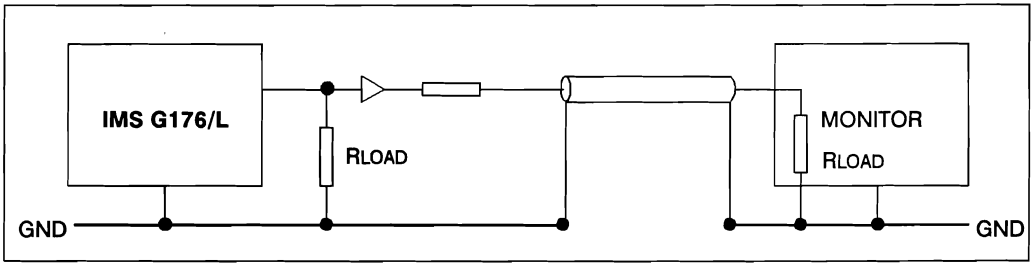


Figure 4.16 Buffered signal

4.4.4 Analogue output – protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G176/L during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G176/L are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection devices (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figures 4.18 and 4.19).

4.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G176/L and the input to the IMS G176/L have a low impedance source and are terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of the IMS G176/L. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing, and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimise reflections, but generally a value around 100Ω will be required. because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

4.4.6 Current reference – design

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 4.17 shows four designs of current reference.

Figure 4.17d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 4.17a-c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuits 4.17b and 4.17c the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 4.17c).

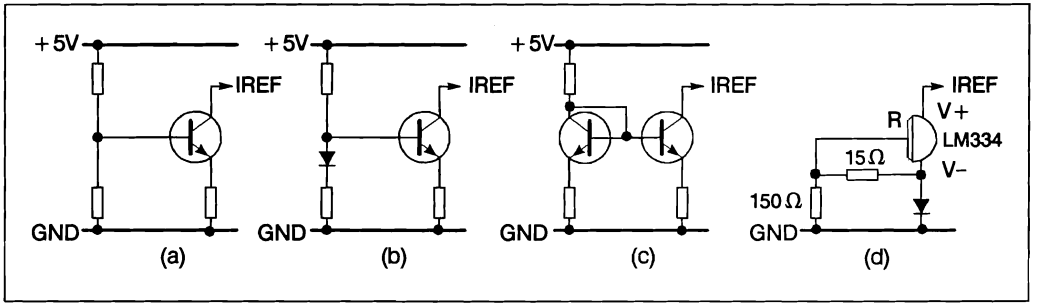


Figure 4.17

4.4.7 Current reference – decoupling

The DACs in the IMS G176/L are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VDD (or to AVDD if the PLCC package is used). This will enable the current reference to track both low and high frequency variations in the supply.

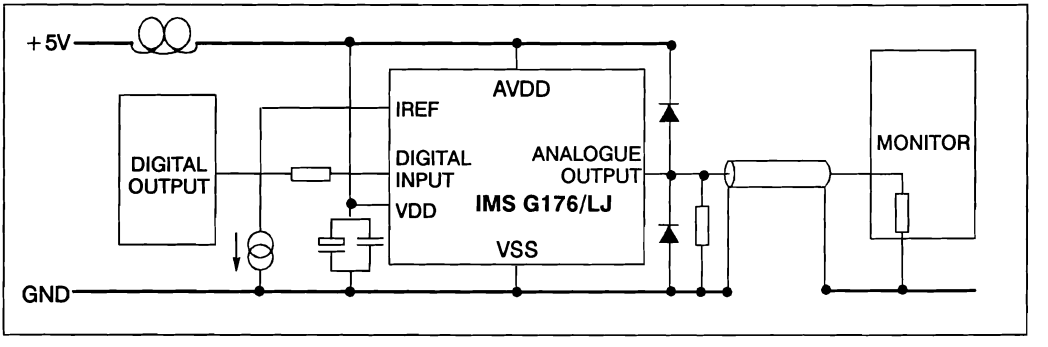


Figure 4.18 Suggested circuit using PLCC package

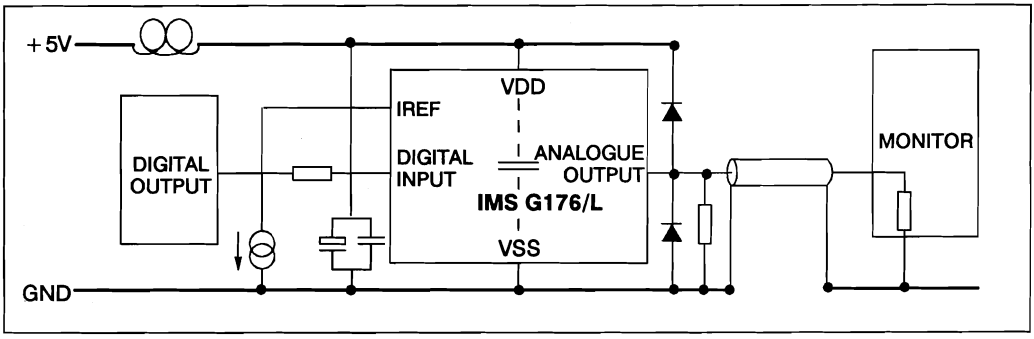


Figure 4.19 Suggested circuit using DIL package

4.5 Package specifications

4.5.1 28 pin dual-in-line package

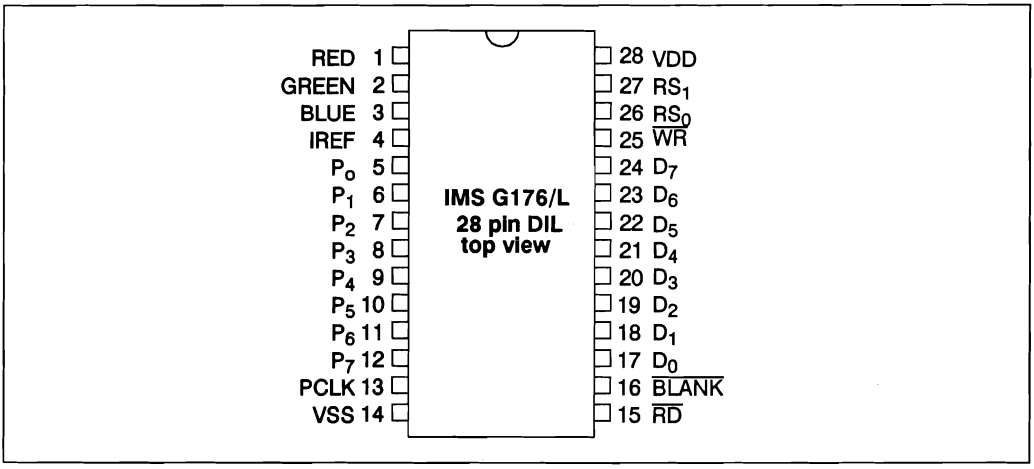


Figure 4.20 IMS G176/L 28 pin dual-in line package pinout

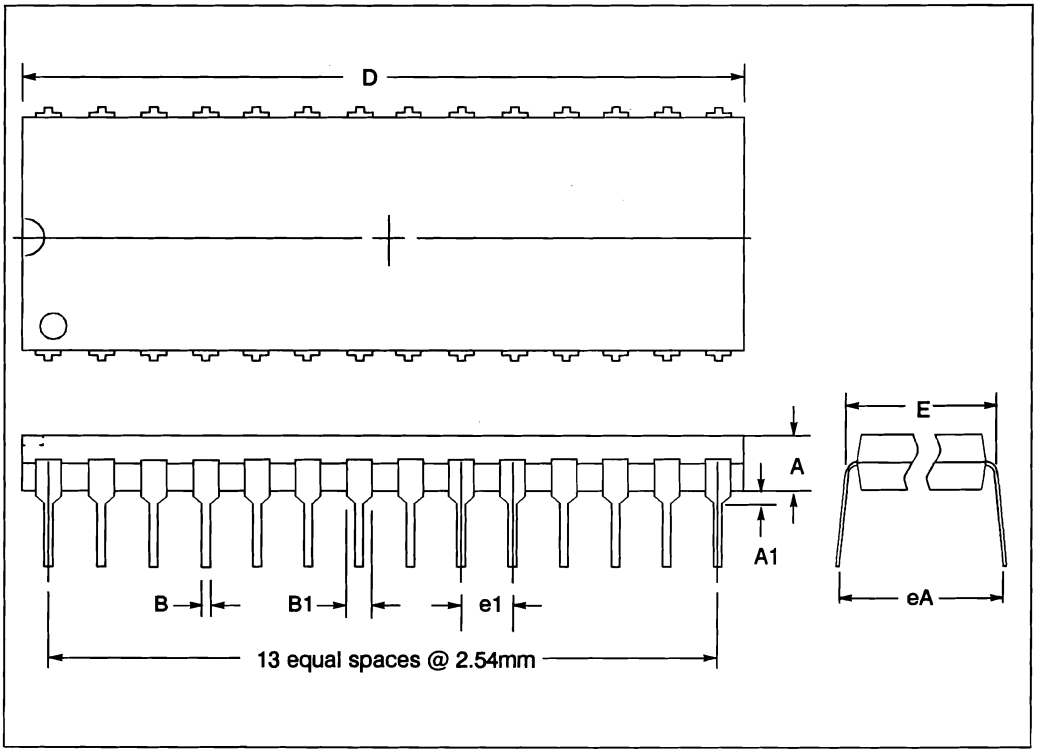


Figure 4.21 28 pin plastic dual-in-line package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	3.556	4.064	0.140	0.160	
A1	0.508		0.020		
B	0.305		0.012		
B1	1.524		0.060		Typical
D	36.449	37.211	1.435	1.465	
E	15.164	15.316	0.597	0.603	
e1	2.286	2.794	0.090	0.110	
eA	15.848	16.644	6.240	0.655	

Table 4.2 28 pin plastic dual-in-line package dimensions

4.5.2 32 pin plastic leaded-chip-carrier package

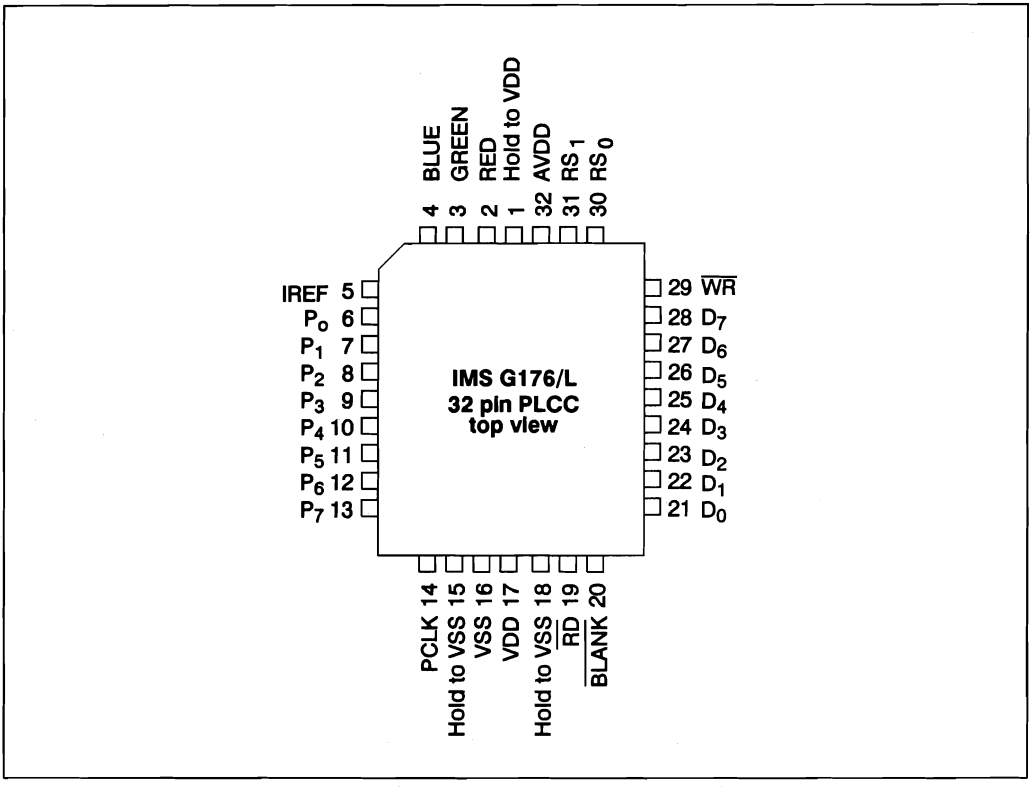


Figure 4.22 IMS G176/L 32 pin PLCC J-bend package pinout

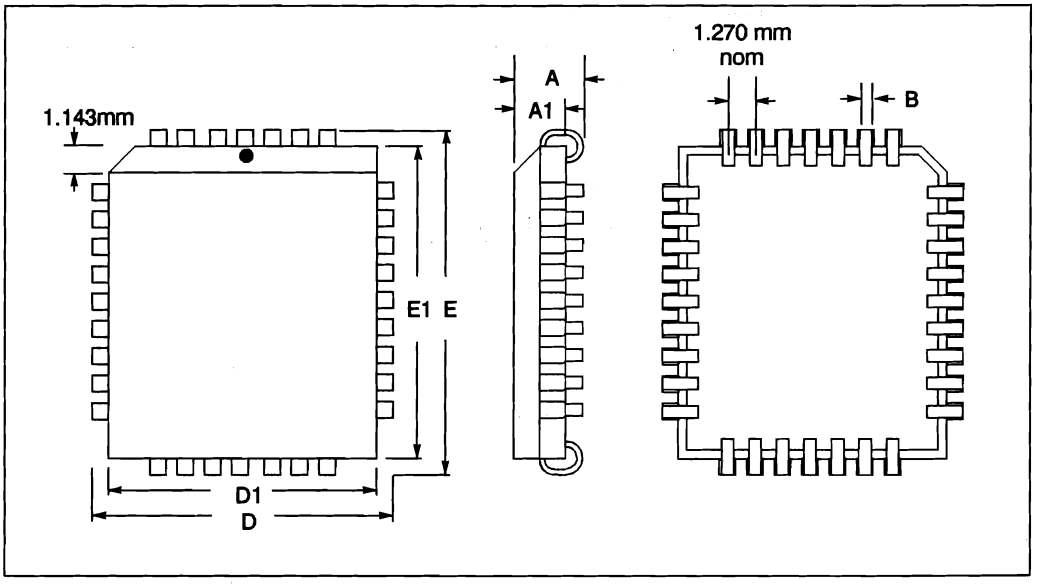


Figure 4.23 32 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	3.120	3.560	0.123	0.140	
A1	2.160		0.085		Nominal
B	0.432		0.017		Nominal
D	12.323	12.577	0.485	0.495	
D1	11.400	11.506	0.449	0.453	
E	14.859	15.113	0.585	0.595	
E1	13.940	14.046	0.549	0.553	

Table 4.3 32 pin PLCC J-bend package dimensions

4.5.3 44 pin plastic leaded-chip-carrier package

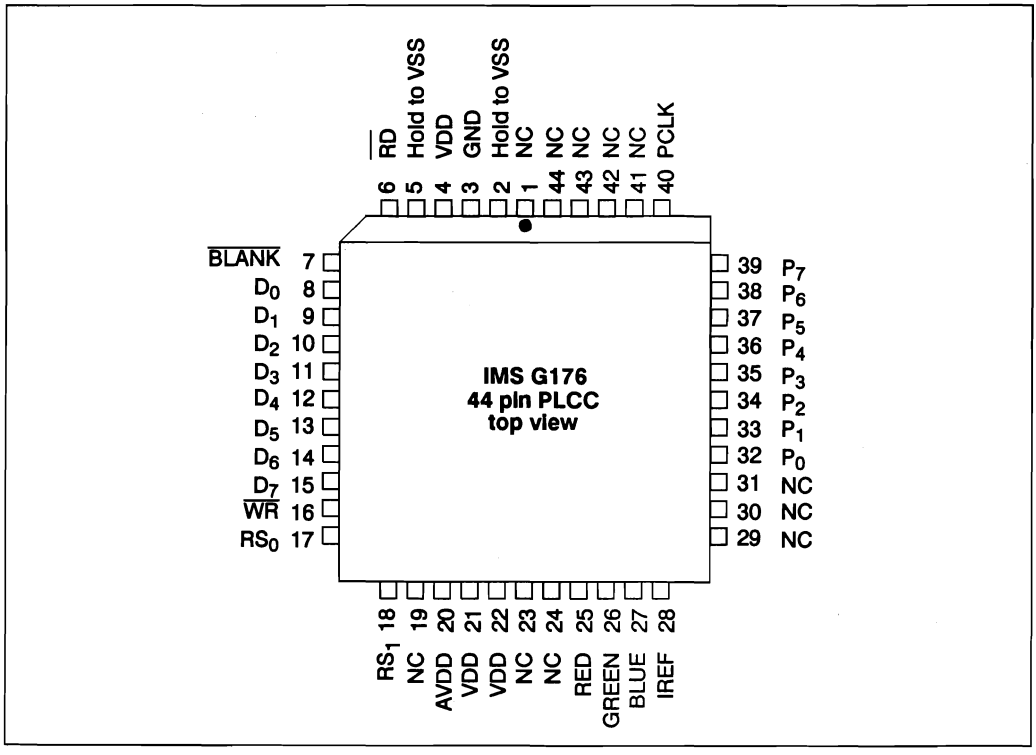


Figure 4.24 IMS G176 44 pin PLCC J-bend package pinout

Note

All **VDD** pins **must** be connected to the 5 Volt power supply.
All **GND** pins **must** be connected to ground.

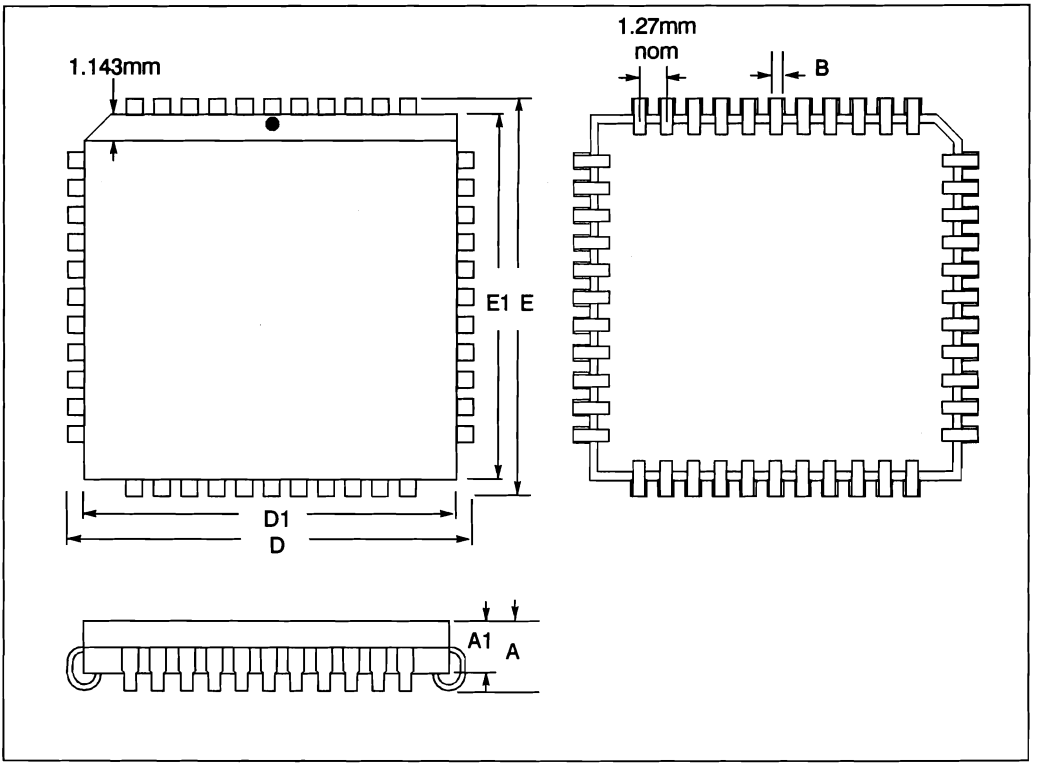


Figure 4.25 IMS G176 44 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	4.191	4.572	0.165	0.180	
A1	3.683	4.064	0.145	0.160	
B	0.457		0.018		
D	17.399	17.653	0.685	0.695	
D1	16.510	16.662	0.650	0.656	
E	17.399	17.653	0.685	0.695	
E1	16.510	16.662	0.650	0.656	

Table 4.4 44 pin PLCC J-bend package dimensions

4.5.4 Ordering Information

Device	Clock rate	Package	Part number	
			Standard	Low power
IMS G176	40 MHz	28 pin Plastic DIP	IMS G176P-40S	
IMS G176	50 MHz	28 pin Plastic DIP	IMS G176P-50S	IMS G176LP50S
IMS G176	66 MHz	28 pin Plastic DIP	IMS G176P-66S	
*IMS G176	80 MHz	28 pin Plastic DIP	IMS G176P-80S	
IMS G176	40 MHz	32 pin Plastic LCC	IMS G176J-40S	
IMS G176	50 MHz	32 pin Plastic LCC	IMS G176J-50S	IMS G176LJ50S
IMS G176	66 MHz	32 pin Plastic LCC	IMS G176J-66S	
*IMS G176	80 MHz	32 pin Plastic LCC	IMS G176J-80S	
IMS G176	40 MHz	44 pin Plastic LCC	IMS G176J-40Z	
IMS G176	50 MHz	44 pin Plastic LCC	IMS G176J-50Z	IMS G176LJ50Z
IMS G176	66 MHz	44 pin Plastic LCC	IMS G176J-66Z	
*IMS G176	80 MHz	44 pin Plastic LCC	IMS G176J-80Z	

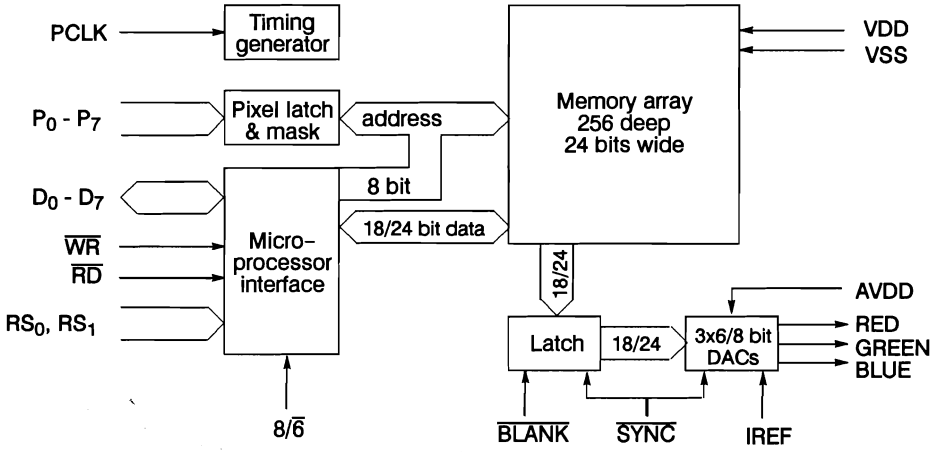
Note: IMS G176J units can be supplied mounted on tape and reel.

* These parts will be available Q1 1991

IMS G178
High performance CMOS colour look-up table

inmos®

Designed to be compatible with IBM PS/2, VGA graphics systems



FEATURES

- Compatible with the RS170 video standard.
- RGB analogue output, configurable to 6 or 8 bit DAC operation.
- 256K or 16M possible colours.
- Composite sync and blank on all 3 channels.
- Pixel rates up to 80MHz.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Asynchronous access to all internal registers.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel
- Pixel word mask.
- Single +5V power supply.
- Low power dissipation, typically 1W at maximum pixel rate.
- 32 and 44 pin Plastic LCC package.
- Backward compatible with other members of IMS G17x look-up table family.

DESCRIPTION

The IMS G178 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 32 pin or 44 pin PLCC package.

The device is switchable between 6 or 8 bit DAC operation, so is capable of displaying 256 colours from a total of 262,144 colours in 6 bit mode, or from over 16 million colours in 8 bit mode.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite blank signals can be generated on all three outputs.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table

The IMS G178 is software-compatible with the IMS G171 and both software and pin-compatible with the IMS G176 products in 6 bit mode. It replaces TTL/ECL systems and thus gives reduced component cost, board area and power consumption.

5.1 Pin designations

5.1.1 Pixel Interface

Signal	Pin number 32	Pin number 44	I/O	Signal name	Description
PCLK	14	40	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address, sync and blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
P_0-P_7	6-13	32-39	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel Mask register and then used as the address into the colour look-up table.
$\overline{BLANK}$	20	7	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.
$\overline{SYNC}$	18	5	I	Sync	A low value on this input, when sampled, will cause an offset corresponding to 30% of the full-scale value to be removed from the DAC output. A high value, if sampled, will add the offset.

5.1.2 Analogue Interface

Signal	Pin number 32	Pin number 44	I/O	Signal name	Description
RED GREEN- BLUE	2 3 4	25 26 27	O O O		These signals are the outputs of the 6/8 bit DACs. Each DAC is composed of a number of current sources whose outputs are summed. The number of current sources active is controlled by the 6/8 bit binary value generated by the look-up table.
IREF	5	28	I	Reference current	The reference current drawn from AVDD via the IREF pin determines the current sourced by each of the current sources in the DACs.

5.1.3 Microprocessor interface

Signal	Pin number 32	Pin number 44	I/O	Signal name	Description
$\overline{WR}$	29	16	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	19	6	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	30,31	17,18	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
D_0–D_7	21–28	8–15	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G176 under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.
8/$\overline{6}$	15	2	I	8/6 mode select	When this pin is held high the part operates in 8 bit mode and when held low the part operates in 6 bit mode.

5.1.4 Power supply

Signal	Pin number 32	Pin number 44	Signal name	Description
				Digital and analogue power to the G178 is supplied on separate pins to provide maximum noise immunity.
VDD	17	4,21,22	Digital supply	Digital logic is supplied via VDD.
AVDD	32	20	Analogue supply	Analogue circuitry, including DACs and reference circuits, is supplied through the AVDD pin.
VSS	16	3	Ground	

5.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
				There is a single Address register within the IMS G178. This register can be accessed through either register select 0,0 or register select 1,1
0	0	8	Address (write mode)	Writing a value to address 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to address 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the colour look-up table addressed and then increments the Address register. A read from address 0,0 is identical to a read from 1,1.
0	1	24	Colour Value	The Colour Value register is internally a 24 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this address. When writing in 6 bit mode, only the least significant six bits (D_0–D_5) are used. When operating in 8 bit mode the full 8 bit word is used for reading and writing, with D_7 being the most significant bit. The sequence of data transfer in both modes is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operations of the IMS G176 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs (P_0–P_7). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed via that interface.

5.2 Device description

The IMS G178 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 x 24 bit words, three 8 bit high speed DACs, a microprocessor interface and a pixel word mask. In addition, the part can be configured, through the use of the $8/\overline{6}$ pin to operate in a restricted 6 bit mode and emulate the function of the IMS G171 and IMS G176. In this mode only 18 bits of the 24 bit colour table are used and the DACs are restricted to 6 bit resolution.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18/24 bit data word being output from the table. This data is partitioned as three fields of 6/8 bits, each field being applied to the inputs of one DAC.

Pixel rates of up to 80 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G178. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

An externally generated sync signal may also be supplied to the IMS G178 on the $\overline{\text{SYNC}}$ pin. This can be used to generate composite video sync on all three of the DAC outputs.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation, overlays and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

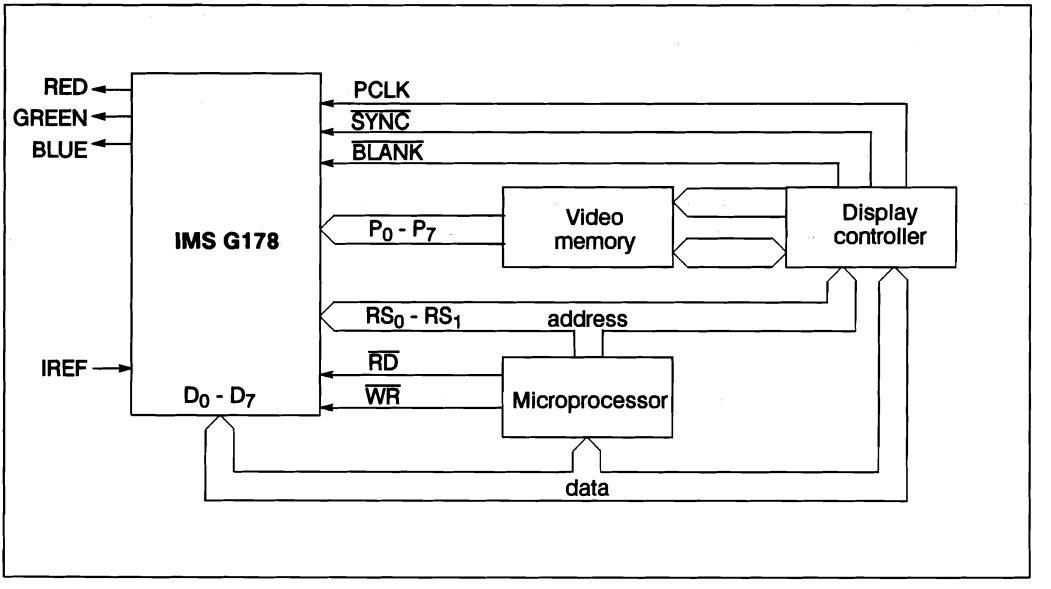


Figure 5.1 Typical IMS G178 application

5.2.1 Video path

P_0–P_7, $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ inputs are sampled on the rising edge of PCLK, their effect appears at the analogue outputs after three further rising edges of PCLK.

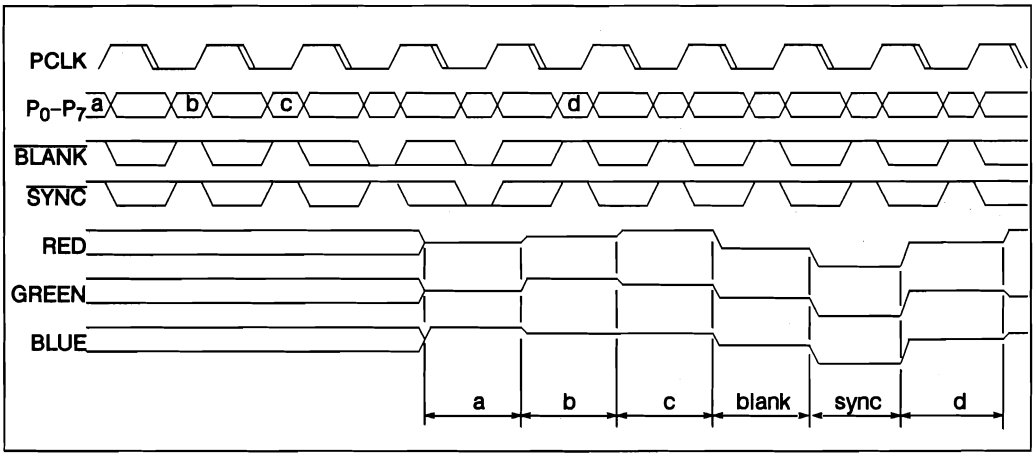


Figure 5.2

5.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 1.0 volt peak white amplitude (conforming to the RS170 standard) with an IREF of 9.07 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The $\overline{BLANK}$ and $\overline{SYNC}$ inputs to the IMS G178 act on all three of the analogue outputs. When the $\overline{BLANK}$ input is low a binary zero is applied to the inputs of the DACs. When $\overline{SYNC}$ is low the sync pedestal is removed from the DAC output.

The IMS G178 internally compensates for the switch between 6 and 8 bit operation; therfore the expressions for calculating the full white component and the sync component (if used) of the video signal in both modes are as follows:

$$V_{WHITE} = 2.058 \times IREF \times R_{EFFECTIVE} \quad \Big| \; V_{WHITE}$$

$$V_{SYNC} = 0.878 \times IREF \times R_{EFFECTIVE} \quad \Big| \; V_{SYNC}$$

5.2.3 Microprocessor Interface

Below are listed the three microprocessor interface registers within the IMS G178 and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address register.

Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous microprocessor interface access

Accesses to all registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G178. Data transfers between the look-up table and the Colour Value register and modifications to the Pixel Mask register are synchronized to PCLK by internal logic. This is done in the period between the microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is completely independent of the Address and Colour Value registers.

5.3 Electrical specifications

5.3.1 Absolute maximum ratings*

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	-1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	-55	125	°C	
TA	Temperature under bias	-40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	-15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VDD/AVDD	Positive supply voltage	4.75	5.0	5.25	volts	2,3,IMS G178-80/66
VDD/AVDD	Positive supply voltage	4.50	5.0	5.50	volts	2,3,IMS G178-50/40
GND	VSS		0		volts	
VIH	Input logic '1' voltage	2.0		VDD+0.5	volts	3
VIL	Input logic '0' voltage	−0.5		0.8	volts	4
TA	Ambient operating temperature	0		70	°C	5
IREF	Reference current	−7.0		−10	mA	6

Notes

1 All voltages are with respect to GND unless specified otherwise.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 These voltage ranges apply equally for AVDD and VDD. (N.B VDD must = AVDD)

4 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

5 With a 400 linear ft/min transverse air flow.

6 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
IDD	Average power supply current		265	mA	4, IMS G178-80
IDD	Average power supply current		240	mA	4, IMS G178-66
IDD	Average power supply current		220	mA	4, IMS G178-50
IDD	Average power supply current		210	mA	4, IMS G178-40
VREF	Voltage at IREF input	VDD−3	VDD	volts	5
IIN	Digital input current (any input)		±10	μA	6,7
IOZ	Off state digital output current		±50	μA	6,8
VOH	Output logic '1'	2.4		volts	IO = −5mA
VOL	Output logic '0'		0.4	volts	IO = 5mA

Notes

1 All voltages are with respect to GND unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). IDD is dependent on digital output loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 These voltage ranges apply equally for AVDD and VDD. (N.B. VDD must = AVDD)

6 VDD = max, VSS $\leq$ VIN $\leq$ VDD.

7 On digital inputs, pins 6-14, 19, 20, 29-31 (for 32 pin PLCC). Pins 32-40, 6, 7, 16-18 (for 44 pin PLCC).

8 On digital input/output. Pins 21-28 (for 32 pin PLCC), Pins 8-15 (for 44 pin PLCC).

5.3.3 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1,2)
	Resolution	6		8	bits	depending on mode
VO(max)	Output voltage			1.5	volts	IO≤IO(max)
IO(max)	Output current	27.5	29.4	31.3	mA	VO≤1V
	Full scale error			±5	%	3,4
	SYNC pedestal error			±10	%	3
	DAC to DAC correlation error			±2.5	%	3,5
	Integral linearity error			±0.5	LSB	3,6 (6 bit mode)
	Integral linearity error			±1	LSB	3,6 (8 bit mode)
	Rise time (10% to 90%)			6	ns	3,7, IMS G178-66/80
	Rise time (10% to 90%)			8	ns	3,7, IMS G178-40/50
	Full scale settling time			12.5	ns	3,7,8,9, IMS G178-80
	Full scale settling time			15.3	ns	3,7,8,9, IMS G178-66
	Full scale settling time			20	ns	3,7,8,9, IMS G178-50
	Full scale settling time			25	ns	3,7,8,9, IMS G178-40
	Glitch energy		75		pVsec	3,7,9

Notes

1 All voltages are with respect to GND unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = -9.07mA.

4 Full scale error from the value predicted by the design equations (SYNC off).

5 About the mid point of the distribution of the three DACs measured at full scale deflection (SYNC off).

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed (SYNC off).

7 Load = 37.5Ω + 30pF with IREF = -9.07mA.

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

5.3.4 AC test conditions

Input pulse levels	GND to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure 5.3

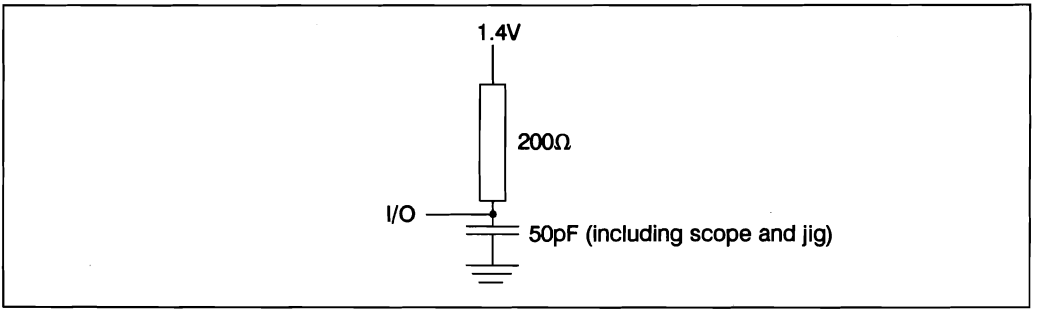


Figure 5.3 Digital output load

5.3.5 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable D_0-D_7

4 BLANK $\leq$ VIL(max) to disable RED, GREEN and BLUE.

5.3.6 Video operation (Figure 5.4)

Symbol	Parameter	All Max.	40 MHz Min.	50 MHz Min.	66 MHz Min.	80 MHz Min.	Units	Notes
tCHCH	PCLK period	10000	25	20	15.1	12.5	ns	
ΔtCHCH	PCLK jitter	±2.5					%	1
tCLCH	PCLK width low	10000	9	6	5	5	ns	
tCHCL	PCLK width high	10000	7	6	5	5	ns	
tPVCH	Pixel address set-up time		5	4	3	3	ns	2
tCHPX	Pixel address hold time		5	4	3	3	ns	2
tBVCH	$\overline{\text{BLANK}}$ setup time		5	4	3	3	ns	
tCHBX	$\overline{\text{BLANK}}$ hold time		5	4	3	3	ns	
tSVCH	$\overline{\text{SYNC}}$ setup time		5	4	3	3	ns	
tCHSX	$\overline{\text{SYNC}}$ hold time		5	4	3	3	ns	
tCHAV	PCLK to valid DAC output	30	5	5	5	5	ns	3
ΔtCHAV	Differential output delay	2					ns	4
	Pixel clock transition time	50					ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (tCHCH) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

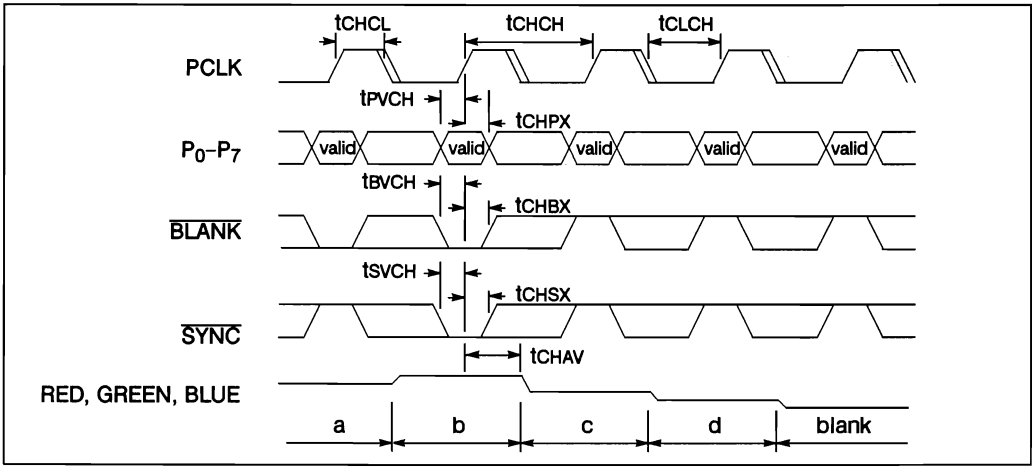


Figure 5.4 Video operation

5.3.7 Microprocessor interface operation

Symbol	Parameter	All	40 MHz	50 MHz	66 MHz	80 MHz	Units	Notes
		Max.	Min.	Min.	Min.	Min.		
tWLWH	$\overline{WR}$ pulse width low		50	50	50	50	ns	
tRLRH	$\overline{RD}$ pulse width low		50	50	50	50	ns	
tSVWL	Register select setup time		15	10	10	10	ns	
tSVRL	Register select setup time		15	10	10	10	ns	
tWLSX	Register select hold time		15	10	10	10	ns	
tRLSX	Register select hold time		15	10	10	10	ns	
tDVWH	Write data setup time		15	10	10	10	ns	
tWHDX	Write data hold time		15	10	10	10	ns	
tRLQX	Output turn-on delay		0	0	0	0	ns	
tRLQV	Read enable access time	40					ns	
tRHQX	Output hold time		0	0	0	0	ns	
tRHQZ	Output turn-off delay	20					ns	1
tWHWL1	Successive write interval							
tWHRL1	Write followed by read interval							
tRHRL1	Successive read interval							
tRHWL1	Read followed by write interval		4xtCHCH +30ns				ns	2
tWHWL2	Write after colour write							
tWHRL2	Read after colour write							
tRHWL2	Write after colour read							
tRHRL2	Read after colour read		6xtCHCH +40ns				ns	2
tWHRL3	Read after read address write							
tCYC	Write/Read cycle time		6xtCHCH +40ns				ns	2,3
	Write/Read enable transition time	50					ns	

Notes

1 Measured ±200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the microprocessor port are internally synchronised to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the microprocessor port being specified in terms of pixel clock periods.

In the case of the IMS G178 the minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is $6 \times tCHCH + 40ns$.

For example, in the case of a 25MHz system the pixel clock period (tCHCH) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

$$6 \times 40ns + 40ns = 280ns$$

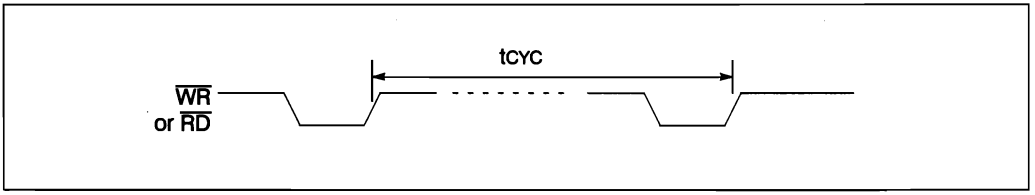


Figure 5.5 Write/Read cycle time

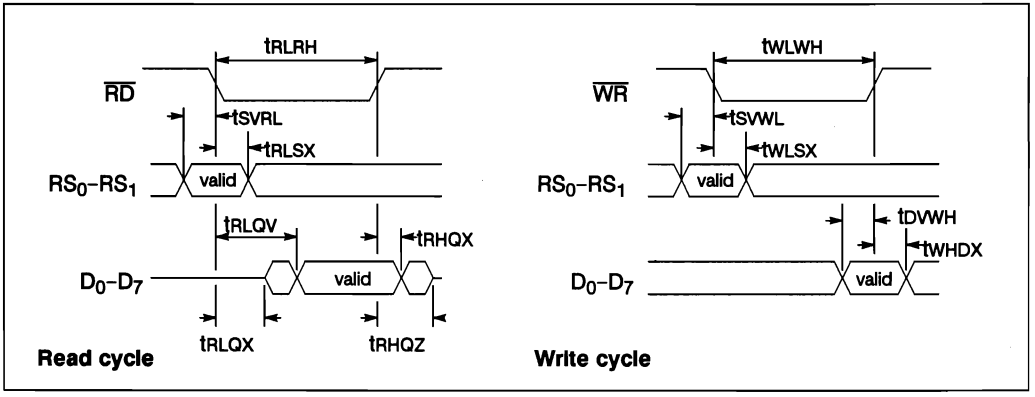


Figure 5.6 Basic read/write cycles

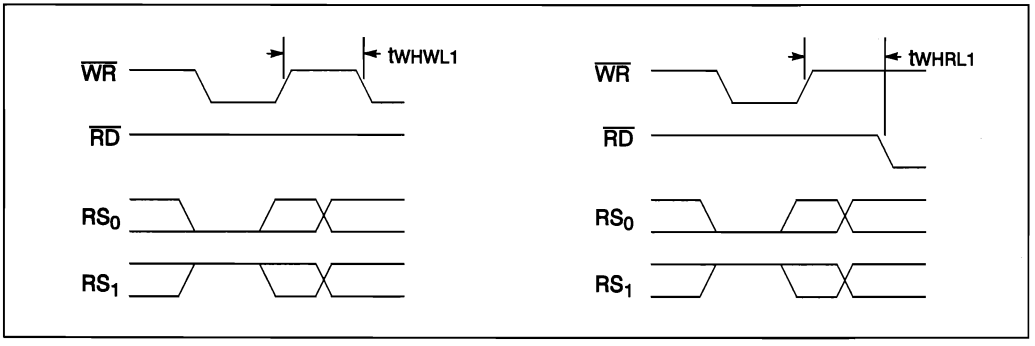


Figure 5.7 Write to pixel mask register followed by any access

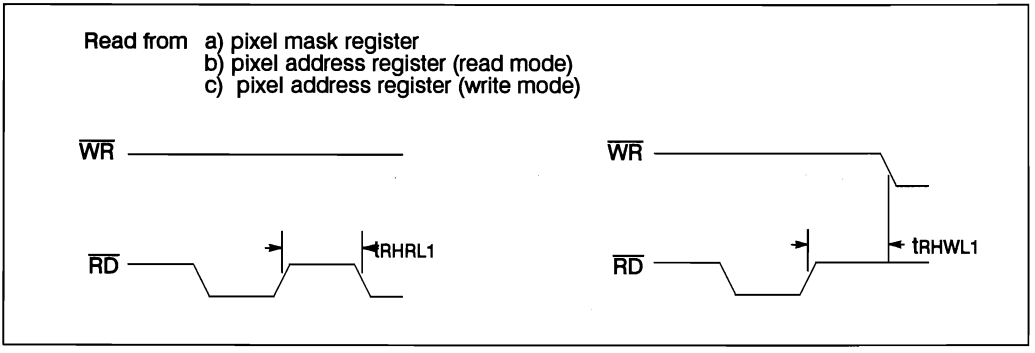


Figure 5.8 Read from register followed by any access

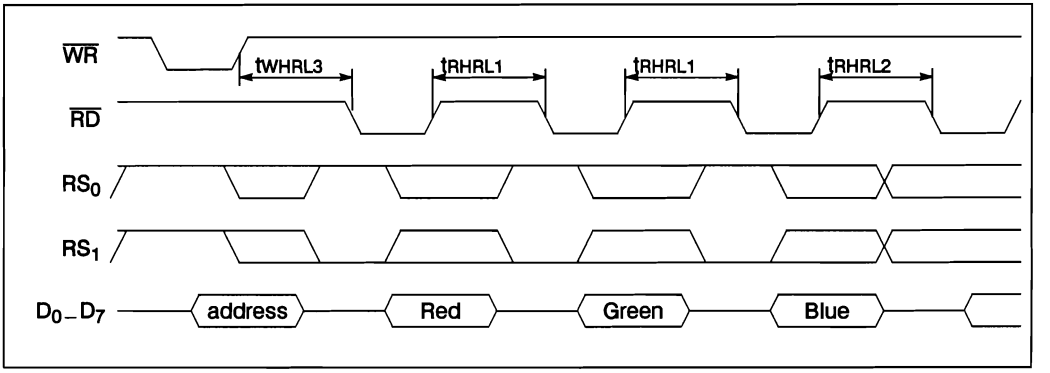


Figure 5.9 Colour value read followed by any read

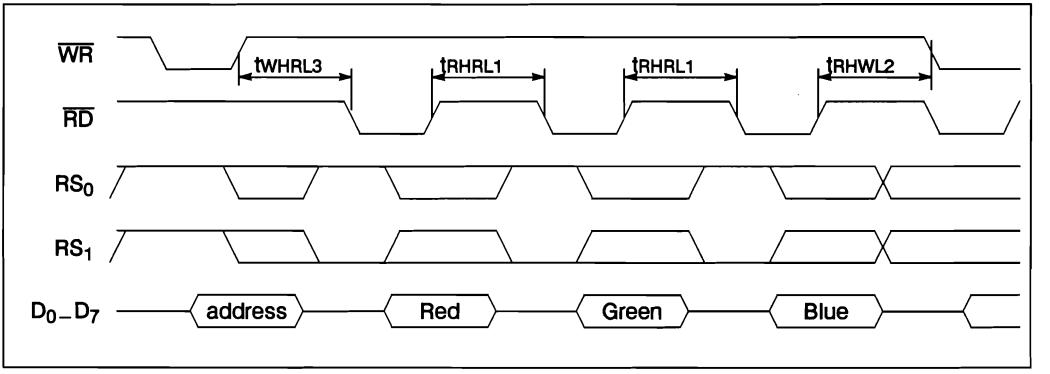


Figure 5.10 Colour value read followed by any write

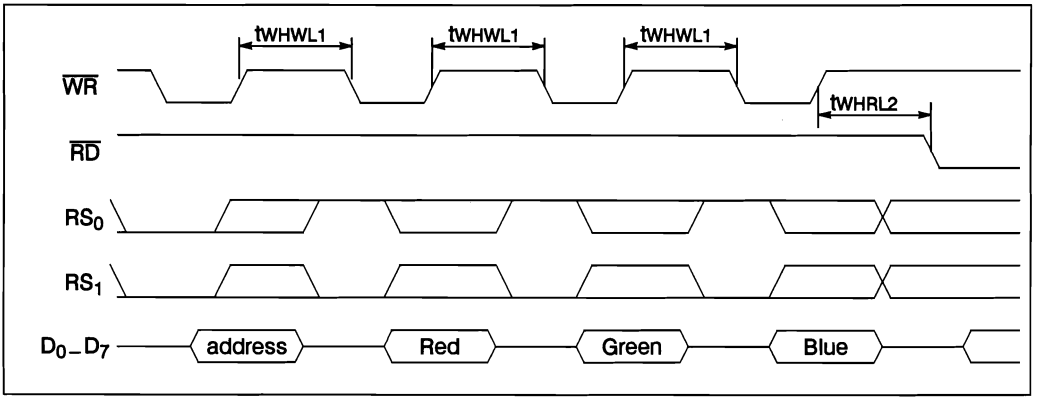


Figure 5.11 Colour value write followed by any read

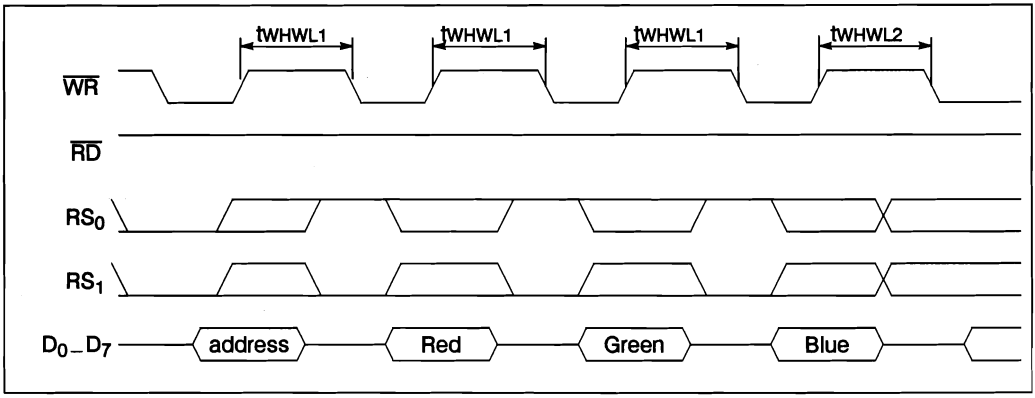


Figure 5.12 Colour value write followed by any write

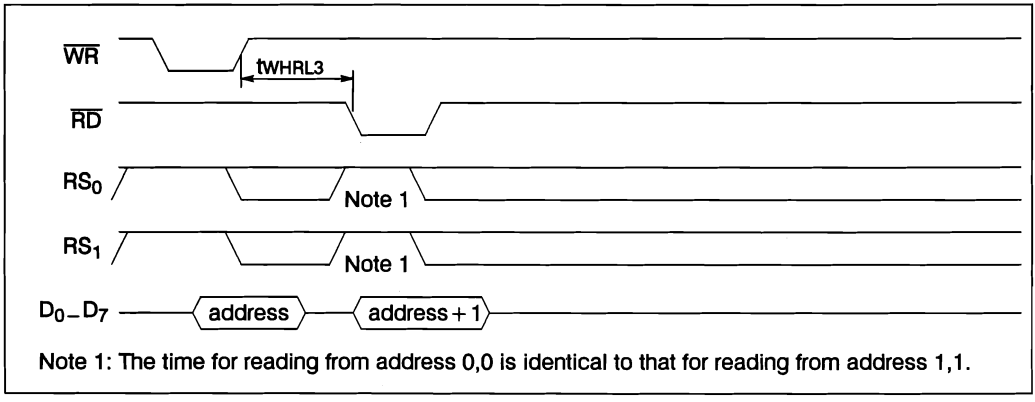


Figure 5.13 Write and read back address register (read mode)

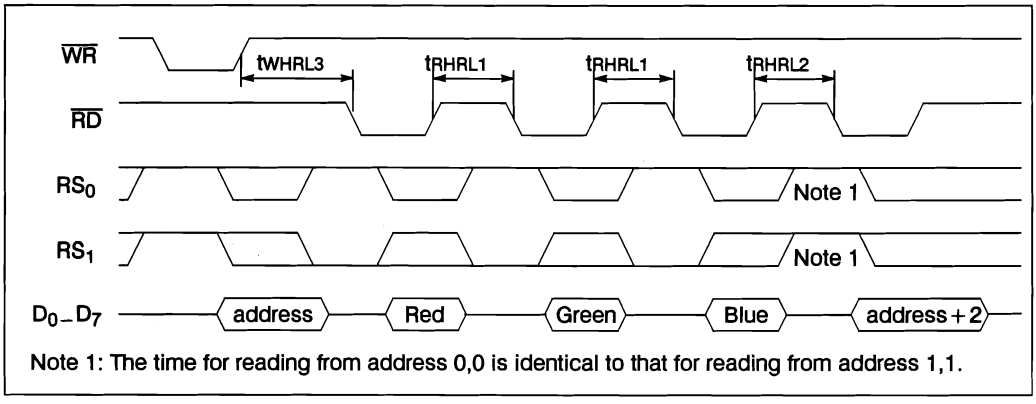


Figure 5.14 Read colour value then the address register (read mode)

5.4 Designing with the IMS G178

5.4.1 Board layout - general

The IMS G178 is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G178. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

5.4.2 Power supply decoupling

The DACs in the IMS G178 are referenced to the positive power supply, so are fairly insensitive to ground supply noise. To minimise the coupling of digital noise from the digital sections of the IMS G178, independent analogue and digital +5V supplies (AVDD and VDD respectively) are provided.

It is further recommended that a high-frequency capacitor of around 100nF (preferably a chip capacitor) should be placed as close as possible to the package between these supplies and VSS. A large tantalum capacitor (between 22μF and 47μF) should also be placed in parallel with this high-frequency capacitor.

In cases where the main digital supply on the graphics board is too noisy to achieve a satisfactory analogue output from the G178 DACs, a separate decoupled supply may be created just for the G178. An inductor may be used to decouple this supply (connected to AVDD and VDD) to the main board supply. This forms a low pass filter rejecting high frequency noise components present on the main board supply (figure 5.18).

5.4.3 Analogue output - line driving

The DACs in the IMS G178 are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G178 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good fidelity, RF techniques should be observed. The PCB trace connecting the IMS G178 to the off-board connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus a double terminated DAC output will rise faster than any singly terminated output.

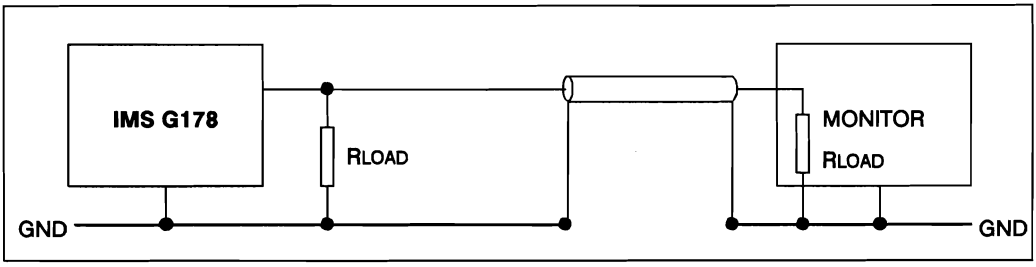


Figure 5.15 Double termination

Buffered signal

If the IMS G178 is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

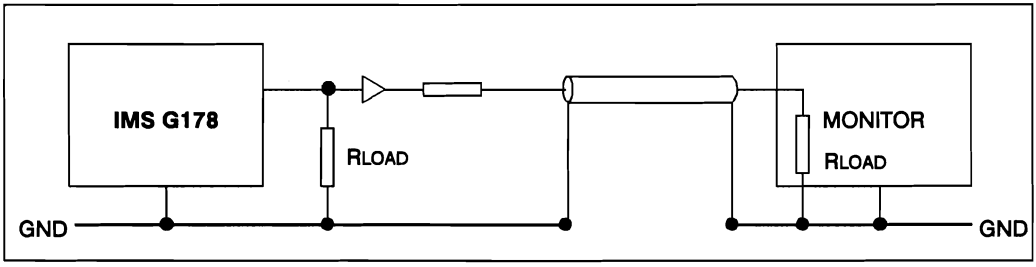


Figure 5.16 Buffered signal

5.4.4 Analogue output - protection

CMOS devices are susceptible to damage from from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G178 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However, if the analogue outputs of the IMS G178 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection diodes (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figure NO TAG).

5.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G178 and the input to the IMS G178 have a low impedance source and are terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of the IMS G178. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a value around 100Ω will be required. Because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

5.4.6 Current reference - design

To ensure that the output current of the DACs is predictable and stable with temperature variations an active current reference is recommended. Figure 5.17 shows four designs of current reference.

Figure 5.17d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 5.17a-c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuit 5.17b and c the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 5.17c).

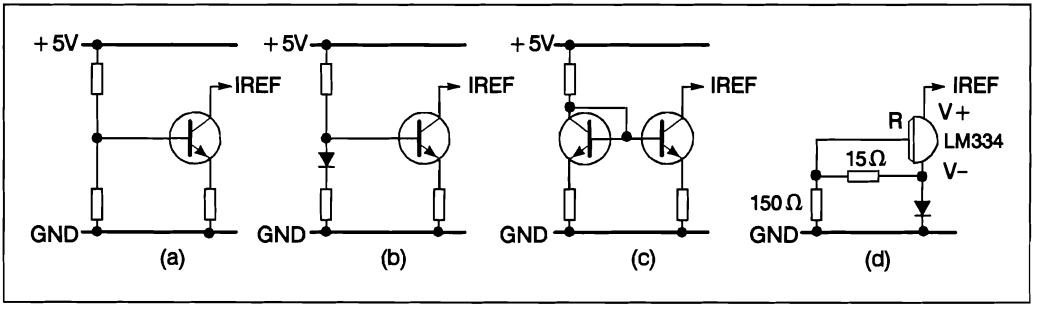


Figure 5.17

5.4.7 Current reference - decoupling

The DACs in the IMS G178 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

As long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capacitor need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high-frequency capacitor of 100nF should be used to couple the IREF input to AVDD. This will enable the current reference to track both low and high frequency variations in the supply.

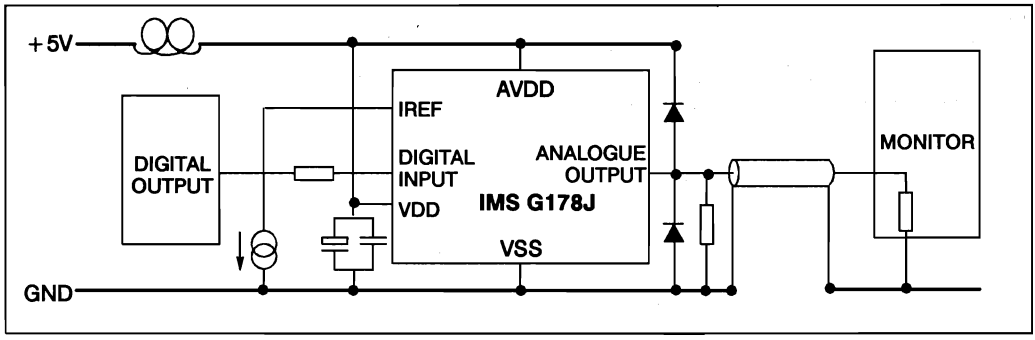


Figure 5.18 Suggested circuit using PLCC package

5.5 Package specifications

5.5.1 32 pin plastic leaded-chip-carrier package

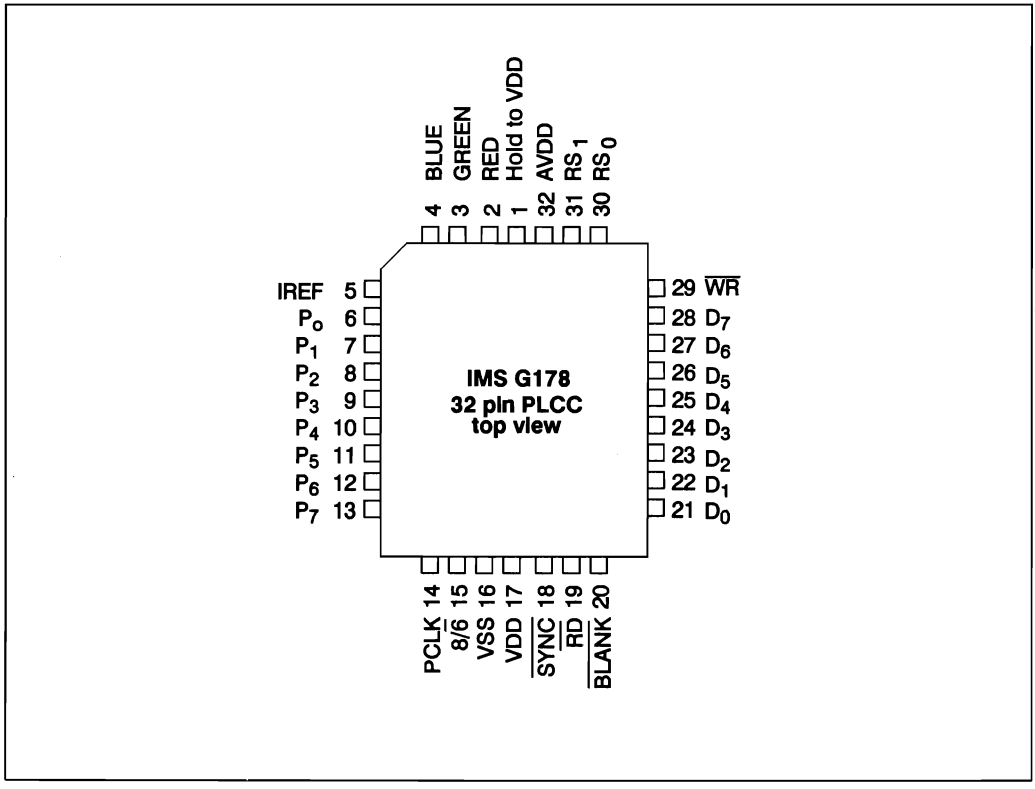


Figure 5.19 IMS G178 32 pin PLCC J-bend package pinout

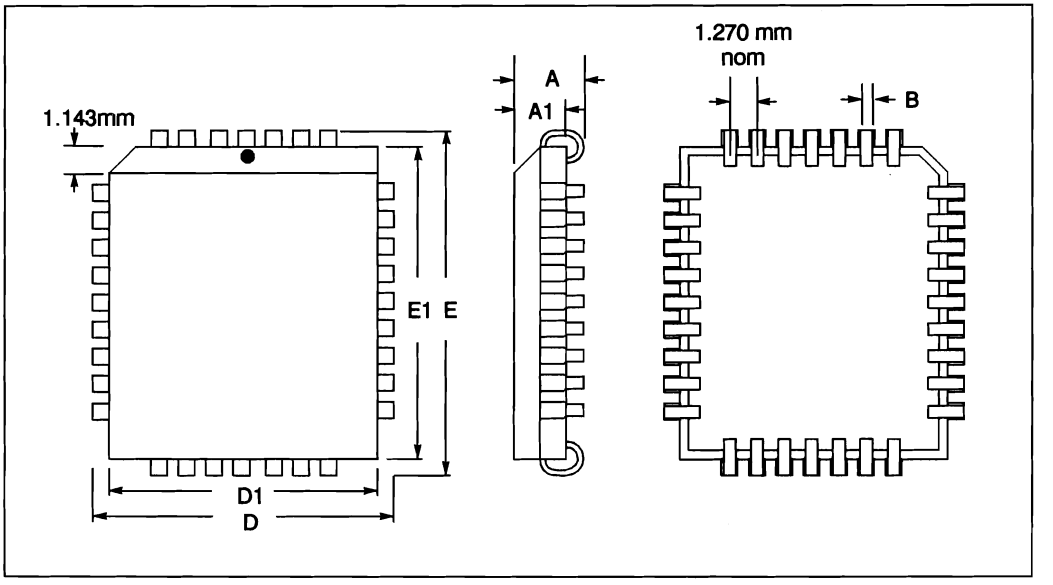


Figure 5.20 32 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	3.120	3.560	0.123	0.140	
A1	2.160		0.085		Nominal
B	0.432		0.017		Nominal
D	12.323	12.577	0.485	0.495	
D1	11.400	11.506	0.449	0.453	
E	14.859	15.113	0.585	0.595	
E1	13.940	14.046	0.549	0.553	

Table 5.1 32 pin PLCC J-bend package dimensions

5.5.2 44 pin plastic leaded chip carrier package

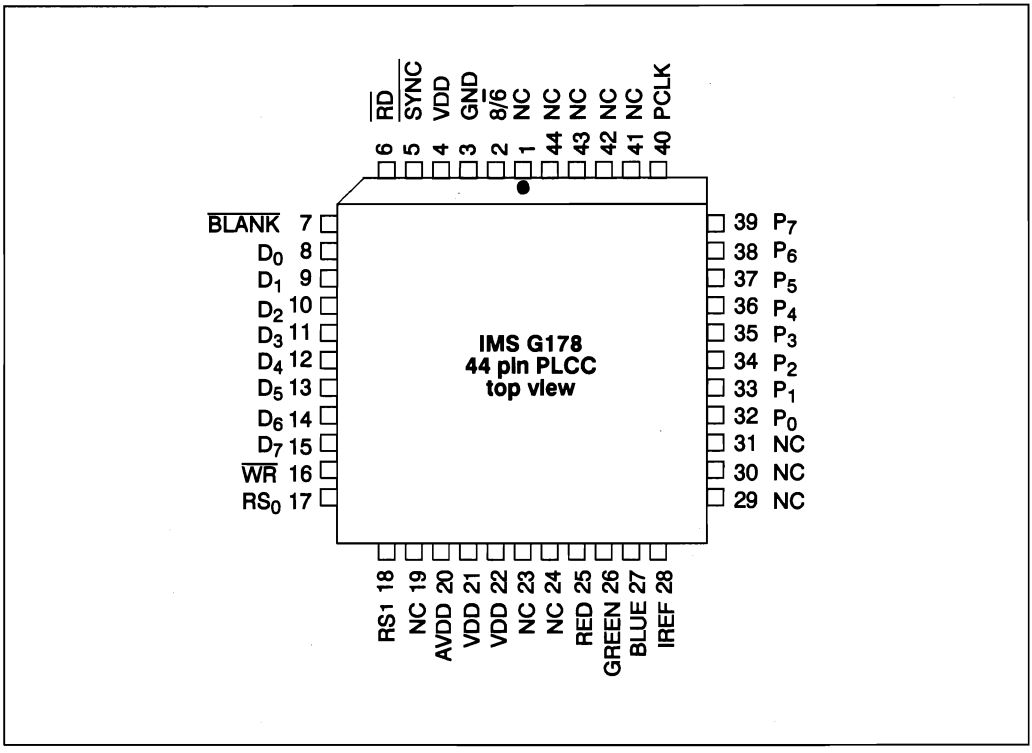


Figure 5.21 IMS G178 44 pin PLCC J-bend package pinout

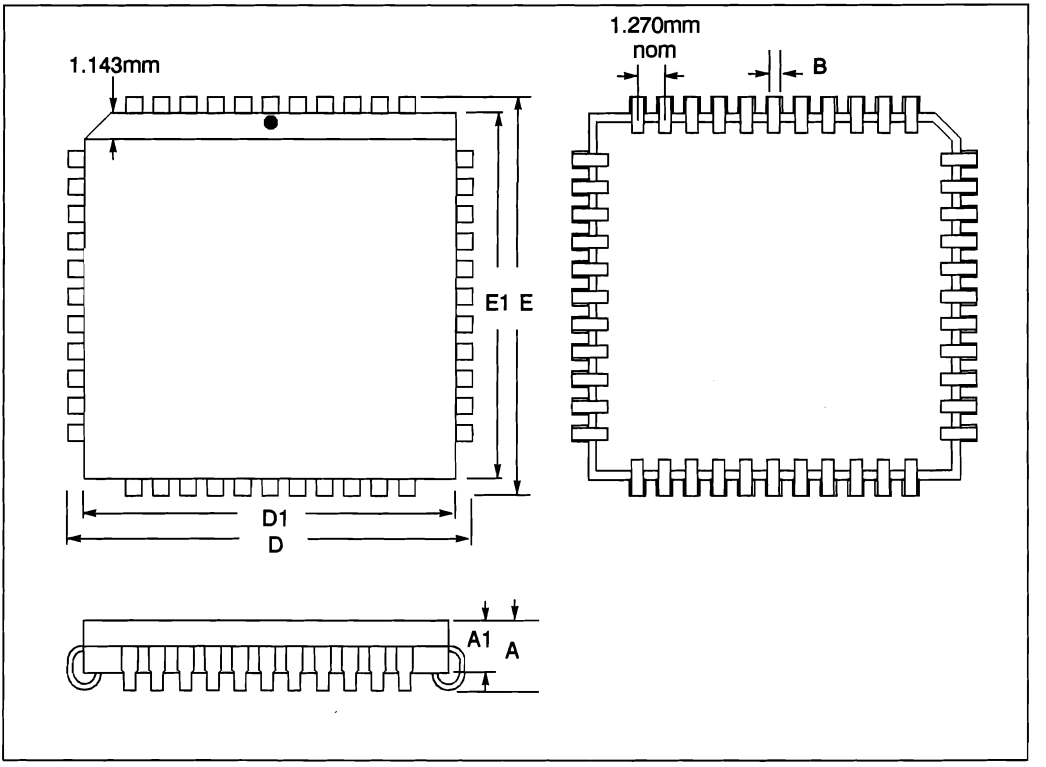


Figure 5.22 IMS G178 44 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	4.191	4.572	0.165	0.180	
A1	3.683	4.064	0.145	0.160	
B	0.457		0.018		
D	17.399	17.653	0.685	0.695	
D1	16.510	16.662	0.650	0.656	
E	17.399	17.653	0.685	0.695	
E1	16.510	16.662	0.650	0.656	

Table 5.2 44 pin PLCC J-bend package dimensions

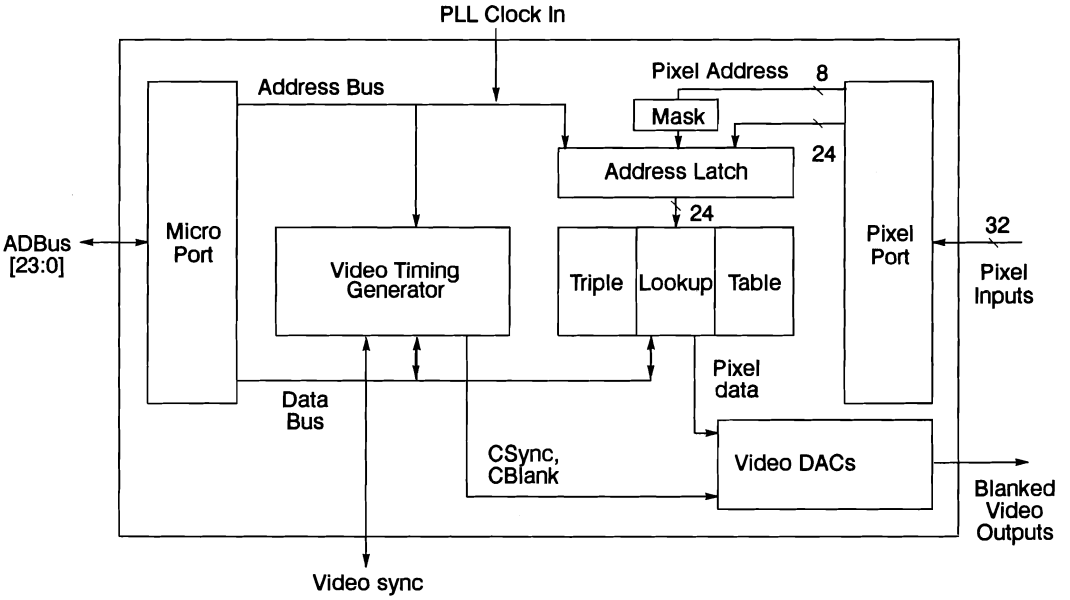
5.5.3 Ordering information

Device	Clock rate	Package	Part number
IMS G178	40 MHz	32 Plastic LCC	IMS G178J-40S
IMS G178	50 MHz	32 Plastic LCC	IMS G178J-50S
IMS G178	66 MHz	32 Plastic LCC	IMS G178J-66S
IMS G178	80 MHz	32 Plastic LCC	IMS G178J-80S
IMS G178	40 MHz	44 Plastic LCC	IMS G178J-40Z
IMS G178	50 MHz	44 Plastic LCC	IMS G178J-50Z
IMS G178	66 MHz	44 Plastic LCC	IMS G178J-66Z
IMS G178	80 MHz	44 Plastic LCC	IMS G178J-80Z

Note: IMS G178J units can be supplied mounted on tape and reel.

IMS G300B
colour video controller

Preliminary data



FEATURES

Video rates up to 110 MHz
Software configurable video timing generator
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

Variable multiplexed Pixel input
1, 2, 4, 8 and 24 bit pixels
On chip triple lookup table
Triple high speed 8 bit video DACs
CCIR and EIA 343-A compatible
Full colour mode with hardware gamma translation

General purpose Video RAM support
Synchronous VRAM Data Transfer strobing
Video RAM Row address auto-increment
Screen width independent of VRAM architecture
On-chip phase-locked loop (PLL)
All external signals and clocks at 1/4 video rate

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

6.1 Introduction

The IMS G300 is a dedicated support chip which provides all necessary functions for controlling real time operation of a raster scan video system, using dual ported video DRAMs. The facilities provided are designed to isolate the host processor from the constraints of the real time system without in any way interfering with the ability of the processor to specify and manipulate screen data.

The device consists of a programmable video timing generator with screen refresh and auto line increment capability, a triple 256 location by 8 bit lookup table (LUT), a triple 8 bit video DAC and an on chip phase-locked loop (PLL); see figure 6.1.

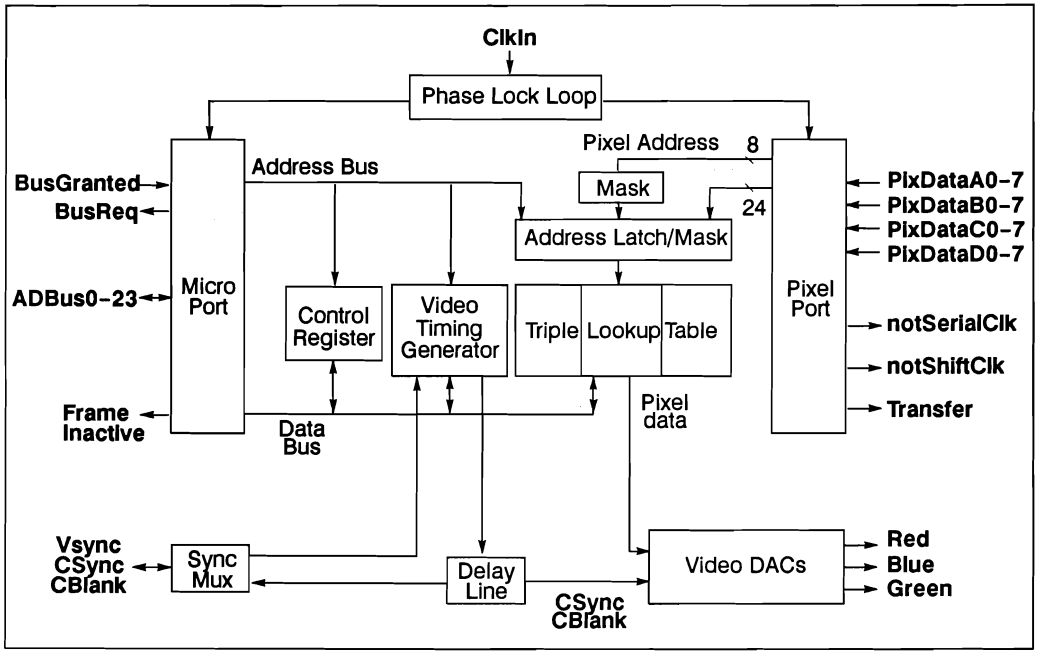


Figure 6.1 IMS G300 Block Diagram

6.1.1 Clocks

Use of the phase-locked loop allows the part to be driven from a low speed clock in the 5MHz to 10MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL.

6.1.2 Video timing

The video timing generator is a programmable finite state machine which is programmed by loading a number of screen description parameters. It can be configured to free run, providing composite or separate sync, or to lock onto an external synchronising source which may be another IMS G300, giving the potential for multiple, synchronous video systems. In either mode, it supplies composite blank and can supply tesselated or plain composite sync to the video DACs. The timing generator runs at one quarter of the video dot rate and the screen parameters are defined in terms of its resolution. Thus the screen is defined in multiples of four pixels.

6.1.3 Screen management

Video RAM support is provided by a screen refresh mechanism which performs a DMA to the video RAM and which allows seamless mid-line update of the screen. The video RAM shift register can be made to

behave as though it is infinitely long and the flow of pixels onto the screen is controlled by starting and stopping the pixel shift clock at the appropriate times (a true serial clock output is also provided for system synchronisation). This method of control divorces the screen line length from dependence on the video RAM shift register length, allowing for very long display lines without extra multiplexing and for efficient use of memory irrespective of screen dimensions.

6.1.4 Pixel port

The pixel port is 32 bits wide and has a number of operating modes, which are selectable in software.

In pseudo colour mode (mode 1), the 32 bit word can be interpreted as consisting of one, two, four or eight bit pixels. These are loaded at the relevant multiplex ratio and accelerated to the full dot rate before addressing the LUT. The 24 bits of pixel data thus accessed are then sent to the video DACs for display.

In full colour mode (mode 2), the top byte of the input word is ignored and the remaining three bytes are used as separate addresses into the triple LUT. No acceleration takes place before the data is sent to the LUT.

Mode 2 is usable only when an external dot-rate clock is supplied, mode 1 can also be used with the phase-locked loop.

6.1.5 Video DACs

The triple video DAC has 8 bit resolution at the full video rate and produces blanked video signals. It is possible to select various styles of analogue output to conform with generally approved monitor and broadcast television output levels and timings, including EIA-343 and CCIR.

6.1.6 Programming port

The IMS G300 has a memory mapped architecture which enables fast configuration and colour cycling through the use of block move or some other simple memory write cycle. Its micro-port appears as a block of memory (occupying 1/2Kword of address space) with the additional capability of operating in byte-wide or word-wide (24-bit) modes.

6.1.7 System Operation

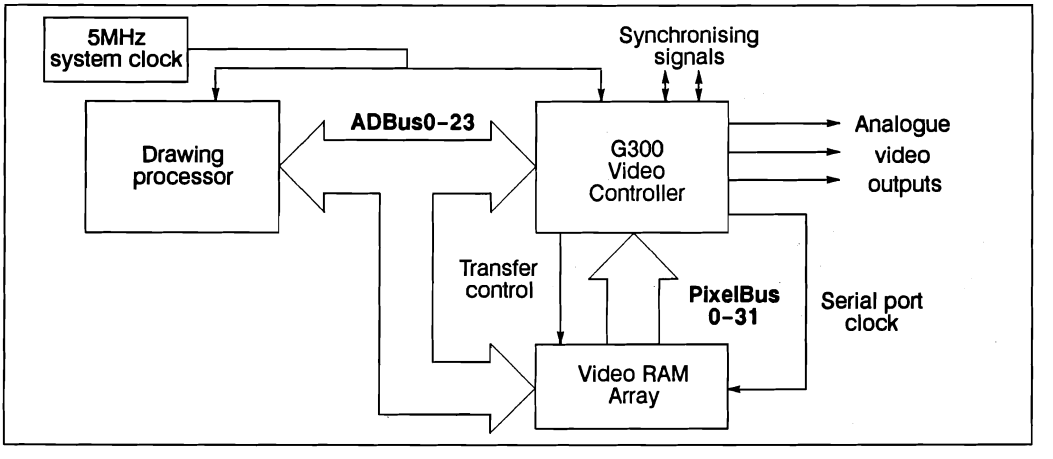


Figure 6.2 IMS G300 operating in a simple graphics system

Figure 6.2 shows how the IMS G300 would fit into a typical single-bitmap display system. The clock is sourced from a 5MHz crystal and the video data is being streamed to the screen at the full video rate of up to 110MHz. The video RAM array is directly accessed by the drawing processor and screen management is performed by the G300 on a DMA basis. All external digital signals and clocks are running at one quarter of the video rate.

6.2 Pin function reference guide

6.2.1 Micro port

Pin name	I/O	Page No.	Comments
FrameInactive	O	117	Timing signal which is high whenever the VTG is in Frame Flyback.
BusReq **BusGranted**	O I	114	DMA signals which, along with **Transfer**, supply the timing information to synchronously refresh the video ram shift registers.
ReadnotWrite **notCS**	I I	112	These signals provide all the timing information for accesses as well as defining access type.
ADBus0-23	I/O	112	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied to **ADBus2-11**. A byte-wide mode is available; the port is also used to drive out the 22-bit VRAM transfer address on **ADBus2-23.**

6.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk **notShiftClk**	O O	114	**notSerialClk** runs at one quarter the video frequency, **notShiftClk** varies its frequency depending on the bits per pixel required. Both of these clocks must be buffered.
Transfer	O	114	**Transfer** refreshes the video ram shift register synchronised to **notSerialClk**
CBlank	I/O	108	**CBlank** is a bidirectional blanking pin. Direction is soft selectable via control bit 16.
PixDataA0-7 **PixDataB0-7** **PixDataC0-7** **PixDataD0-7**	I I I I	118	The four pixel address bytes are used in the order A, B, C, D. In mode 2 **PixDataD0-7** is not used and RGB maps to ABC.

6.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	105	Active high, must be held active with clocks running for at least six cycles of **notSerialClk.**

6.2.4 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus **CapMinus**	N/A	126	Phase locked loop decoupling pins, also used to select external dot rate clock source by connecting **CapPlus** to **CapMinus**.
ClkIn	I	126	Clock input for both PLL and times one operation.

6.2.5 Video signals

Pin name	I/O	Page No.	Comments
Red **Green** **Blue**	O O O	122	Blanked video outputs. Drive into doubly terminated 75Ω load.
Iref	I	122	Video DAC reference current.
VSync **CorHSync**	I/O I/O	107	These pins can be used as outputs to supply various software-selectable sync signals or as inputs to lock the device to a system. They are both active low.

6.2.6 Supplies

Pin name	I/O	Page No.	Comments
AVDD	N/A	124	**AVDD** supplies analogue portions of chip.
VDD	N/A	124	**VDD** supplies digital portions of chip.
Ground	N/A		

6.3 Register function reference guide

Register	Address	Page No.	Comments
Boot Location	#X1A0	111	Startup location to which must be written the clock multiplication factor and the clock source (PLL or dot rate).
Null	#1B0	113	Un-decoded location used for resetting byte mode state.
Top of Screen	#X180	113	Read/write register giving ability to reprogram the top of screen pointer at any time.
Control Register	#X160	93	Read/write control register. Read/write accessible at all times, contains all configuration information. Used to start and stop timing generator.
Mask Register	#X140	118	Read/write mask register. Read/write accessible at all times, masks each pixel address byte.
Datapath Registers	#X121 to #X12C	101	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Colour Palette	#X00 to #XFF	118	256 locations of 24 bit colours read/write accessible at all times, programmed via micro port. The values stored in the colour palette relate to the DACs as follows: lowest byte = RED, next byte = GREEN, highest byte = BLUE.

All other addresses in the range are reserved and must not be written to.

Note: #X = Hexadecimal address.

6.4 The control register and boot location reference guide

The bit pattern written to the control register determines the operating mode of the part. The function of each bit is given in table 6.1.

Bit	Function	Comments
23	Blank Function switch	1 = Undelayed ClkDisable at pad 0 = Delayed CBlank at pad
22	Reserved	Write zero
21	Interlace Standard	1 = CCIR Interlace format 0 = EIA Interlace format
20-19	Address step control	Sets size of VRAM transfer address increment
18-17	Bits per pixel	Sets Pixel port to required pixel depth
16	Blank I/O	1 = CBlank pin is output 0 = CBlank pin is input
15	Turn off blanking	1 = blanking disabled for test 0 = blanking enabled
14	Turn Off DMA	1 = No video RAM management 0 = DMA VRAM update operational
13	Reserved	Write zero
12	Black level	Selects blanking level 0 = Blank = Black level
11-9	Delay value	Delays Sync and Blank by 0 to 7 VTG clock cycles
8	Pixel port mode	0 = mode1, 1 = mode2
7	Micro port mode	0 = word mode, 1 = Byte mode
6	Reserved	Write zero
5	Analogue video format	1 = video only 0 = video and sync composite
4	Digital sync format	0 = mixed sync, 1 = separate sync
3	Frame flyback pattern	1 = plain synchronising waveform 0 = tesselated synchronising waveform
2	Device operating mode	0 = master mode, 1 = slave mode
1	Screen format	0 = non-interlaced, 1 = interlaced
0	Enable VTG	0 = VTG disabled, 1 = VTG running

Table 6.1 Control register bit allocations

Boot Address	Bit Allocation
#X1A0	**ADbus6-23** = Write zero **ADBus5** = Clock source select 1 = PLL mode, 0 = external clock mode **ADBus0-4** = Binary coded PLL multiplication factor (when in external clock mode, load zero)

Table 6.2 Boot location bit allocations

6.5 Micro port timing reference guide

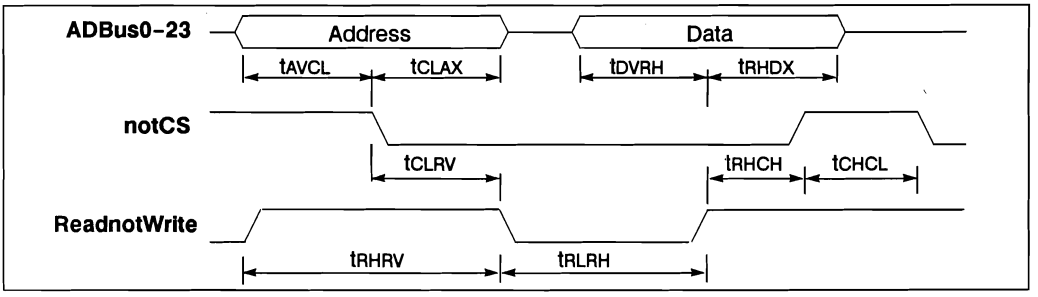


Figure 6.3 Micro port write cycle

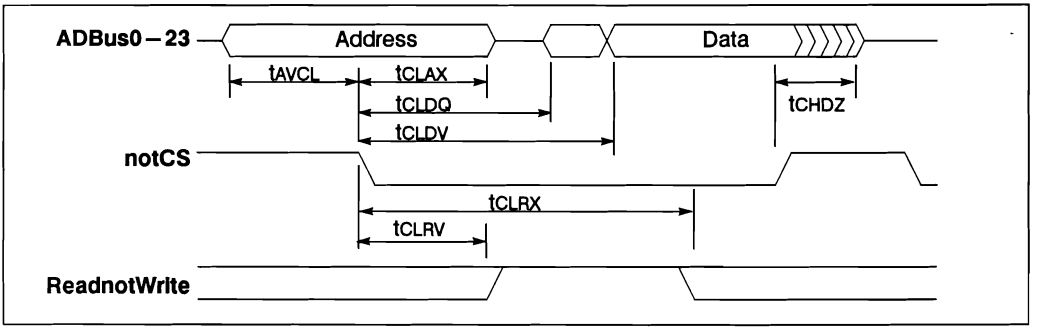


Figure 6.4 Micro port read cycle

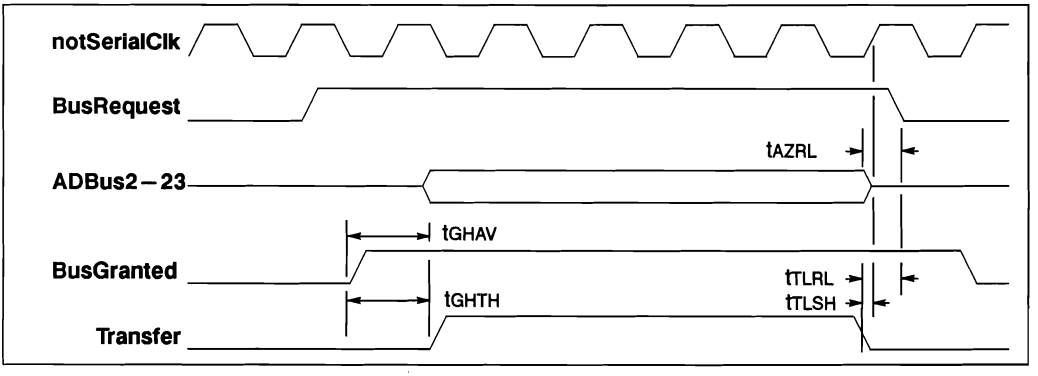


Figure 6.5 Micro port DMA and data transfer timings

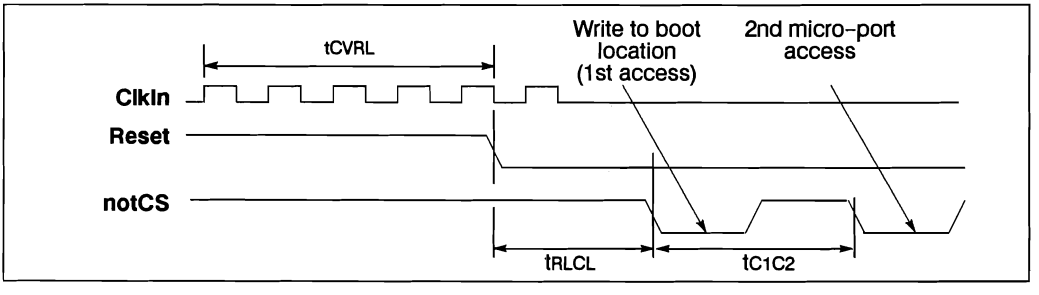


Figure 6.6 Reset timings

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	10		ns
tCLAX	Address hold time	20		ns
tCLRV			0.5	periods SClk
tCHCL		1+20ns		periods SClk
tDVRH	Data setup time	10		ns
tRHDX	Data hold time	20		ns
tRHCH				*
tRLRH		4		periods SClk
tRHRV		1+20ns		periods SClk
tCLCL	Cycle time	7		periods SClk
Where SClk is the period of **notSerialClk** **Note:** These figures are not characterised and are subject to change				
RHCH = RHRV−CHCL−CLRV				

Table 6.3 Micro port write cycle parameters

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	10		ns
tCLAX	Address hold time	20		ns
tCLDQ	Time to bus driven	1.5		periods SClk
tCLDV	Data access time		5SClk+20	ns
tCLRV			0.5	periods SClk
tCLRX		3.5+20ns		periods SClk
tCHDZ	Data turn off delay		30	ns
tCLCL	Cycle time	7		periods SClk
where SClk is the period of **notSerialClk** **Note:** These figures are not characterised and are subject to change				

Table 6.4 Micro port read cycle parameters

Symbol	Description	Min.	Max.	Unit
tGHAV	**busGranted** high to address valid		3*SClk+30	ns
tAZRL	**ADBus** tristate to **busRequest low**	0		ns
tGHTH	**busGranted** high to **Transfer** high		25	ns
tTLRL	**Transfer** low to **Bus Request low**	1	2	SClk
tTLSH	**Transfer** low to **notSerialClk** high	-10	3	ns
Note: These figures are not characterised and are subject to change				

Table 6.5 Micro port DMA and transfer timing parameters

Symbol	Description	Min.	Max.	Unit
tRLCL	**Reset** low to **notCS** low	100		ns
tCVRL	**ClkIn** valid to **reset** low			ns
tC1C2	Time between 1st and 2nd access	20		µs

Table 6.6 Reset timing parameters

6.6 Pixel port timing reference guide

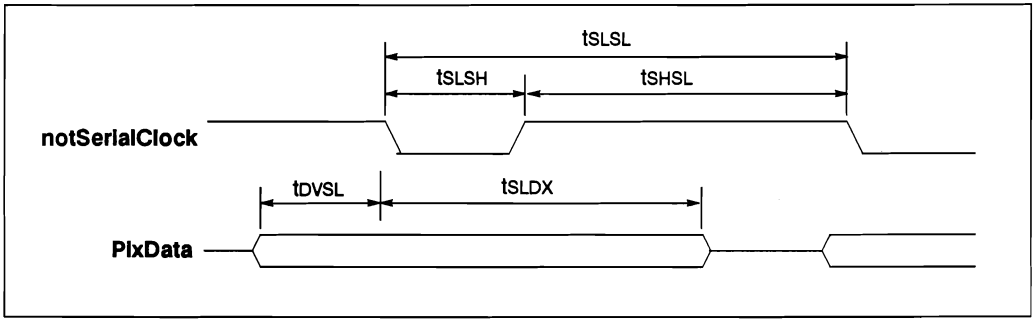


Figure 6.7 Pixel port signals in mode 1

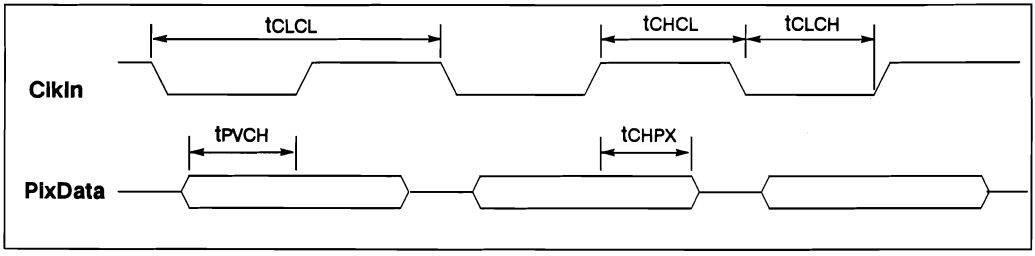


Figure 6.8 Pixel port signals in mode 2

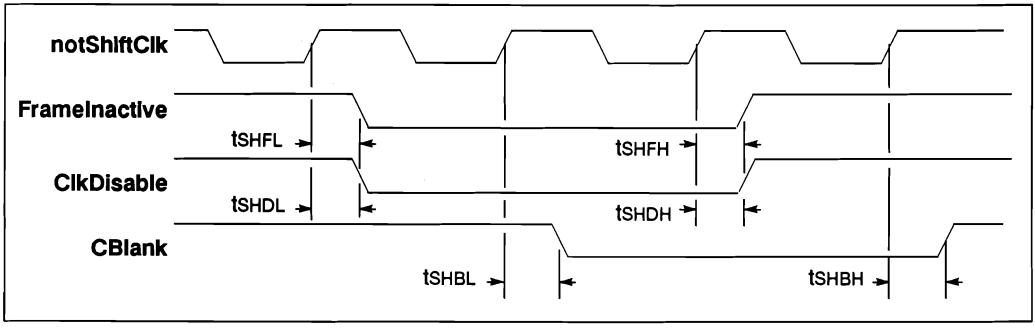


Figure 6.9 Relationship between **notShiftClk, FrameInactive, ClkDisable** and **CBlank**

Symbol	Description	-66 Min	-85 Min	-100 Min	-110 Min	Units
tSLSL	**notSerialClk** period	61	47	40	36	ns
tSLSH	**Clk** low time	12	10	10	10	ns
tSHSL	**Clk** high time	12	10	10	10	ns
tDVSL	data setup time	−3	−3	1	1	ns
tSLDX	data hold time	15	12	9	9	ns
Note: These figures are not characterised and are subject to change						

Table 6.7 Pixel port mode 1 timings

Symbol	Description	All Max	-66 Min	-85 Min	-100 Min	-110 Min	Units
tCLCL	Pixel period	10000	31	25	20	18	ns
tCHCL	**ClkIn** high time	10000	10	8	7	6	ns
tCLCH	**ClkIn** low time	10000	10	8	7	6	ns
tPVCH	Pixel data setup time		6	5	4	4	ns
tCHPX	Pixel data hold time		6	5	4	4	ns
Note: These figures are not characterised and are subject to change							

Table 6.8 Pixel port mode 2 timings

Symbol	Description	Min.	Max.	Unit
tSHFL		-5	5	ns
tSHFH		-5	5	ns
tSHDL		-5	5	ns
tSHDH		-5	5	ns
tSHBL		SClk/4-5	SClk/4+5	ns
tSHBH		SClk/4-5	SClk/4+5	ns

Table 6.9 **notShiftClk, FrameInactive, ClkDisable** and **CBlank** parameters

6.7 ClockIn timing reference guide

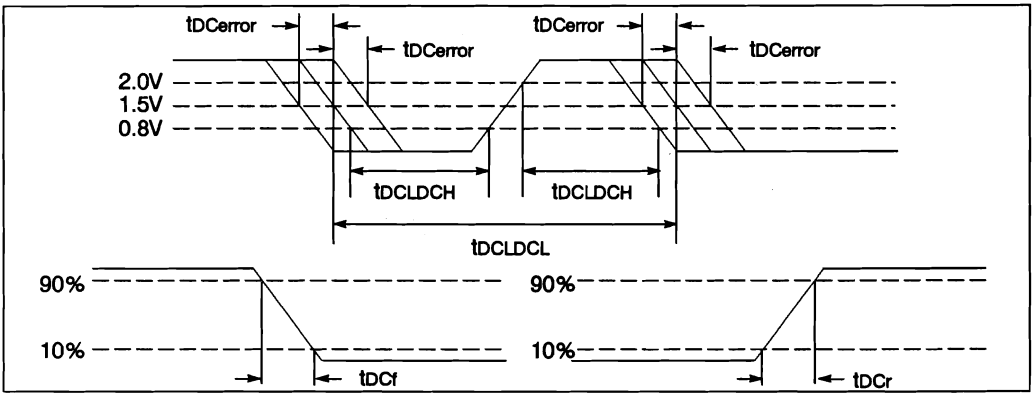


Figure 6.10 **ClockIn** timing

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
tDCLDCH	ClockIn pulse width low	20			ns	
tDCHDCL	ClockIn pulse width high	20			ns	
tDCLDCL	ClockIn period	100		200	ns	1
tDCerror	ClockIn timing error			±0.015	%	2
tDCr	ClockIn rise time			10	ns	3
tDCf	ClockIn fall time			8	ns	3
Note: These figures are not characterised and are subject to change						

Table 6.10 **ClkIn** timings in PLL mode

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their normal times.

3 Clock transitions must be monotonic within the range **VIH** to **VIL**.

6.8 General parametric conditions and characteristics

6.8.1 Absolute maximum ratings*

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	-1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	-55	125	°C	
TA	Temperature under bias	-40	85	°C	
PDmax	Power dissipation		2	W	
	Reference current	-15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

*Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

6.8.2 Operating conditions

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	1
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD + 0.3	Volts	
VIL	Input Logic '0' Voltage	−0.3		0.8	Volts	
TCPGA	Case Temperature	tbd		tbd	°C	2,3
TCQC	Case Temperature	tbd		tbd	°C	2,3
Note: These figures are not characterised and are subject to change						

Notes

1 AVDD = VDD

2 Measured on the lid of the package at maximum power dissipation.

3 VDD = 5V

6.8.3 Operating characteristics

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
IDD	Power Supply Current		250	tbd	mA	
IIN	Digital Input Current			±10	µA	
IOZ	Off State Dig Output Current			±50	µA	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	−5			mA	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOH	Output Logic '0' Current	5			mA	
Note: These figures are not characterised and are subject to change						

6.8.4 Output drive capability

Parameter	Min.	Typ.	Max.	Units	Notes
notShiftClk			25	pF	1
notSerialClk			25	pF	1
Transfer			25	pF	
ADBus [23:0]			25	pF	

Notes

1 **This loading limit must be strictly adhered to or picture quality will be degraded.**

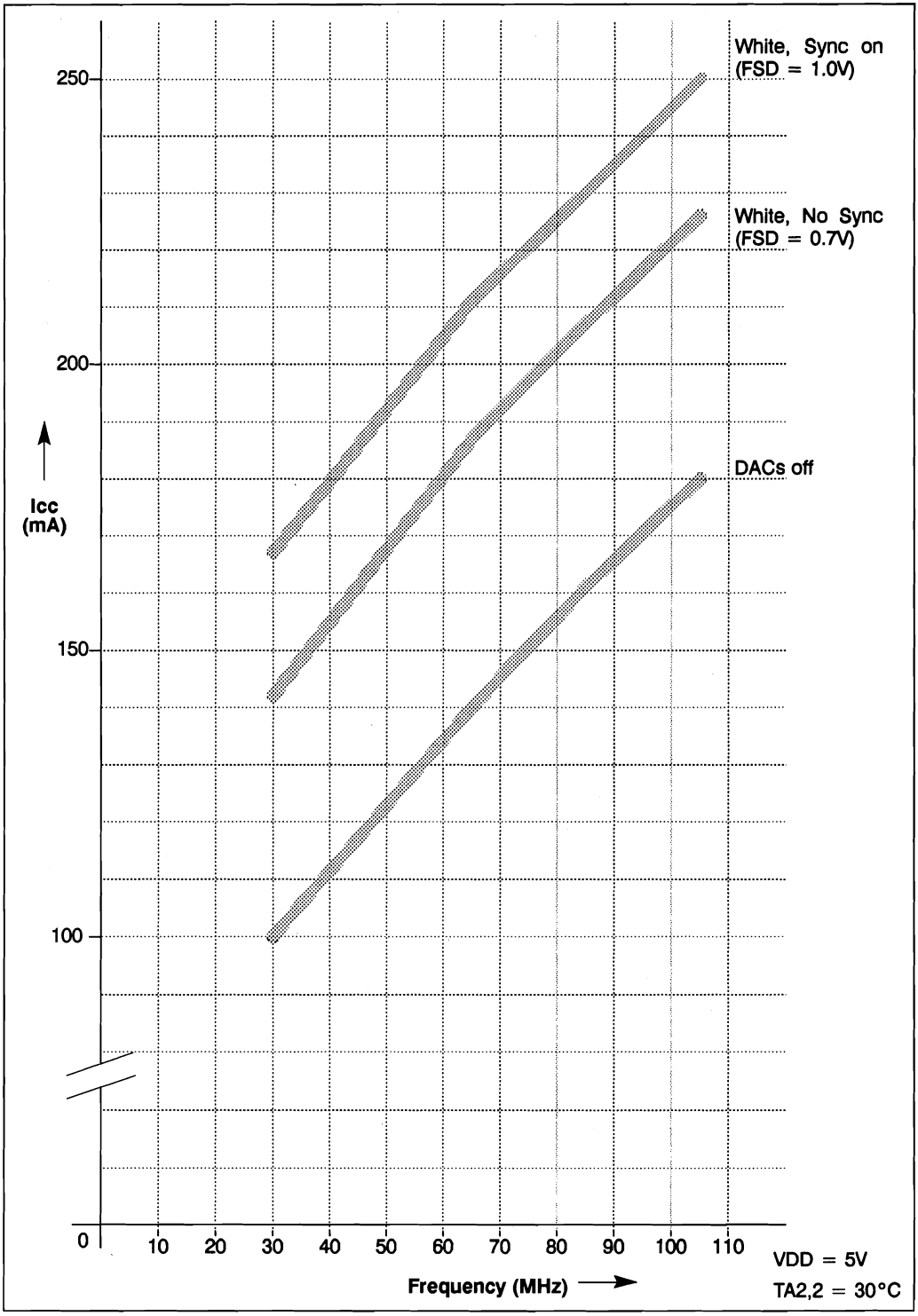


Figure 6.11 Icc (typical) versus pixel frequency

6.9 The video timing generator

6.9.1 Introduction

The Video Timing Generator is a programmable finite state machine. It provides composite sync and blanking to the on-chip video DACs, it controls the timing of **BusReq** and **Transfer** and it starts and stops **notShiftClk** to control the flow of pixels onto the screen. It also provides a **FrameInactive** signal which is asserted whenever the display enters frame flyback, enabling the controlling processor to perform frame flipping or major screen updates invisibly.

The timing generator can be configured to control an interlaced or non interlaced monitor and to generate the synchronising waveforms required by the EIA-343 (NTSC) and CCIR (PAL) studio television standards. These options are selectable in software and are controlled by the contents of the control register. Also controlled by this register is the operating mode of the device; it can be set to free run in which case it will drive synchronising signals out, or it can be set into slave mode when it will lock onto frame and line sync pulses supplied externally.

Programming of the timing generator is achieved by writing a set of screen description parameters to the timing registers. Its resolution is one quarter that of the individual pixels hence the scan lines must be described in 'screen units' of four pixels each (i.e. a line with 1024 pixels is described as having 256 screen units).

6.9.2 The display screen

In a raster scan display system, the picture is built up of a number of visible lines, which are displayed and a much smaller number of frame flyback lines, which are blanked. Each of the displayed lines has a single, visible, display period and a blanked line flyback period made up of front and back porch plus line sync. The total linetime is the sum of the displayed and blanked periods.

The frame timing periods are specified in multiples of half a linetime while the line timings are specified in screen units of four pixels duration each.

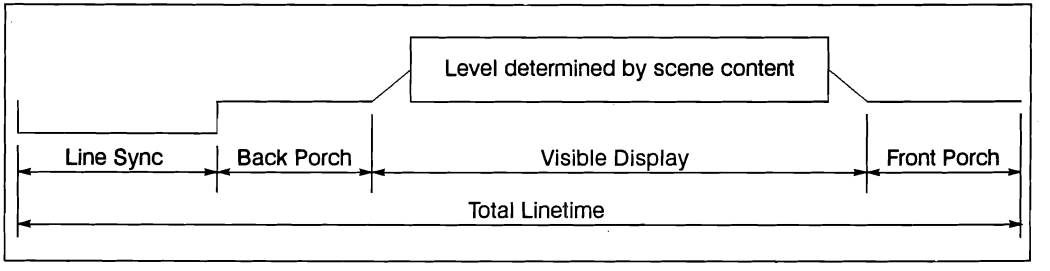


Figure 6.12 Scan line segments

Each displayed scan line of the raster is built up of the sections shown in figure 6.12. The visible portion is contained within the period 'display', so that, if a screen width of 1024 visible pixels (equal to 256 screen units) is required, then 256 is the number written to the 'display' register. For the remainder of the scan, the display is in line flyback and is therefore blanked.

The total linetime is the sum of all the sections of figure 6.12 and this is the number written to the 'linetime' register.

6.9.3 Line timing parameters

The line segments shown in figure 6.12 map directly to timing generator registers with two exceptions. First, the line synchronising pulse is split into two periods of equal duration which are used in immediate succes-

sion – the parameter used for this is 'halfsync' – and second, there is no register for frontporch, rather the total line time is programmed into a separate register and the end of the scan line occurs when this time-base period expires.

Figure 6.13 (a) shows the flowchart of a standard displayed or blanked scan line (as distinct from the truncated unscanned lines used in vertical sync and equalisation). The state machine proceeds from one state to the next according to the delay programmed in by the user; on entering a new state the Sync and blanking outputs are modified depending on which part of the cycle is being executed.

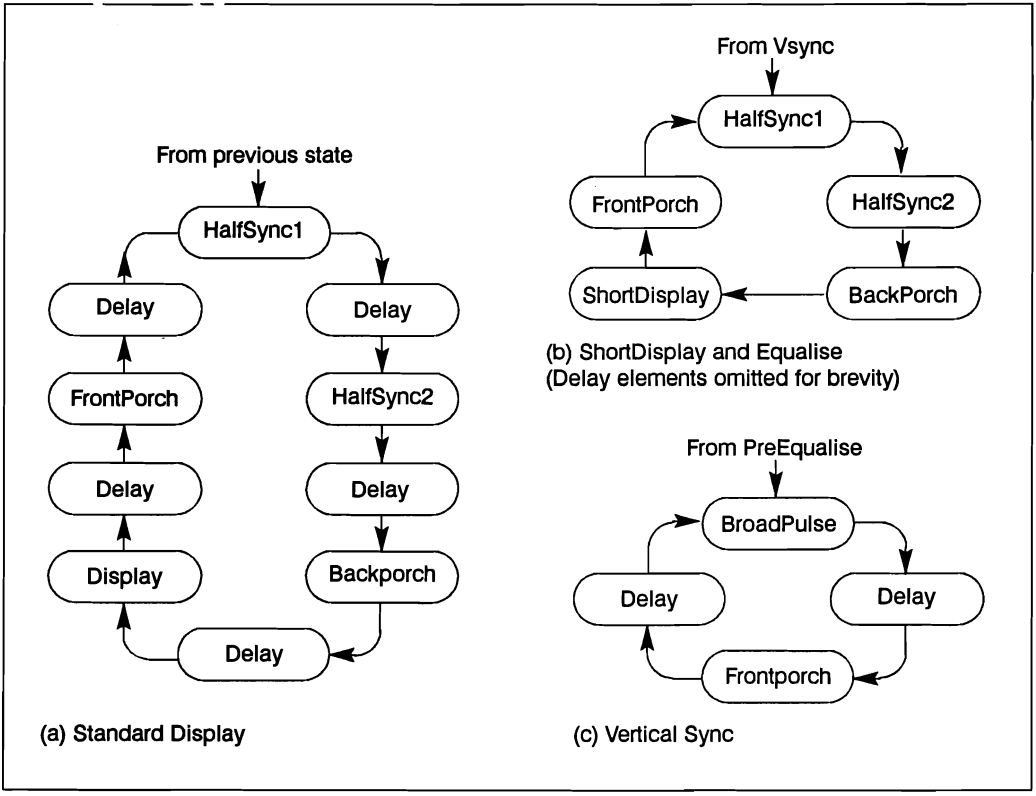


Figure 6.13 Flow diagrams for video timing generator

Figure 6.14 (a) shows the relationship of the screen description parameters to a full scan line. Note that frontporch is undefined and halfsync is used twice in succession to construct the line sync pulse.

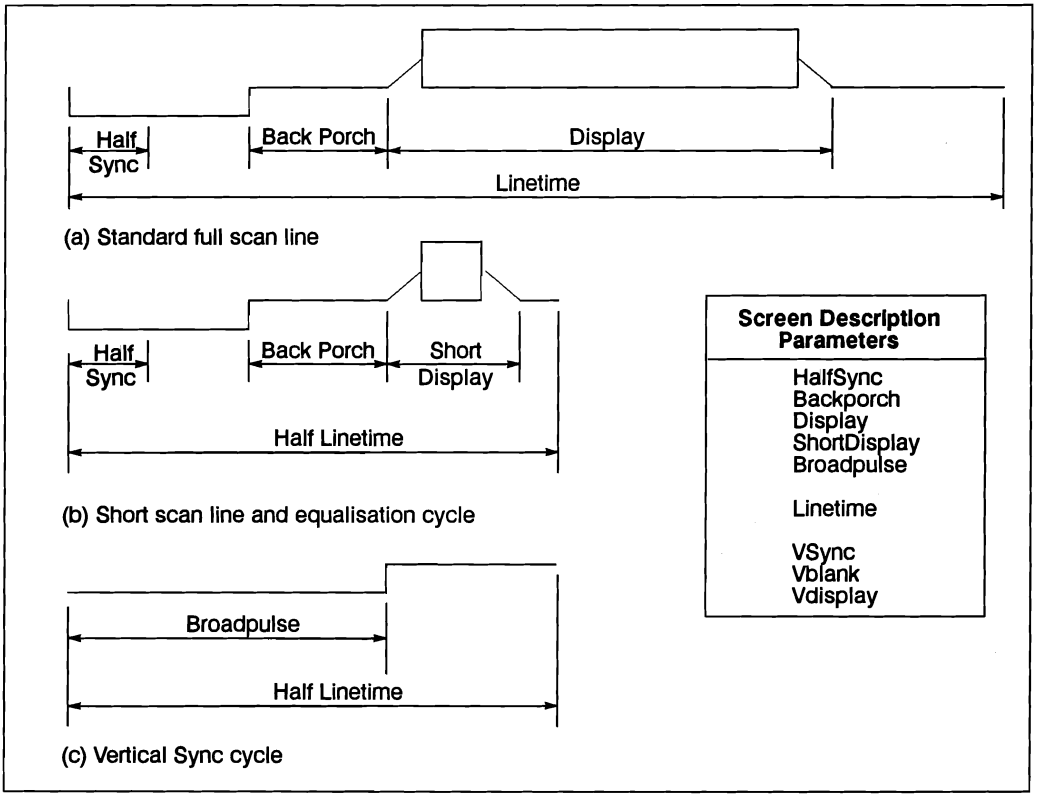


Figure 6.14 Screen description parameter definitions

6.9.4 Frame timing parameters

The G300 generates synchronising signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating the ordinary frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tesselated sync signals for an interlaced television system (see figure 6.15).

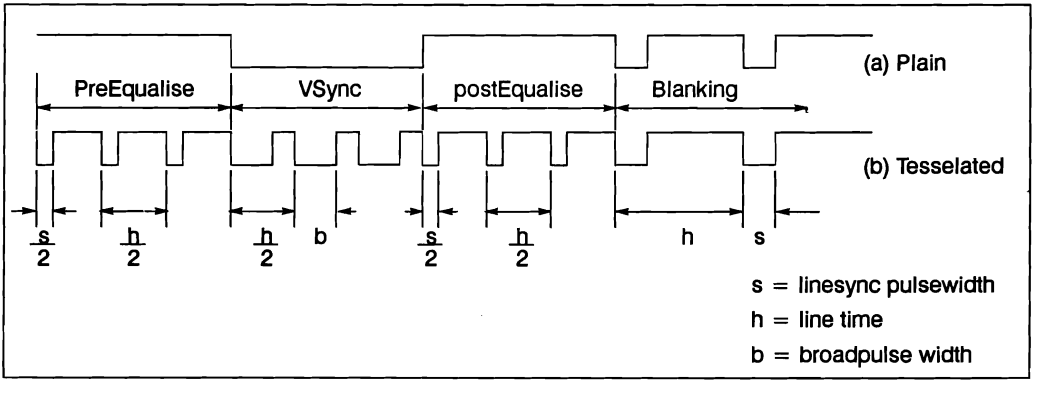


Figure 6.15 Composite Sync frame flyback waveforms

A further requirement of the television standards is that each frame must contain an odd number of scan lines. As a result, the frame timing parameters need to be specified in terms of half line times. Thus a non-in-

terlaced screen of 1024 visible lines has the value 2048 written to the VDisplay register. (An interlaced screen of 625 lines would have 625 in that register since in interlace, the VDisplay register decribes the vertical display *field* rather than the entire frame – see table 6.11).

Screen Type	Lines per Frame	Value in VDisplay Register	Lines per Field
non-Interlace	1024	2048	1024
Interlace	1024	illegal	illegal
non-Interlace	625	1250	625
Interlace	625	625	312.5

Table 6.11 Frame programming examples

The duration of preEqualise, postEqualise and VSync are all set by the VSync parameter and are hence always equal, the vertical backporch period is independent and has its own parameter, Vblank. The total frame blanking period is the sum of these four.

In order to generate the tesselated equalisation and blanking waveforms shown in figure 6.15(b), some additions to the basic line parameters are needed. The low period during VSync is defined as 'broadpulse' with its duration stored in the 'broadpulse' register. The shorter low period during pre and post equalisation is equal to half the line sync period and hence uses the value stored in the 'halfsync' register.

Reference to figure 6.13(b) and (c) shows that, on entering frame flyback, the state machine loop shortens to give a period of half a linetime. In equalisation, this is achieved simply by substituting 'shortdisplay' for 'display' in the sequence, whereas in vsync the sequence is changed to include only 'broadpulse' and 'frontporch'.

6.9.5 Parameter calculation

Calculation of the frame timing parameters is simple and direct – to produce the flyback waveform in figure 6.15(a) the parameter VSync is set to 3 – and the line parameters are derived from the equations in table 6.12. There is also an example in section 6.17.

During a full line cycle (VBlank, VDisplay)		
Halfsync	=	Horizontal Sync/2
BackPorch	=	BackPorch
Display	=	Display
Linetime	>	(2×HalfSync + BackPorch + Display)
During an equalisation cycle		
ShortDisplay	<	Linetime/2 – (2×HalfSync + BackPorch)
Low period	=	HalfSync
High period	=	Linetime/2 - HalfSync
During a VSync cycle		
BroadPulse	=	Linetime/2 - Pulse width*
Low Period	=	BroadPulse
High period	=	Pulse width

Table 6.12 Screen description line parameter equations

* Note: Pulse width = duration of serration pulse high time

The following restrictions on parameter values must be observed:

- All parameters must be non-zero.
- Linetime must be an even multiple of the period of **notSerialClk**.
- 2×HalfSync + BackPorch + Display > Linetime/2 > 2×HalfSync + BackPorch.
- The total number of displayed lines in each frame must be a whole number. In interlace, this must be an odd whole number.
- Backporch must exceed TransferDelay by at least one **notSerialClk** period.
- Transfer delay must not exceed ShortDisplay.

(The parameter TransferDelay is described in section 6.12).

6.9.6 The startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is accomplished while the timing generator is disabled.

On startup, after reset, the host processor must write a configuration pattern to the G300 bootstrap location. The effect of this is to set the PLL multiplication factor and clock source (PLL or external crystal). The host should then wait for a period t_{C1C2} for the PLL to settle to the new value. Following this it must set the microport mode (byte wide or word wide) by writing to bit 7 in the control register and initialise the VTG by writing a 0 to bit 0.

Startup sequence:

1 Assert, then deassert **Reset**.

2 Write configuration pattern to bootstrap location.

3 Write to control register to set microport and initialise VTG.

After this the screen parameters and colour table data can be written to the appropriate locations in any order. The processor must then make another write to the control register to enable the VTG which will then start up immediately at the beginning of frame sync. The G300 can be reprogrammed without asserting Reset.

The reprogramming sequence has three steps:

1 Write zero to bit 0 of the control register, disabling VTG.

2 Write to the screen parameter registers chosen for redefinition.

3 Write one to bit 0 of the control register, (redefining modes if necessary by modifying the relevant register bits) and enabling the VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed the full startup procedure must be followed, including reset.

6.10 The G300 Address Map

The various register locations of the IMS G300 are memory mapped as shown in the table below. The values given are hexadecimal word addresses driven on to **ADBus2-10** All other locations within the address space occupied by the G300 are reserved and must not be addressed. The boot location is not readable, all other locations are read/write.

Location	Address
Colour Palette	
starts	#X000
ends	#X0FF
Mask Register	#X140
Control Register	#X160
Top of Screen	#X180
Boot Location	#X1A0
Data Path Registers	
HalfSync	#X121
BackPorch	#X122
Display	#X123
ShortDisplay	#X124
BroadPulse	#X125
VSync	#X126
VBlank	#X127
VDisplay	#X128
Linetime	#X129
Top of Screen	#X12A
MemInit	#X12B
TransferDelay	#X12C

Table 6.13 IMS G300 address map

6.11 Synchronising and Blanking signals

6.11.1 Introduction

The video timing generator produces sync and blank signals to a pattern specified by a combination of the operating mode of the G300 and the screen description parameters. Internally, composite sync and composite blank are supplied to all three video DACs by default. However, both of these functions can be disabled by setting bits 5 and 15 of the control register, respectively.

The internal sync and blank signals are supplied with the correct delay to allow for the transfer of data from the video RAM array into the G300 with the difference in delay due to the alternate G300 operating modes automatically catered for.

In order to allow pipeline stages between the output of the video RAM and the pixel inputs , the IMS G300 includes a programmable delay line which can be set (via Control Register bits 9 to 11) to insert a further delay of up to seven **notSerialClock** cycles between the outputs of the VTG and the inputs of the DACs.

6.11.2 Master mode

When running in master (internal sync) mode, the **VSync** and **CorHSync** pins are outputs and the G300 drives them in the appropriate fashion, active low. Composite or Horizontal sync selection is specified by Control Register bit 4. Untesselated frame sync always appears on the **VSync** pin while the **CorHSync** pin is switchable to supply one of Line sync, untesselated composite sync or tesselated composite sync (see table 6.14). These signals are all delayed by the same amount as the internal sync signals specified above. They are also subject to the further delays as programmed into the control register.

Control Bits		Vsync	CorHSync	
			HSync	CSync
4	3			
0	0	Plain	-	Tesselated
0	1	Plain	-	Plain
1	0	Plain	Plain	-
1	1	Plain	Plain	-

Table 6.14 Sync Style Selection

6.11.3 Slave mode

In slave mode the **VSync** and **CorHSync** pins are designated as inputs and the G300 will lock onto vertical and horizontal sync pulses supplied to them.

The sampling circuit on the **Sync** inputs means that the IMS G300 can be locked to a completely asynchronous source without metastability problems. It will tolerate a large amount of instantaneous variation in the synchronising inputs due to the inbuilt flexibility of the timing algorithm. This provides synchronisation guaranteed to within one period of **notSerialClk**, which may not be adequate in a system where two video streams are being merged. In this case, it is necessary to observe the timing shown in figure 6.16 when the G300 will give no synchronising errors.

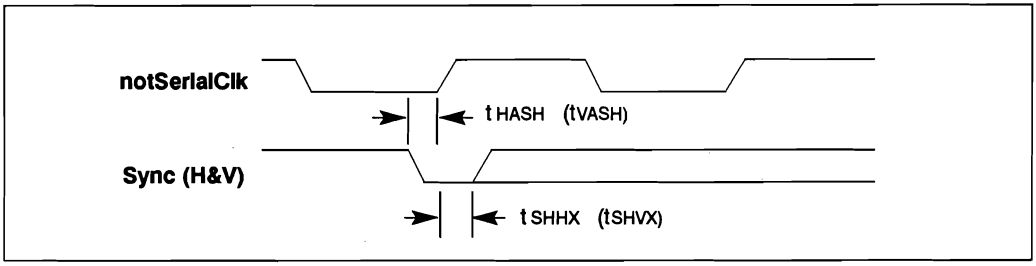


Figure 6.16 External synchronisation

For a genlocked system, it will be necessary to run the G300 in external clock mode (ie: not using the phase locked loop) with **ClkIn** derived from the global linesync using a standard sync splitter and external PLL.

When set to slave mode, the G300 will free run until it recieves a frame sync signal which resets the timing generator to the start of **VSync**. There will be a fixed delay between the **VSync** signal being detected and the VTG restarting. This delay will remain constant from then on. In an interlaced system, the G300 will sample the line sync pulses to determine the current field and, on detecting an error, it will resynchronise at the start of the next field, thus there may be a period of one field duration before a correct lock is achieved. In order to function correctly, the external line sync pulse must overlap by at least one period of **notSerialClk** with the internally produced line sync.

Symbol	Description	Min.	Max.	Unit
tVASH	Vsync setup time	SClk/4	3SClk/4	ns
tHASH	Hsync setup time	SClk/4	3SClk/4	ns
tSHVX	Vsync hold time	0		ns
tSHHX	Hsync hold time	0		ns
Note: These figures are not characterised and are subject to change				

Table 6.15 External sync waveform timings

6.11.4 Digital Blanking pin

The **CBlank** pin is configured by bit 16 of the Control Register to be input or output. As an input it is treated in exactly the same way as a pixel thus in mode 1 its resolution varies from every fourth pixel boundary at 8 bits per pixel to every 32nd pixel boundary at one bit per pixel. In mode 2 it is sampled along with each pixel latched in. The input data on this pin has the same timing requirements as a Pixel input.

As an output, **CBlank** has two distinct possible functions which are selected by bit 23 of the Control Register. Function one is as a simple blanking output, active high and delayed to coincide with the blanking period of the DAC outputs. Function two is as a clock disable pin. This is undelayed with respect to **notShiftClk** and has special behaviour at the start of an even interlace field. Whereas composite blank is active during the first half of the first scan line of an even field, clock disable is not, so that the requirements of the VRAM framestore can be met. The purpose of this function is to stop and start the pixel clock in a system which uses less than 4:1 multiplexing in the video RAMs, as is possible in mode 2 operation.

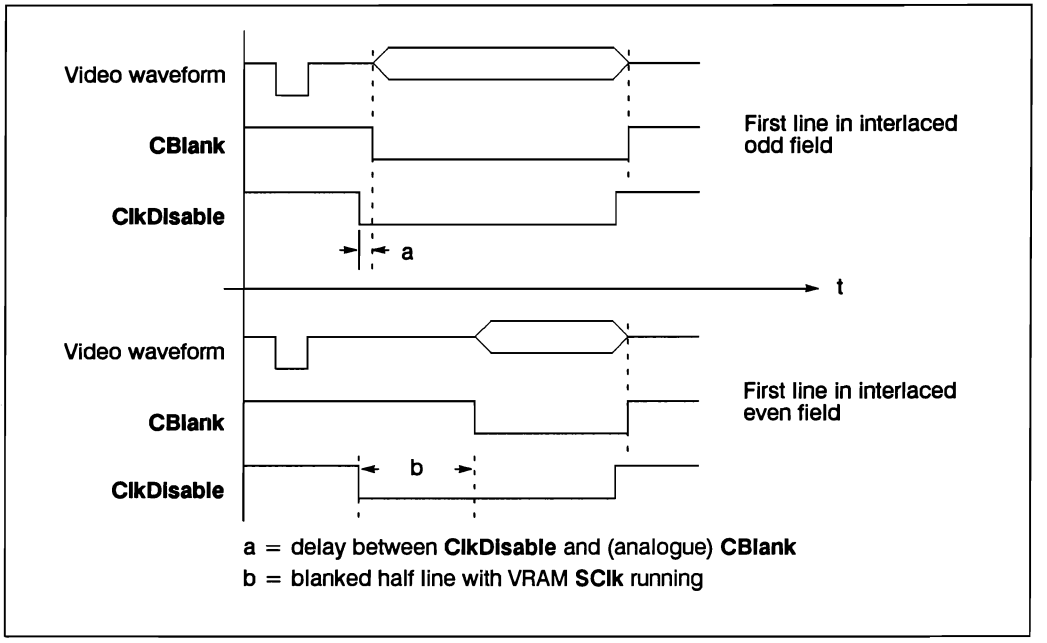


Figure 6.17 Relationship between Video, **CBlank** and **ClkDisable**

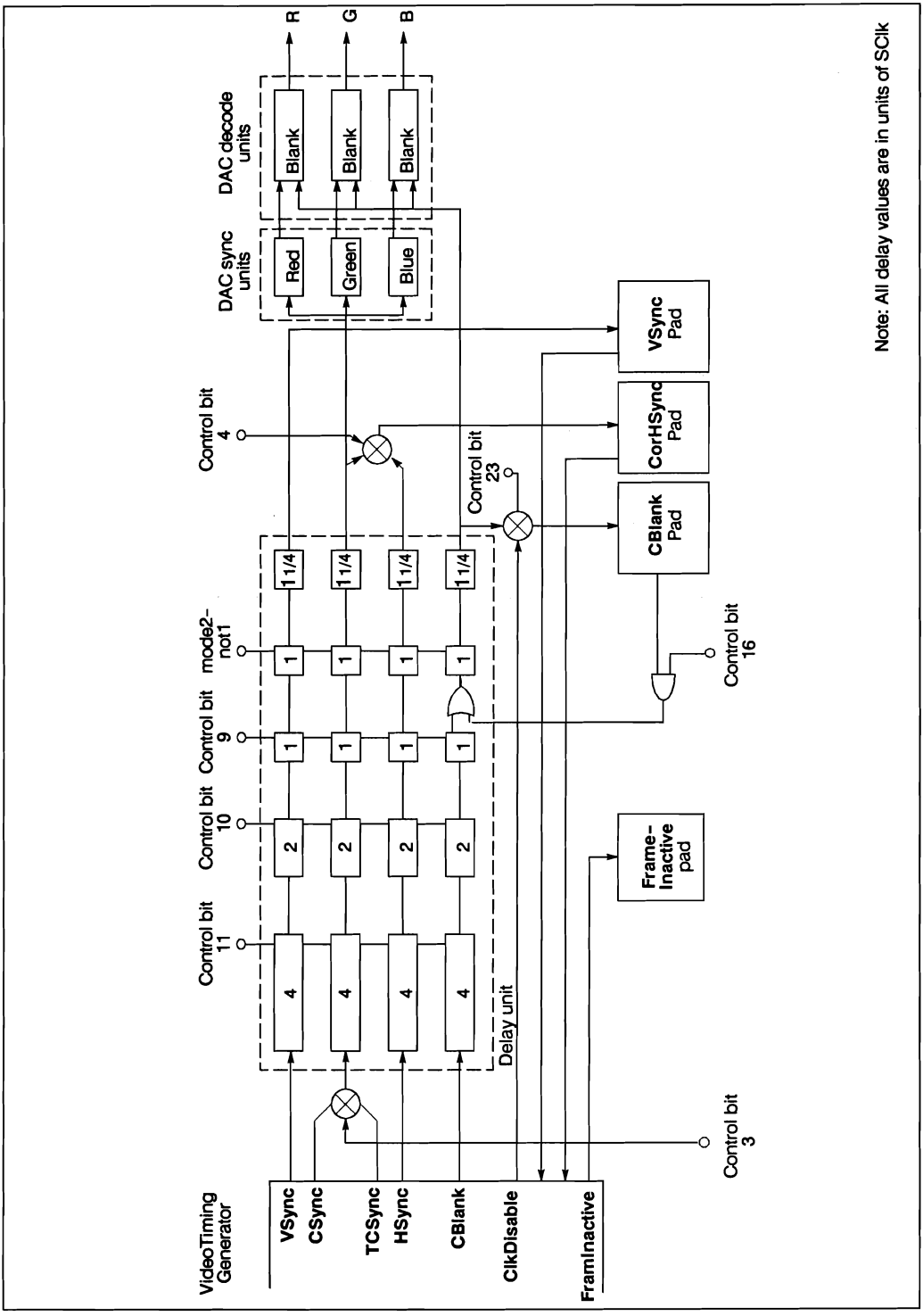


Figure 6.18 Digital and analogue syncing and blanking system

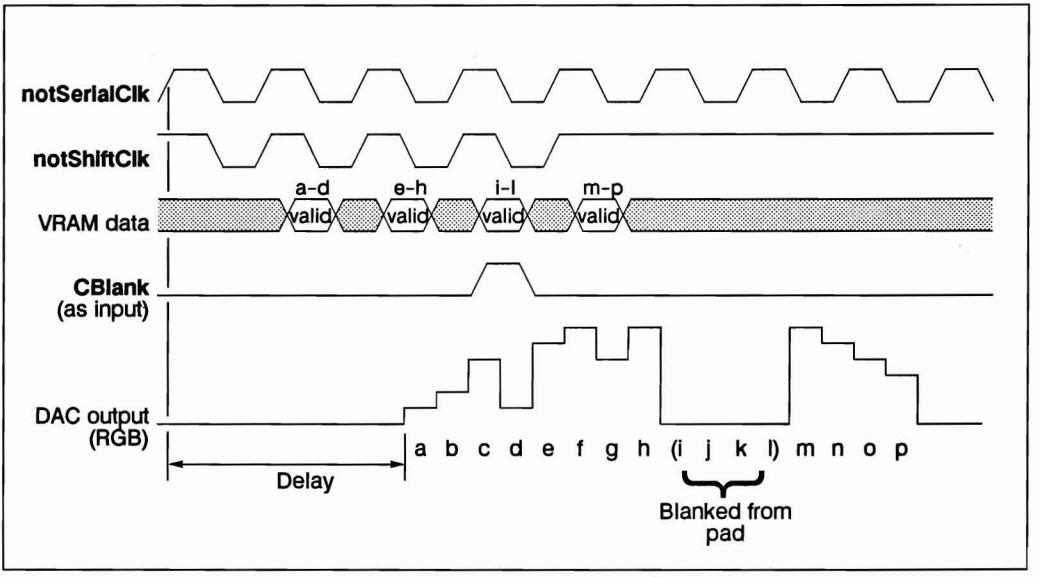


Figure 6.19 Delay between **notShiftClk** and DAC outputs in mode 1

$$\text{Delay} = \text{SClk} \times (2.5 + 4 \times \text{Control bit 11} + 2 \times \text{Control bit 10} + 1 \times \text{Control bit 9})$$

Note: Diagram shows delay with Control bits 9 to11 = 0

6.12 The micro port

6.12.1 Introduction

The micro port is a bidirectional 24 bit interface which can be configured to operate in byte wide or 24 bit wide mode (word mode). It consists of a multiplexed address and data bus with several control signals, described below, and is used for programming both the video timing generator screen description registers and the colour lookup table. The micro port timings are asynchronous with the remainder of the G300.

As well as serving as a programming port the interface is also capable of performing a video RAM shift register transfer operation using a fully handshaken DMA. The timing of this operation is synchronous with the pixel port and is arranged so that seamless update of the video RAM shift register is possible.

6.12.2 Initialisation

The choice of clock source is made by writing to bit 5 in the boot location. If the phase locked loop is to be used, a suitable crystal oscillator must be connected to the **ClkIn** pin. If the direct drive option is used, the system must supply a dot rate clock to the **ClkIn** pin. On Power up, the **Reset** pin must be taken high and ClkIn must have been running for at least t_{CVRL} after **VDD** is valid before the end of **Reset**. After deasserting **Reset**, the first access to the micro port must be a preliminary configuration access to the boot location as specified in section 6.9. This sets the clock source and the PLL multiplication factor if the clock source is to be the PLL. This first access must occur after a minimum period of time after **Reset** goes low (t_{RLCL}).

The microport mode defaults to word mode on reset so, if byte wide operation is required, it must be selected by writing to bit 7 in the control register.

Once these two write cycles have been performed normal operation of the micro port may commence.

6.12.3 Programming operation

For normal read and write cycles the address is latched into the G300 on the falling edge of **notCS**. **ReadNotWrite** is sampled 1/2 a period of **notSerialClk** later to establish the cycle type. In a read cycle, the data lines will be driven a time t_{CLDV} later and will remain valid until **notCS** goes high. In a Write cycle, data will be latched into the G300 on the rising edge of either **ReadNotWrite** or **notCS**, whichever occurs first.

6.12.4 Byte Wide operation

When the part is configured to byte-wide mode, three complete read or write cycles must be made to the same address in order to complete each cycle. The data is written to or read from **ADBus0-7** least significant byte first. A byte wide read or write may be aborted before completion without causing data corruption. The system is reset by latching in a new address.

Read cycles

The micro port stores a history of accesses using a three-deep buffer. For every Read cycle, it determines whether the last access was a read, and if so, whether it was from the same address. If the last access was a write, or if it is was from a different location to the current read, then an internal 24-bit data fetch is performed and the least significant byte is driven out onto **ADbus 0-7**.

If the current read is from the same address as an immediately preceding read, the data stored from that previous internal data fetch is rotated eight bits and the next most significant byte is driven onto **ADbus 0-7.**

Write cycles

For a Write cycle, the data presented to **ADbus 0-7** is stored until the micro port detects the third write to the same address, when an internal data store is performed. If a byte write sequence is aborted before completion by either writing to a different address or by performing a read, then no data will have been written due to that operation.

Writing to the Control register in byte mode

The control register is a special case in that the access history must be reset between two consecutive accesses to its address. This is done in the normal way by performing an aborting cycle.

Thus two control register writes must be separated by either a read or a write to some other location.

Address #X1B0 is a suitable address for Null accesses.

Interaction with DMA

The byte access history registers are completely static so that there is no overall time limit for completion of a byte access. However, if the G300 completes a DMA cycle before a byte access sequence has completed, then that cycle must be aborted and restarted.

Aborting a byte-access sequence

A read access sequence is aborted by performing a write, and a write access sequence is aborted by performing a read. If the access is being aborted to perform a sequence of the other type then the aborting access can be from the first access of a sequence. If the aborted access is to be restarted immediately then the aborting access is itself aborted by the restarted operation.

Initialising to byte mode

Since the G300 defaults to word mode, the control register access to set the microport to byte mode is an exception to the above rules. It must be aborted after a single access, before normal operation commences. If the access immediately following it is to be a read, that is sufficient to initialise the byte sequencer—but a single read operation must be inserted if the next access is a write.

6.12.5 Byte access sequence definitions

Definition	Notes
a) Write to control register to configure micro port to byte mode	
1 Write to #160, setting bit 7 to 'one'	
2 Read from #1B0	
3 Commence normal byte operations	
b) Normal byte write sequence	
1 Write to address #A, driving least significant byte of word onto **ADBus0-7**	
2 Write to address #A, driving next significant byte of word onto **ADBus0-7**	
3 Write to address #A, driving most significant byte of word onto **ADBus0-7**	
c) Normal byte read sequence	
1 Read from address #A, reading least significant byte of word from **ADBus0-7**	
2 Read from address #A, reading next most significant byte of word from **ADBus0-7**	
3 Read from address #A, reading most significant byte of word from **ADBus0-7**	
d) Normal byte access to/from control register	
1 Perform normal read or write sequence as defined above to/from address #160	
2 Perform normal read or write sequence to/from address #1B0	1
e) Aborted byte write sequence	2
1 Perform steps 1, or steps 1 and 2 of Normal byte write	
2 Either : i) Write to any address except #A or ii) Read from any address	
f) Aborted byte read sequence	2
1 Perform steps 1, or steps 1 and 2 of Normal byte read	
2 Either : i) Read from any address except #A or ii) Write to any address	

Notes

1 This step can be replaced by either:
i) A single read/write from any location except #160
or:
ii) A valid byte read/write sequence from any valid location.

2 The aborting read or write may be the first operation of a valid byte read or write sequence.

6.12.6 The transfer address, line start and top of screen

The G300 outputs a new 22 bit address on **ADBus2-23** during every transfer cycle it initiates. The first address in each frame is specified in the Top of Screen register, which is programmed on startup but which can be modified at any time. Note that this register appears at two separate locations, Line Start and Top of Screen. Line Start is accessible only when the VTG is disabled, Top of Screen, only when it is running.

The current row address is incremented by the amount specified in bits 20-19 of the control register, used in conjunction with the 'Interlace' bit (bit 2). These bits specify the VRAM step length and the screen format. Refer to table 6.16. for bit assignments.

The column address is never incremented by the G300 so that the SAM start address remains constant until modified by the host.

Changes to the Top of Screen pointer become effective from the top of the subsequent screen (or field in an interlace system).

The framestore format for interlace is identical to that for non-interlace. Address ordering depends on the standard selected. CCIR scans even lines first, NTSC scans odd lines first.

In interlace, the first half of Line Zero is always blanked at the video DACs but the G300 will clock the VRAM shift registers as though visible. This preserves compatibility between interlace and non-interlace.

Option	Register Bit			Description
	20	19	1	
a	0	0	0	Increment by 1. Non interlace format. Maintains compatibility with equivalent G300A mode.
b	0	0	1	Increment by 1. Interlace format.
c	0	1	0	Increment by 256. Non interlace format.
d	0	1	1	Increment by 2. Interlace format. Replaces G300A interlace mode. Every second field offset by 1.
e	1	0	0	Increment by 512. Non interlace format.
f	1	0	1	Increment by 512. Interlace format. Every second field offset by 256.
g	1	1	0	Increment by 1024. Non interlace format.
h	1	1	1	Increment by 1024. Interlace format. Every second field offset by 512.

Table 6.16

6.12.7 The screen transfer operation

The G300 provides two software programmable strobes which enable it to perform the necessary screen data-transfer cycles on video RAMs to reload the internal shift registers with new data. These may be synchronous updates which happen part way across a line or updates which occur during flyback.

The user may program these strobes, **BusRequest** and **Transfer**, to cause the data transfer cycles to occur at the correct points during the screen display to implement seamless line update, thus decoupling the screen configuration from dependence on the video RAM architecture. These strobes are controlled by values loaded into two special purpose registers, MemInit and TransferDelay. The G300 also outputs a transfer address specifying the new row of pixels to be displayed. It is left to the user to generate RAS, CAS and any other strobes he may need from **busRequest**, **Transfer**, **notSerialClk** and **notShiftClk**.

The G300 is primarily designed to be used with video RAMs, although it can be used with static or standard dynamic rams if desired. In this case the strobes provided can be used to arbitrate bitmap accesses.

6.12.8 Transfer cycle timing

Video RAMs reload their shift registers by performing a normal read cycle with a special pin (usually called notDT or notDT/notOE) held low as RAS falls. The address values presented to the VRAM on the falling edges of RAS and CAS define which row is loaded into the shift register and which bit in the shift register is shifted out first, respectively. The instant at which the actual transfer takes place is set by the time at which notDT is brought high again and this edge alone must be synchronised to the shift clock which clocks data out of the shift registers.

In many systems the reloading of the shift registers takes place at the end of the line during retrace. However, one of the most useful features of using the G300 with VRAMs is the ability to reload the shift registers mid-line. This allows screens with an arbitrary number of pixels per line to be constructed with any length shift register. In order to do this however some look-ahead is required in order to be able to make the transfer at exactly the right point without any discontinuity on the screen. This look-ahead is provided by programming the appropriate values into the MemInit and TransferDelay registers.

At the start of each display frame, the G300 will initiate a transfer cycle at the beginning of the backporch period of the first line and will perform the data transfer with the delay specified in the TransferDelay register.

This ensures that there is data loaded ready for the first line scan to begin.

The G300 will then begin to count **notSerialClk** cycles and will initiate a further transfer cycle after MemInit cycles of **notSerialClk** by asserting **BusReq**. After a further number of cycles of **notSerialClk** equal to TransferDelay, the G300 will take **Transfer** low and the new data will be loaded into the shift registers.

TransferDelay	$\leq$	Backporch -1
TransferDelay	=	System DMA Latency + VRAM Access + 4 SClk
MemInit + TransferDelay	$\leq$	VRAM shift register length - SAM start address
	In an interlaced system only:	
MemInit + TransferDelay	=	Display
TransferDelay	<	ShortDisplay

Table 6.17 Restrictions of screen update parameters

Thus the period of row transfer operations is;

MemInit + TransferDelay

and apart from the restrictions quoted above, it need bear no relation to the screen line length at all. This permits any display line length with any type of video RAM.

The critical parameter as far as DMA accesses are concerned is TransferDelay which needs to be long enough to allow for the DMA latency of the drawing processor as well as the access time of the video RAMs. The G300 imposes an extra overhead of one notSerialClk period which needs to be added to the Transferdelay parameter but which does not appear as part of the delay between **BusReq** and notDataTransfer.

If there is a data transfer operation pending when the system enters flyback, (i.e. the G300 would have control of the bus for a considerable length of time) then the transfer cycle is aborted before **BusReq** is made and will be restarted on the next following active display backporch. This ensures that any DRAM is never left unrefreshed during flyback and also makes best use of the available memory bandwidth. In order to implement this function, the G300 predicts, after a DMA is internally sheduled but before BusReq is asserted, that the video RAM shift registers are not going to run out of pixels before the end of the current line and hence the Row refresh may be left until the following active backporch. When **BusReq** is rescheduled the DMA is restarted at the beginning of backporch in the same way as the first line in the frame but the transfer delay parameter is carried over from the previous line and is incremented only when the system re-enters active display. This preserves the correct ordering of data onto the screen, while the insertion of the backporch period ensures that the DMA latency is always exceeded. Refer to figure 6.21 .

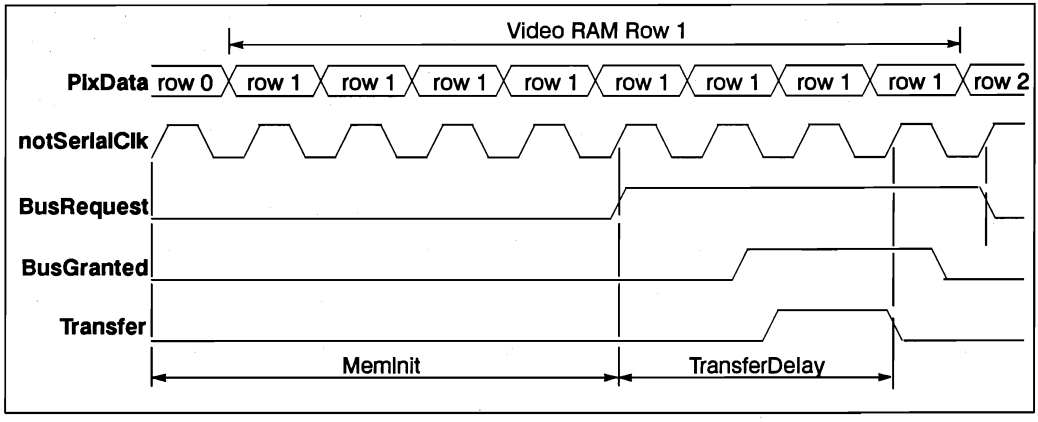


Figure 6.20 Data transfer sequence

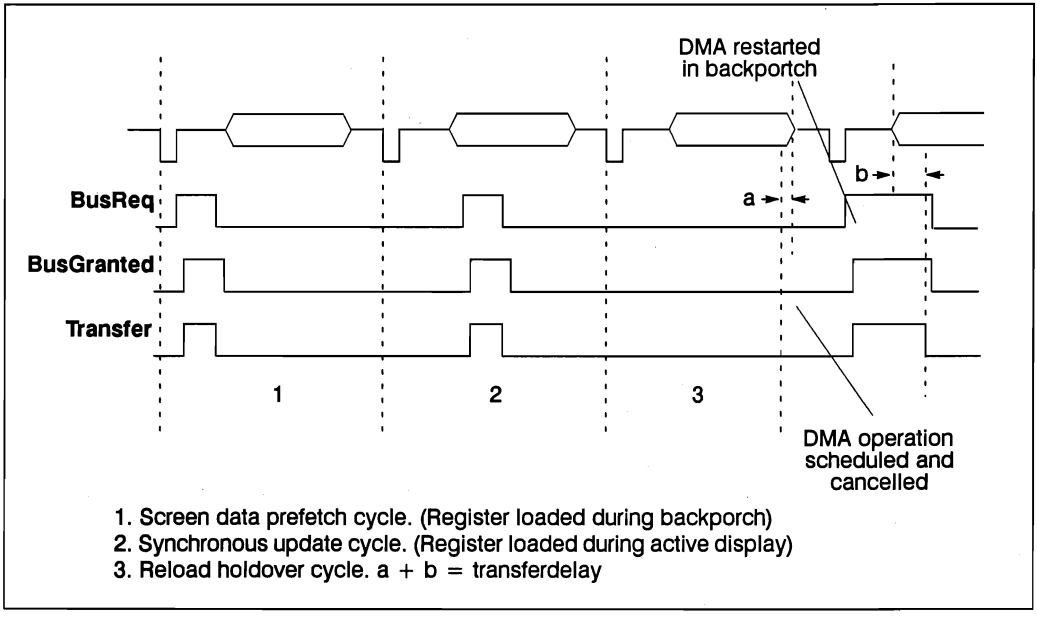


Figure 6.21 Data transfer operational behaviour

Figure 6.20 shows the sequence of events during a synchronised VRAM row transfer operation performed by the IMS G300 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers.

It should be noted that the G300 signals **notShiftClk**, **notSerialClk** and **Transfer** are all designed to be buffered by inverting buffers outside the G300 and so are the logical inverses of the signals driving the VRAMs.

MemInit defines the number of periods of **notSerialClk** before the G300 asserts **busRequest**. This is the first event which signals the start of a transfer cycle. When the host processor returns **busGranted** the G300 asserts **Transfer** and drives out the new transfer address to be strobed into the VRAMs. Only after a further number of **notSerialClk** cycles equal to TransferDelay, does the G300 remove **Transfer** (synchronously with respect to **notShiftClk**) and so perform the actual transfer. **busRequest** is also taken away at this point to return the **ADBus** back to the host. The user should arrange for TransferDelay to be sufficiently long to

allow for the worst case bus request latency plus the time required to strobe RAS and CAS with the address supplied from the G300.

The most memory-efficient way of using the transfer cycle feature is to make Meminit + TransferDelay equal to the length of the video RAM shift registers thus packing the bitmap into the smallest possible space, but it is obviously possible to specify a smaller number and then use the remainder of the bitmap as a larger 'world' which can be panned through by modifying the SAM start address between frames.

6.12.9 FrameInactive

A further timing signal, **FrameInactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **FrameInactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

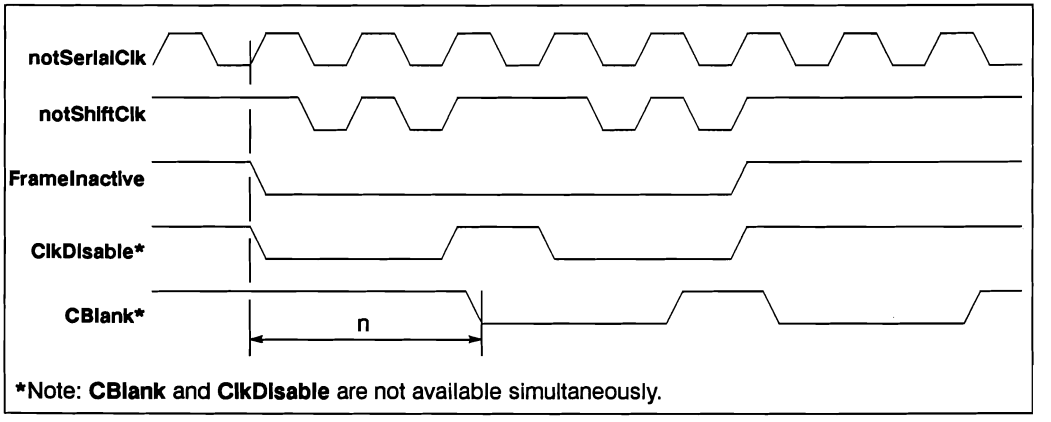


Figure 6.22 Relationship between **notShiftClk**, **FrameInactive**, **CBlank** and **ClkDisable**

FrameInactive goes low on the rising edge of **notSerialClk** immediately prior to the first falling edge of **notShiftClk** of each frame. It goes high on the rising edge of **notSerialClk** immediately after the last falling edge of **notShiftClk** of each frame.

Assuming the G300 is in 8 bits per pixel mode, **ClkDisable** goes low on the rising edge of **notSerialClk** immediately prior to the first falling edge of **notShiftClk** of each line. It goes high on the rising edge of **notSerialClk** immediately after the last falling edge of **notShiftClk** of each line. In all other bit per pixel modes **ClkDisable** is produced as though it were in 8 bit per pixel mode.

CBlank is similar to **ClkDisable** except that it is delayed with respect to **FrameInactive** by n cycles of **notSerialClk** where:

$$n = (2.25 - \text{Control bit 8} + 4 \times \text{Control bit 11} + 2 \times \text{Control bit 10} + \text{Control bit 9})$$

and, in interlace mode, the falling edge of **CBlank** on the first line of each even field is delayed by a further m cycles of **notSerialClk** where:

$$m = \text{linetime}/2 - (\text{Backporch} + 2 \times \textbf{HalfSync})$$

6.13 The pixel port

6.13.1 Pixel port operation

The pixel port takes in pixel data from the video RAM and has two modes of operation;

mode 1 – pseudo colour, multiplexed input.
mode 2 – gamma corrected full colour, direct input.

The mode is defined by a single bit in the G300 control register. The clock source is set by a combination of wiring option and boot location bit, (See the section on the programming interface). By varying these options it is possible to use the G300 in one of three configurations as shown in table 6.18.

Mode	Clock Option	Video Clock Source	Pixel Route
1	PLL (nom 5MHz)	Output of on-chip PLL	Through LUT
1	Direct (video rate)	**ClkIn**	Through LUT
2	Direct (video rate)	**ClkIn**	Through gamma table

Table 6.18 Clock and pixel port options

6.13.2 Mode 1 operation

In mode 1, 8 bits per pixel the G300 latches four 8-bit pixels on **PixDataA0-7**, **PixDataB0-7**, **PixDataC0-7** and **PixDataD0-7** on a single falling edge of **notShiftClk**. These four pixels are then serialised to the full pixel rate internally and applied to the colour palette address inputs in turn – A, B, C and D. In other bit per pixel modes the multiplex ratio is modified automatically.

The eight bit pixels used in mode 1, allow a choice of 256 simultaneous colours from a palette of 16 million. Changing the palette through the programming interface allows rapid colour selection and modification. The colour palette may be loaded and read back via the programming interface (see the G300 memory map). If the G300 memory interface is being used in word-mode, then a colour word may be loaded in one G300 external memory interface cycle and a complete colour palette may be block moved into or out of the G300 by the processor.

Mode 1 allows the pixel input to be multiplexed up to 32 into 1, this allows clocking of the video RAMs well below pixel clock frequency. The G300 supplies a signal **notShiftClk** which is designed to be buffered through a single inverting driver outside the G300 directly into the SC (serial clock) of each of the video RAMs. This clock pulses once for each new group of pixels required by the display. It is not free running, but stops during line and frame flyback. A free-running clock **notSerialClk** is also generated by the G300. This provides a continous clock synchronous to the video stream. If this clock is loaded identically to **notShiftClk** then its edges will be coincident to **notShiftClk**, it will not stop during flyback, and is always 1/4 pixel frequency. The frequency of **notShiftClk** depends on dot rate and the selected pixel depth.

notSerialClk = dot frequency/4
notShiftClk = dot frequency x bits per pixel/32

By taking a minimum of 4 pixels into the G300 in one go, the clock rate to the video rams for a nominal 110MHz system can be reduced to 27.5 MHz maximum. It is therefore possible to use standard video RAMs without extra multiplexing on the board. It is also possible to drive the pixel data down a backplane using easily available TTL parts in order to gang up extra boards in a distributed system. It has the further advantage that all external clocks and signals are running at comparatively low frequencies.

A memory mapped mask register is available for masking the incoming pixel address to the LUT in mode 1. The contents of this register (mapped onto **ADBus0-7**) are logically ANDed with the incoming pixel stream.

By altering the contents of this register the microprocessor may achieve simple rapid colour changes on the screen.

Colour programming in 1, 2 and 4 bits per pixel modes

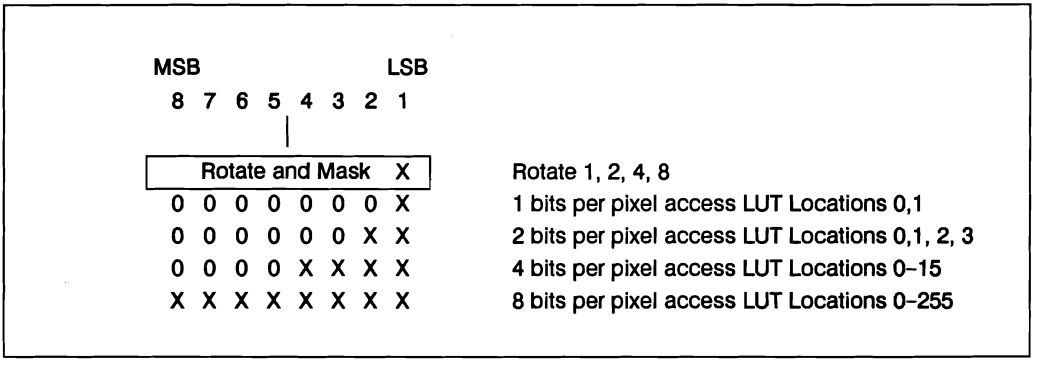


Figure 6.23 Colour palette programming information in 1, 2 and 4 bits per pixel modes

In 1, 2 and 4 bit per pixel modes, each byte is rotated and masked by an extra masking function as shown in figure 6.23

The bits per pixel mode must not be changed while the video timing generator is active.

Pixel ordering

The pixel order is always 'little-endian'. Thus:

In 8 bits per pixel mode, the first pixel displayed is byte A.

In 4 bits per pixel mode, the lower nibble of byte A is displayed first.

In 2 bits per pixel mode, bits 1, 0 of byte A are displayed first.

In 1 bit per pixel mode, bit 0 of byte A is displayed first.

Register Bit		Bits per pixel
18	17	
0	0	1
0	1	2
1	0	4
1	1	8

Table 6.19 Programming of bits 17 and 18 of the pixel mode control register

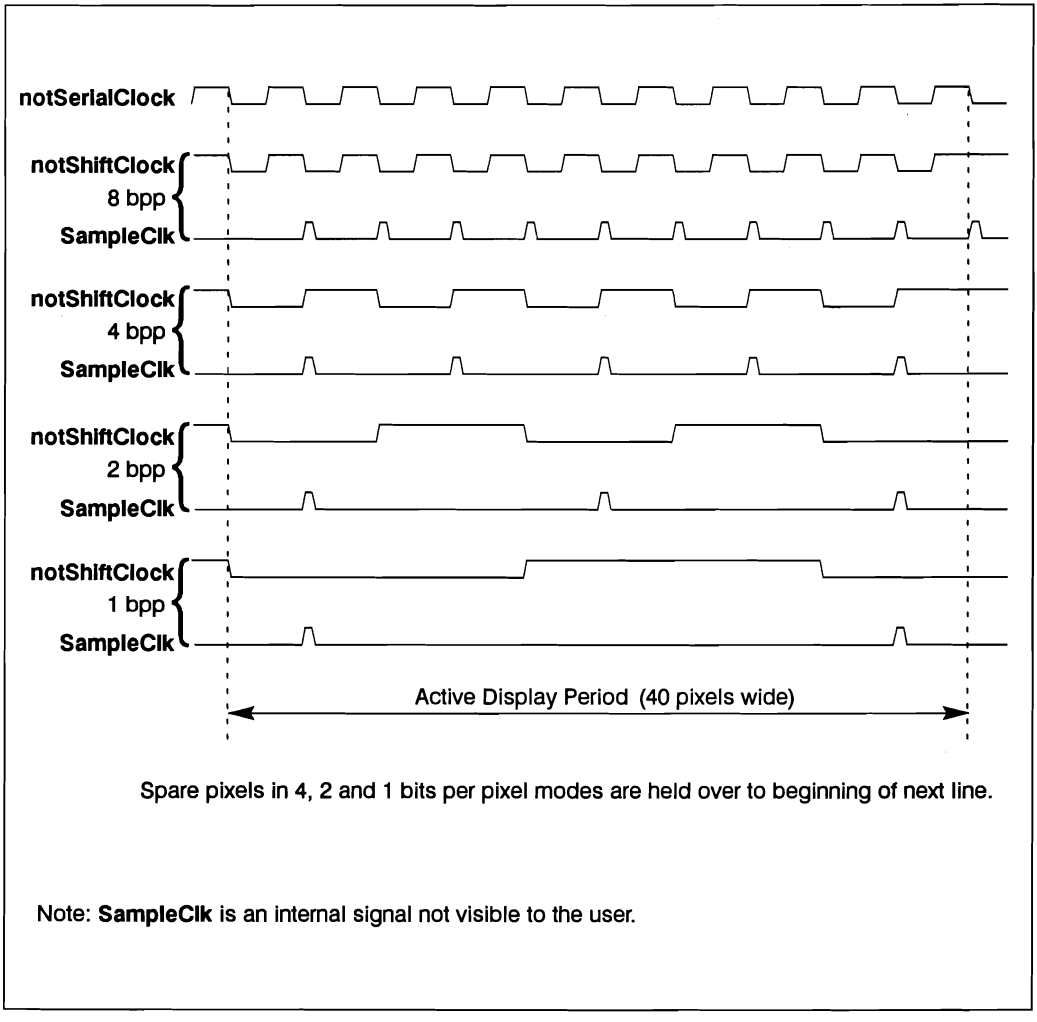


Figure 6.24 Relationship between Serial and Shift Clocks to pixel data in various bits per pixel modes

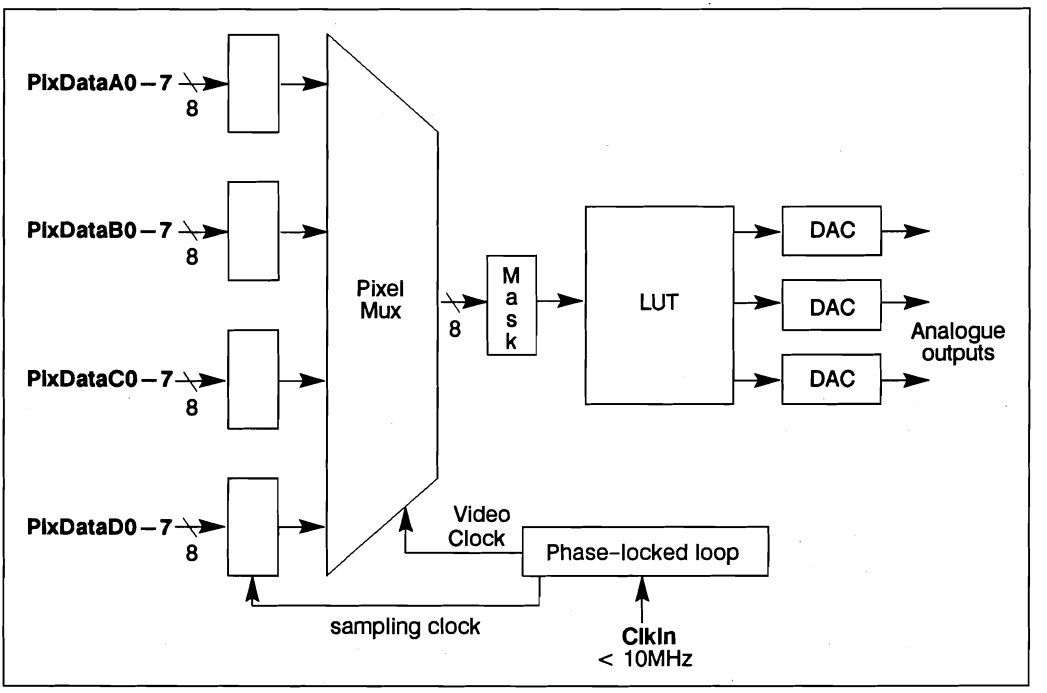


Figure 6.25 Pixel port in mode 1

6.13.3 Mode 2 operation

In mode 2, direct write, pixel inputs are used as three 8-bit addresses into the triple LUT. This allows the use of the full range of up to 16 million colours simultaneously displayed on the screen but requires pixels to be supplied to the G300 at the full video rate.

One 24-bit wide pixel is latched into the G300 on every *rising* edge of the externally supplied pixel clock – **ClkIn**. (The PLL is not used in mode 2.) **PixDataA0-7** feeds the red DAC, **PixDataB0-7** feeds the green DAC and **PixDataC0-7** feeds the blue DAC.

Note that in mode 2, the specified timings for the pixel setup and hold times must be observed, even during flyback, otherwise corruption of the lookup table can occur. Also, the mask register content has no effect on pixel data in mode 2.

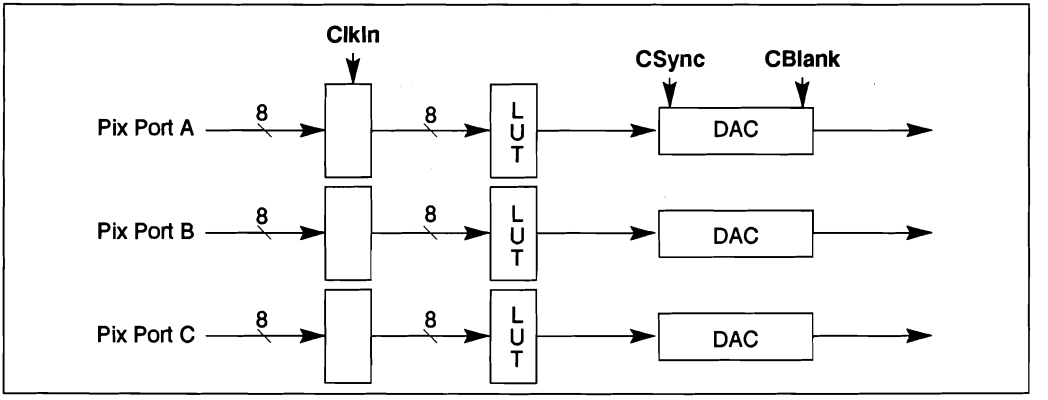


Figure 6.26 Pixel port in mode 2

6.14 The video DACs

6.14.1 General

The video DACs on the G300 have 8-bit resolution at the full video rate. They are designed to drive a doubly terminated 75Ω transmission line and produce analogue video signals compatible with either the RS-170 or RS-343 video standards.

6.14.2 DAC output waveform

The DACs work by sourcing a current proportional to their digital input. The unit current sourced for each digital increment is defined by a reference current drawn from the part using an external current source.

The complete analogue video signal comprises three components as shown in figure 6.27. The current sourced by each component is defined in terms of DACunits. The value of 1 DACunit is set by the reference current drawn from the **Iref** pin:

$$1 \text{ DACunit} = \textbf{Iref}/120$$

The colour information output by each gun ranges from 0 to 255 units under control of the digital input from the colour palette or the pixel port.

A black-level pedestal of 20 DACunits is provided. This extra pedestal distinguishes between a displayed value of intensity 0 during display (ie black) and the 'blacker than black' level present when the electron beam is blanked for flyback. When enabled (by setting the relevant bit in the control register), this extra level is switched on only during the active display time of each line. It is switched off during blanking so as to ensure no visible trace of the beam appears on the screen during this period.

A sync pedestal, again selected using the control register, is provided to allow the superposition of the sync timing signals on the video outputs. When this composite sync option is selected the sync level is added to the output during blanking and active display. Sync pulses are present on all three of the video DACs. The size of the sync pedestal is 108 DAC units.

Table 6.20 defines the value of each of the three components which make up the complete video output current sourced by each DAC.

	Colour Data (Full Scale)	Black Level Pedestal	Sync
units	255	20	108

Table 6.20 DAC output level components

Both the black-level pedestal and the sync signals may be independently turned on or off by setting bits 12 and 5 in the control register respectively.

(Note that the extra blanking pedestal units, if used, add to the full scale deflection so that the current source must be redefined in order to use this mode).

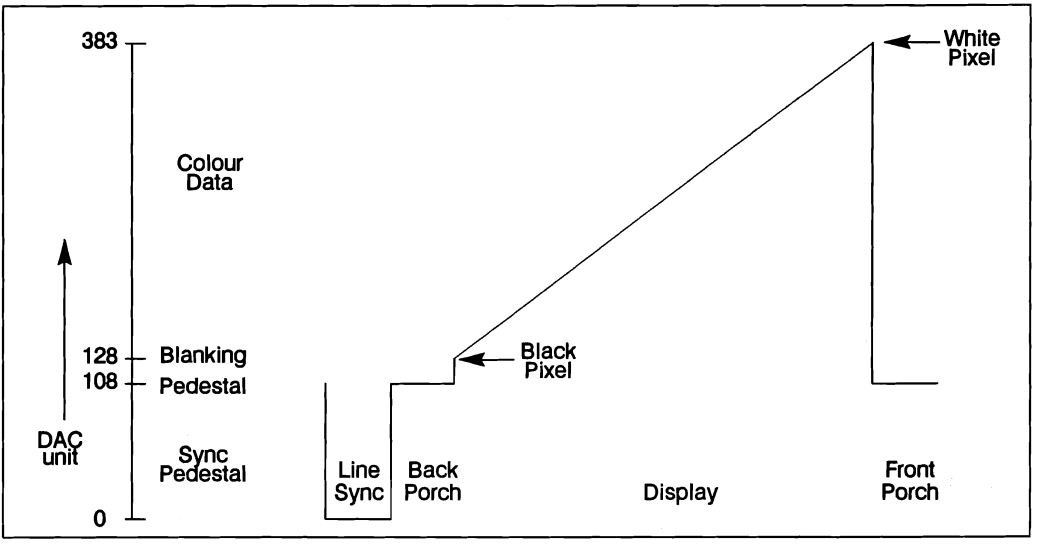


Figure 6.27 DAC output levels

6.14.3 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
	Resolution		8		bits	
VO(max)	Output voltage			1.5	V	2
IO(max)	Output current			32	mA	VO≤1V
	Full scale error			± 5	%	2, 3
	Sync pedestal error			±10	%	2
	Blank level pedestal error			±10	%	2
	DAC to DAC correlation error			± 2.5	%	2, 4
	Integral Linearity error			± 1	LSB	2, 5
	Glitch Energy		75		pVSec	2, 6, 7
IREF	Reference current	7		10	mA	
VREF	Reference voltage	VDD −3V		VDD	Volts	
Note: These figures are not characterised and are subject to change						

Notes

1 All voltages with respect to **Ground** unless specified otherwise.

2 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

3 From the value predicted by the design equation, sync and black level pedestals off.

4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.

5 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

6 Load = 37.5Ω +30 pF with IREF = −8.88mA.

7 This parameter is sampled not 100% tested.

Symbol	Parameter	-66 Max.	-85 Max.	-100 Max.	-110 Max.	Units	Notes
	DAC Risetime	6	6	4	4	ns	1
	DAC Settling time	15.3	11.7	10	9.1	ns	1, 2, 3
Note: These figures are not characterised and are subject to change							

Notes

1 Load = 37.5Ω + 30pF, IREF = −8.88mA.

2 From a 2% change in output voltage until settling to within 2% of the final value.

3 This parameter is sampled not 100% tested.

6.14.4 Power supply and current reference

It is recommended that a high frequency decoupling capacitor (preferably a chip capacitor) in parallel with a larger tantalum capacitor (22μF to 47μF) be placed between **AVDD** and **Ground** to provide the best possible supply to the analogue circuitry of the DACs.

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 6.28 shows four designs of current reference.

In order to ensure the best picture quality, it is recommended that the IMS G300 be soldered directly into the PCB without the use of a socket, since this minimises inductance.

If the board **VDD** supply is very noisy, then it is advisable to provide a quiet supply for just the IMS G300. This may be done by supplying both **VDD** and **AVDD** through a small inductor (1–5μH). This will act as an ac filter for high frequency noise. However, if this is done care should be taken to ensure the power rating of this inductor is not exceded.

Figure 6.28(d) shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 6.28(a)–(c) are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuits 6.28(b) and 6.28(c) the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 6.28(c)).

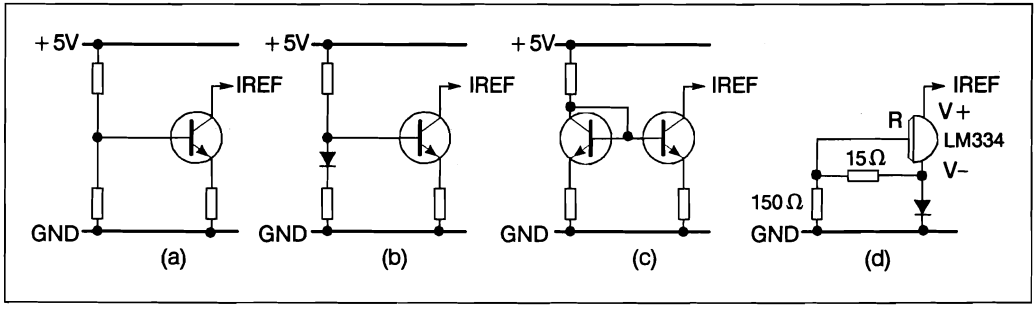


Figure 6.28

6.14.5 Current reference – decoupling

The DACs in the IMS G300 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VDD. This will enable the current reference to track both low and high frequency variations in the supply.

6.14.6 Analogue output – line driving

The G300 is designed to drive a doubly terminated 75Ω line. This arrangement is illustrated in figure 6.29. The effective load seen by the G300 video outputs with this circuit is 37.5Ω.

The connection beteween the DAC outputs on the G300 and the input to the colour monitor should be regarded as a transmission line. Impedance changes along this line will result in reflection of part of the video signal back along the line. These reflections can result in a degradation of the picture displayed by the monitor. To ensure good fidelity RF techniques should be used; in particular the PCB trace from the G300 video output pins to the video sockets on the graphics board should be kept short (less than 3 inches is ideal). If this is done then any reflections due to a mismatched impedance at the video connectors will occur within the risetime of the DAC waveform and will not cause a degradation of the image quality.

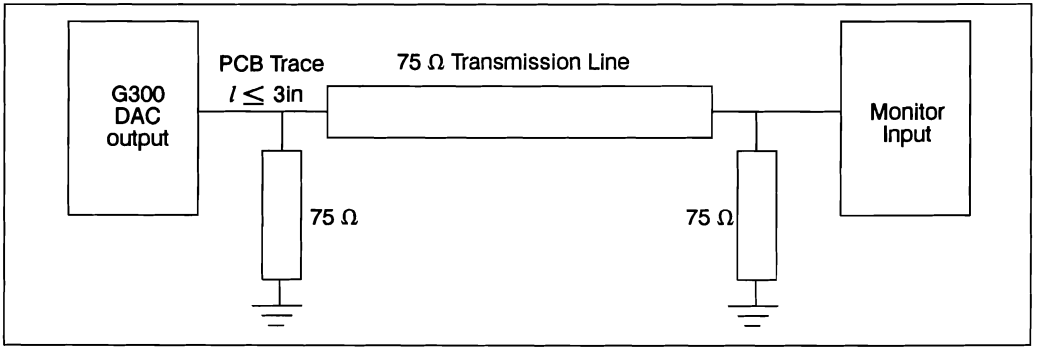


Figure 6.29 DAC output loading

6.14.7 Analogue output – protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G300 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G300 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection diodes to the power rails are recommended at this exposed interface.

6.15 Clock generation and phase locked loop

6.15.1 Introduction

The IMS G300 has two alternate clocking schemes which between them provide a high degree of system flexibility. The primary clocking system uses a phase locked loop on the chip to multiply the low frequency (< 10MHz) input clock up to the required video data rate. This scheme is used only when the part is in mode 1 and contributes to its overall ease of design. A full dot-rate clock is supplied to the **ClkIn** pad for the alternate scheme, which must be used when the IMS G300 is in mode 2 and when mode 1 is to be driven in 'times one' configuration.

6.15.2 ClkIn

When the PLL is to be used, **ClkIn** must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. **ClkIn** must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits. Phase locked loop mode is selected by placing a capacitor between **CapPlus** and **CapMinus**, and then writing a 'one' to the boot location bit 5.

6.15.3 CapPlus, CapMinus

The internally derived power supply for internal clocks requires an external low leakage, low inductance 1 μF capacitor to be connected between **CapPlus** and **CapMinus**. A ceramic capacitor is preferred, with an impedance of less than 3Ω between 100kHz and 10MHz. If a polarised capacitor is used the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm. The connections must not touch power supplies or other noise sources.

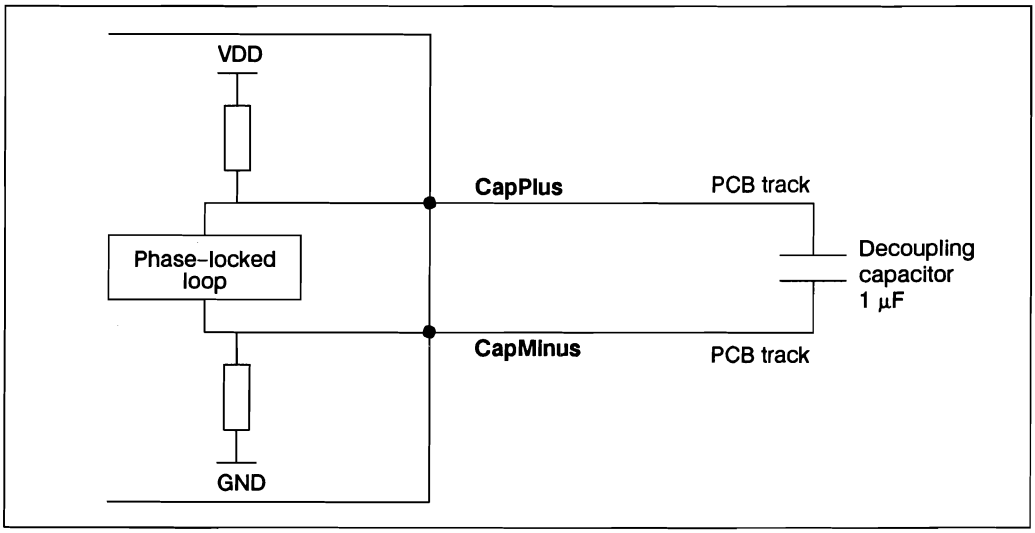


Figure 6.30 Recommended PLL decoupling

6.15.4 Speed selection

The multiplication factor of the phase locked loop is set by writing a binary value to the IMS G300 boot location. This location is enabled for writing by performing a reset cycle. Once it has been written to, another reset must be performed before reprogramming is possible. Only **ADBus**[5:0] are valid as data during these write cycles, in all other respects they conform to the diagrams given in section 6.12. Although all possible multiplication factors will work with all permissible input frequencies up to the speed rating of the

part, the quoted figures are guaranteed only if the recommended combinations are adhered to. The multiplication factor selected is the binary number written to the boot location bits[4:0].

6.15.5 Recommended input clock and multiplication factors

Intermediate video data frequencies can be produced by choosing the multiplication factor for the quoted frequency closest to that desired and varying the input clock frequency to achieve the correct value. Clock multiplication factors less than 5 are not allowed.

It is possible to produce the full range of frequencies from a 5 MHz input clock (in steps of 5 MHz) but the PLL will be more susceptible to power supply noise and clock input jitter when a very high multiplication factor is used.

Parameter	Min.	Max.
Input frequency	5MHz	10MHz
Multiplication factor	5	31*

*Subject to speed rating of device.

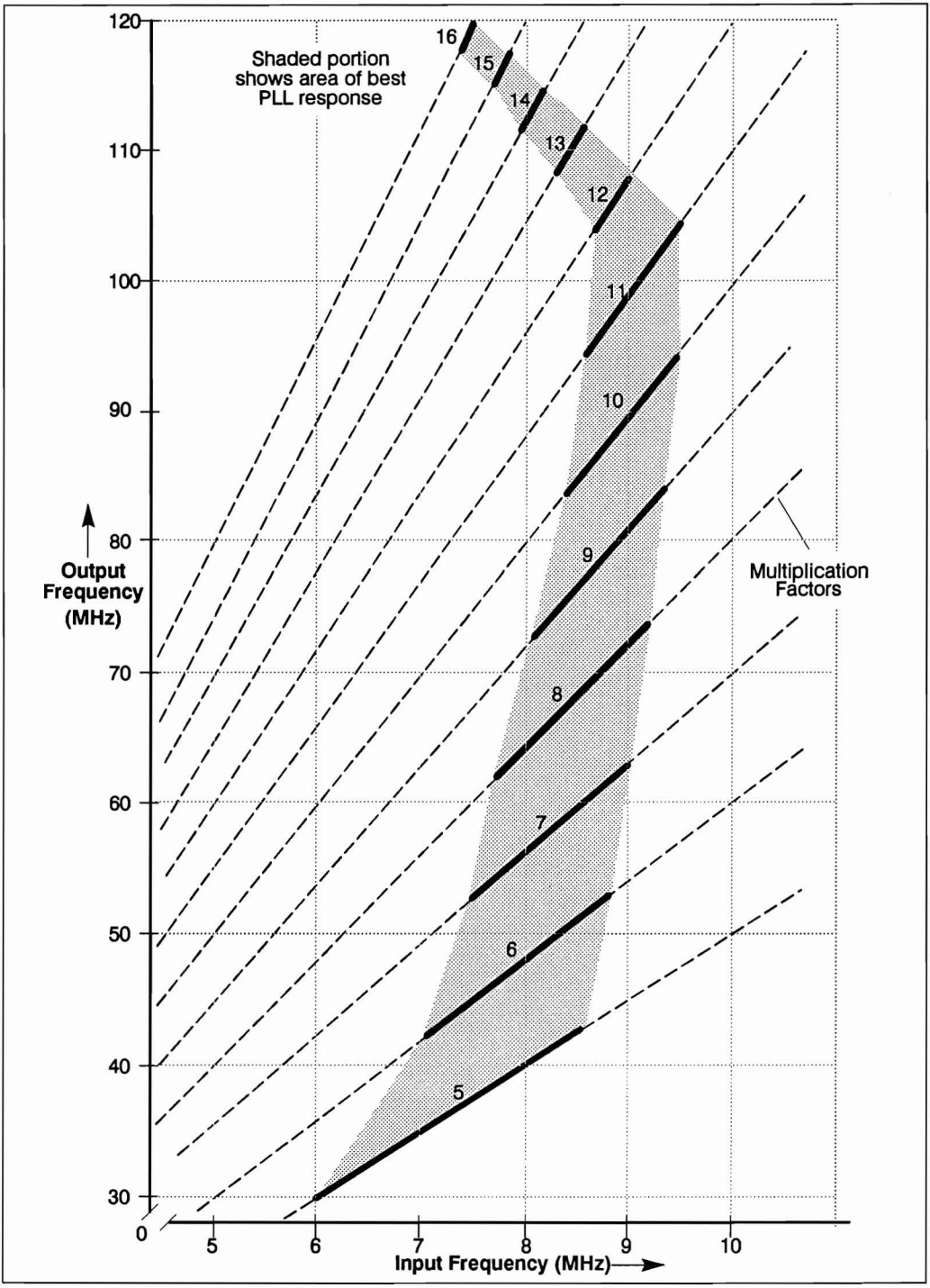


Figure 6.31 Best multiplier settings for G300 PLL

6.16 Package specifications

6.16.1 84 pin grid array package

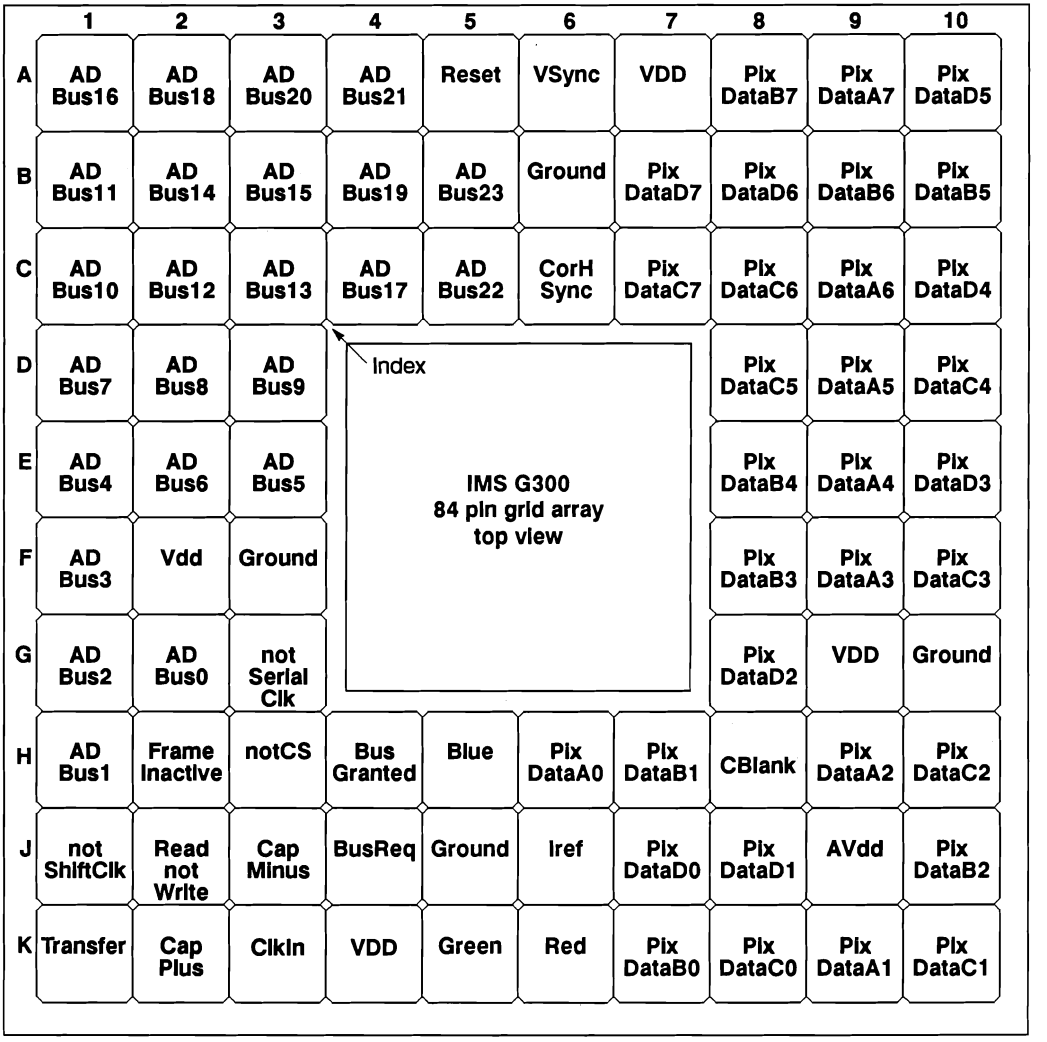


Figure 6.32 IMS G300 pin configuration

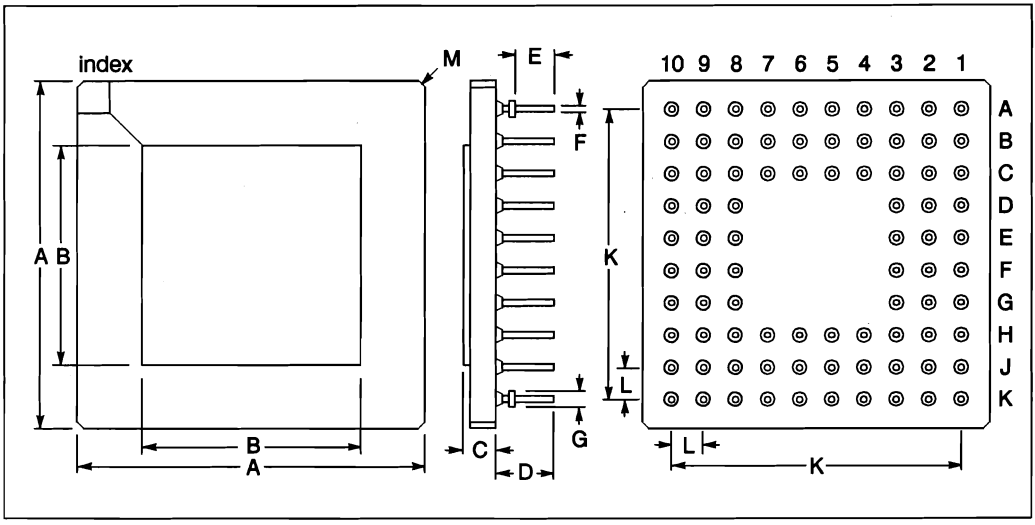


Figure 6.33 84 pin grid array package dimensions

	Millimetres		Inches		
DIM	NOM	TOL	NOM	TOL	Notes
A	26.924	±0.254	1.060	±0.010	
B	17.019	±0.127	0.670	±0.005	
C	2.456	±0.278	0.097	±0.011	
D	4.572	±0.127	0.180	±0.005	
E	3.302	±0.127	0.130	±0.005	
F	0.457	±0.025	0.018	±0.001	Pin diameter
G	1.143	±0.127	0.045	±0.005	Flange diameter
K	22.860	±0.127	0.900	±0.005	
L	2.540	±0.127	0.100	±0.005	
M	0.508		0.020		Chamfer
Package weight is approximately 7.2 grams					

Table 6.21 84 pin grid array package dimensions

6.16.2 100 pin ceramic quad flatpack package

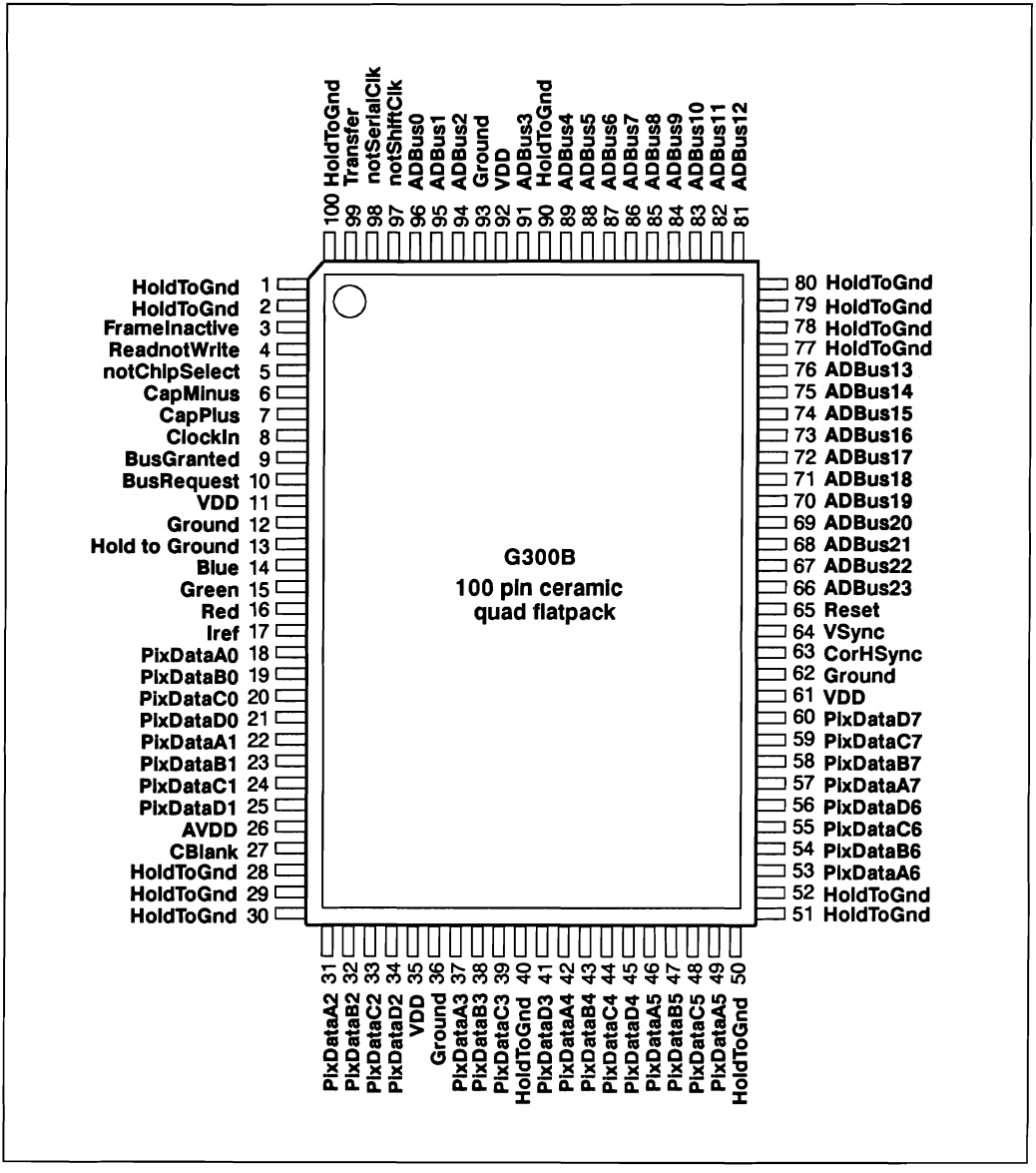


Figure 6.34 IMS G300 pin configuration

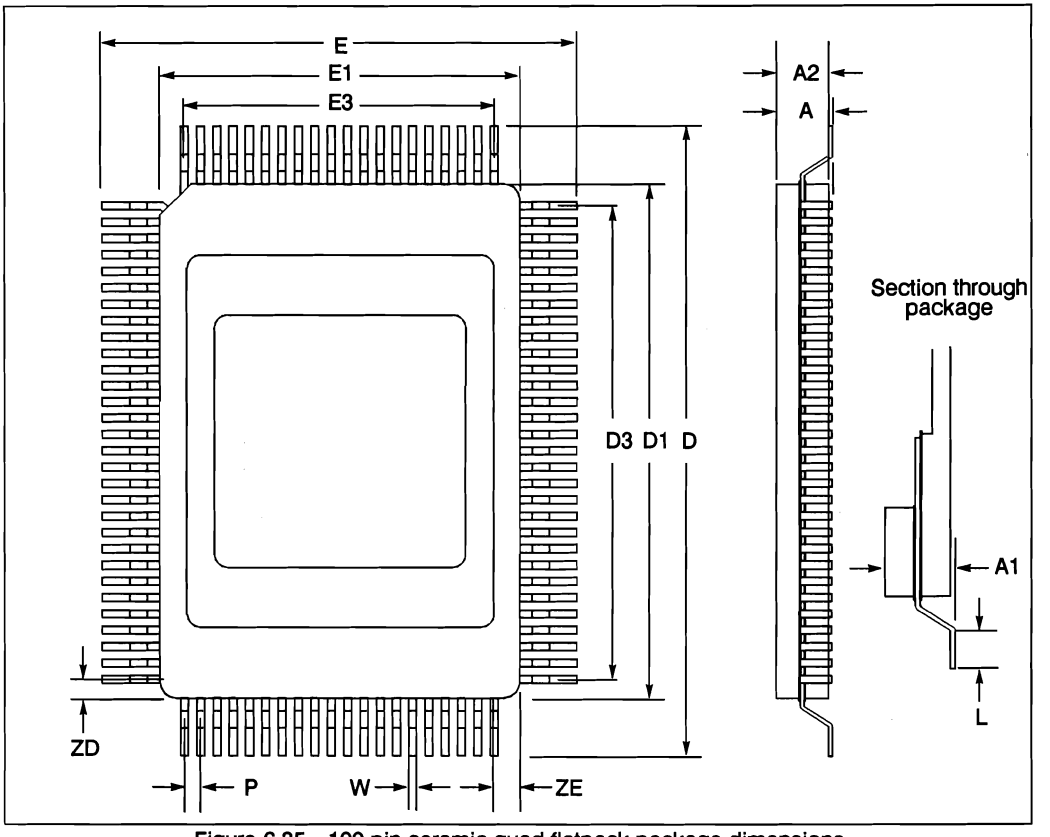


Figure 6.35 100 pin ceramic quad flatpack package dimensions

Dim	Millimetres			Inches			Notes
	Min	Nom	Max	Min	Nom	Max	
A			3.300			0.130	
A1	0.000		0.250	0.000		0.010	
A2	2.550	2.800	3.050	0.100	0.110	0.120	
D	23.650	23.900	24.150	0.931	0.941	0.951	
D1	19.900	20.000	20.100	0.783	0.787	0.791	
D3		18.850			0.742		Ref.
ZD		0.580			0.023		Ref.
E	17.650	17.900	18.150	0.695	0.705	0.715	
E1	13.900	14.000	14.100	0.547	0.551	0.555	
E3		12.350			0.486		Ref.
ZE		0.830			0.033		Ref.
L	0.650	0.800	0.950	0.026	0.031	0.037	
P		0.650			0.026		BSC
W	0.220		0.380	0.087		0.015	

Table 6.22 100 pin ceramic quad flatpack package dimensions

6.16.3 Ordering information

Device	Clock rate	Package	Part number
IMS G300	66 MHz	84 pin PGA	IMS G300G-66S
IMS G300	85 MHz	84 pin PGA	IMS G300G-85S
IMS G300	100 MHz	84 pin PGA	IMS G300G-10S
IMS G300	110 MHz	84 pin PGA	IMS G300G-11S
IMS G300	66 MHz	100 pin ceramic quad flatpack	IMS G300F-66S
IMS G300	85 MHz	100 pin ceramic quad flatpack	IMS G300F-85S
IMS G300	100 MHz	100 pin ceramic quad flatpack	IMS G300F-10S
IMS G300	110 MHz	100 pin ceramic quad flatpack	IMS G300F-11S
Note: PQFP for this device is currently under development			

6.17 Programming example for Hitachi HM-4219/4119 monitor

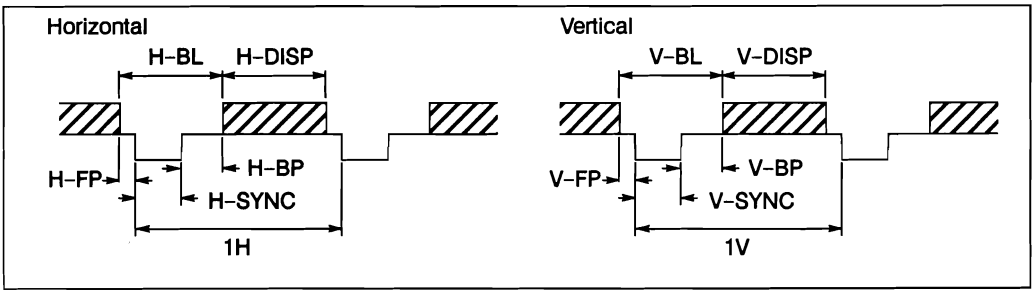


Figure 6.36 Hitachi HM-42/4119 timing

	Item	Equation	Rating (64kHz Version)	Unit
a	Resolution H		1280	Pixel
b	Resolution V		1024	Pixel
c	Pixel rate		9.296	ns
d	Pixel frequency	1 / c	107.573	MHz
e	H-DISP	a x c	11.899	µs
f	H-BL	g + h + i	3.800	µs
g	H-FP		0.200	µs
h	H-SYNC		1.600	µs
i	H-BP		2.000	µs
j	1H		15.699	µs
k	H frequency	1 / j	63.7	kHz
l	V-DISP	b x j	(1024H)	ms
m	V-BL*	n + o + p	(37H)	ms
n	V-FP		(0H)	ms
o	V-SYNC		(3H)	ms
p	V-BP*		(34H)	ms
q	1V	l + m	(1601H)	ms
r	V frequency	1 / q	60.0	Hz

Table 6.23 Recommended timings for monitor (64kHz version)

* Note: These parameters do not map directly to CVC register values.

6.17.1 Calculation of parameters

At the recommended pixel rate of 9.296ns,

screen unit = 4 x 9.296ns = 37.184ns

All line timing parameters are calculated as multiples of this figure.

Line Scan period

$$\text{Linetime} = 15.699\mu s / 37.184ns = 422.19$$

$$\text{so set Linetime} = 422$$

This obeys the rule associated with the Linetime parameter; that it should be an even number of screen units.

If it is absolutely necessary to meet the recommended linescan frequency then it is best to specify the input clock frequency as the variable but, in practice, all monitors will synchronise to a close approximation.

Line sync pulse

The G300 constructs this from two halfsync periods so:

$$\text{Halfsync} = 1.6\mu s / (2 \times 37.184ns) = 21.5$$
$$\text{so set Halfsync} = 21 \text{ screen units}$$

Backporch

$$\text{Backporch} = 2\mu s / 37.184ns = 53.7$$
$$\text{so set Backporch} = 54 \text{ screen units}$$

Display

This parameter is set in terms of the number of pixels you wish to display so in this case:

$$\text{Display} = 1280 / 4 = 320 \text{ screen units.}$$

Frontporch

There is no explicit frontporch parameter; this period being implied as the difference between the sum of the other parameters and the linetime period.

$$\begin{aligned}\text{Frontporch} &= \text{Linetime} - ((\text{Halfsync} \times 2) + \text{Backporch} + \text{Display}) \\ &= 422 - (21 \times 2 + 54 + 320) \\ &= 6 \text{ screen units} \\ &= 6 \times 37.184 \text{ ns} = 0.223 \mu s\end{aligned}$$

Which compares with the monitor requirement of 0.2 μs.

The 'halfline point' rule is obeyed by these timings since:

$$(\text{HalfSync} \times 2) + \text{Backporch} + \text{Display} < \text{Linetime} / 2 > (\text{HalfSync} \times 2) + \text{Backporch}$$

In a non interlaced system such as this the remaining two line parameters are actually used only during frame flyback in order to count in multiples of half a line time. In an interlaced system, the parameter Short-display is used to construct the short displayed lines at top and bottom of the screen if the total number of displayed lines is odd. BroadPulse is used to produce the low pulses in a tesselated frame sync period. Both of these parameters must always be programmed whether or not your system explicitly uses them.

ShortDisplay

$$\begin{aligned} \text{Shortdisplay} &= (\text{Linetime} / 2) - [(\text{HalfSync} \times 2) + \text{Backporch} + \text{Frontporch}] \\ &= 211 - (42 + 54 + 6) \\ &= 109 \text{ screen units} \end{aligned}$$

$$\begin{aligned} \text{BroadPulse} &= (\text{Linetime} / 2) - \text{Frontporch} \\ &= 211 - 6 \\ &= 205 \text{ screen units} \end{aligned}$$

Frame timing parameters

All frame timings are specified in terms of half line times.

Number of Displayed lines is 1024

$$\text{VDisplay} = 1024 \times 2 = 2048$$

Which complies with the requirement that each frame must contain an even number of half lines.

The G300 produces frame flyback waveforms in accordance with the broadcast standards which means that:

$$\text{VSync} = \text{PreEqualisation} = \text{PostEqualisation}$$
$$\text{VSync} = 6$$

Total Blanked period is 37H so :

$$\text{VBlank} = 74 - (6 \times 3) = 56$$

Which is a whole number of lines.

HalfSync	=	21
BackPorch	=	54
Display	=	320
LineTime	=	422
ShortDisplay	=	109
BroadPulse	=	205
VSync	=	6
VBlank	=	56
VDisplay	=	2048

The remaining three parameters are concerned with management of the video RAM bitmap. Assuming that 256K video RAMs are being used, the shift register length will be 256 bits. The sum of the parameters MemInit and TransferDelay must not exceed this figure unless some external form of multiplexing is used which generates an effective register length greater than this. It is possible to use parameters which total less than 256 in order to implement a hardware pan function, but for the purpose of this example, we will assume that all of the bitmap is to be displayed. Thus:

$$\text{Meminit} + \text{TransferDelay} = 256$$

Transfer delay is

$$\text{System DMA latency} + \text{VRAM access time} + 3 \text{ Screen units}$$

Assume DMA latency to be around 500ns and the VRAM access time to be 100ns then:

$$\begin{aligned}\text{TransferDelay} &= 600\text{ns} / 37.184\text{ns} + 1 = 17.13 \\ &= 20 \text{ screen units}\end{aligned}$$

Which obeys the conditions for TransferDelay that:

$$\begin{aligned}\text{TransferDelay} &< \text{Backporch} \\ \text{TransferDelay} &< \text{ShortDisplay}\end{aligned}$$

(These are the only screen related limitations on the value of the VRAM management parameters)

$$\text{MemInit} = 256 - 20 = 236 \text{ screen units.}$$

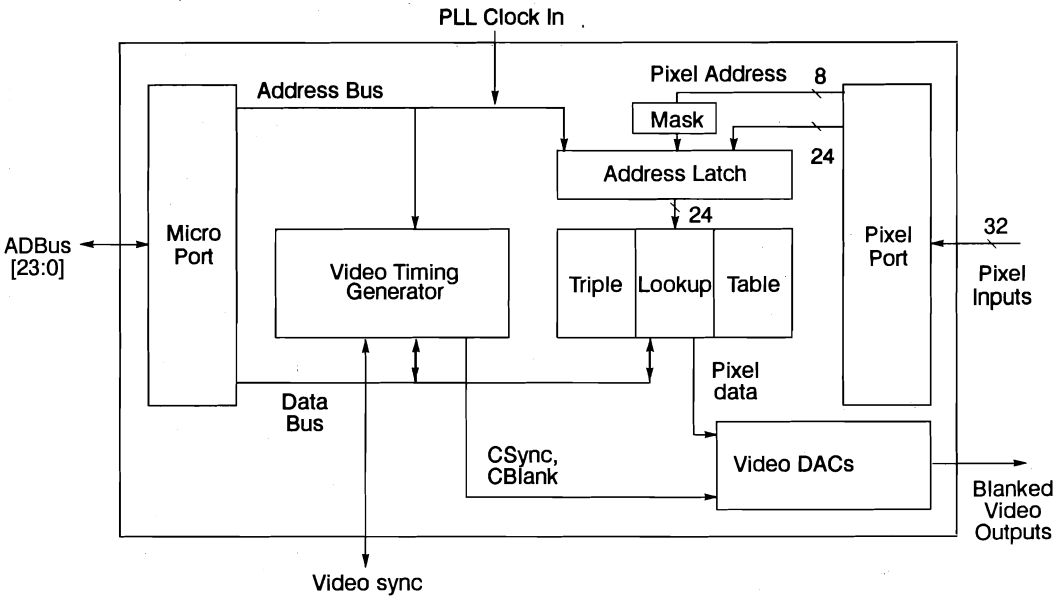
LineStart is the top of screen pointer and it can be programmed to any value but with the following restrictions.

If the bitmap is to appear byte-linear to the processor, the SAM start address must be zero.

The SAM start address must never become greater than (256 − TransferDelay)

IMS G300C
colour video controller

Preliminary data



FEATURES

Video rates up to 110 MHz
Software configurable video timing generator
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

Variable multiplexed Pixel input
1, 2, 4, 8 and 24 bit pixels
On chip triple lookup table
Triple high speed 8 bit video DACs
CCIR and EIA 343-A compatible
Full colour mode with hardware gamma translation

General purpose Video RAM support
Synchronous VRAM Data Transfer strobing
Video RAM Row address auto-increment
Screen width independent of VRAM architecture
On-chip phase-locked loop (PLL)
All external signals and clocks at 1/4 video rate

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

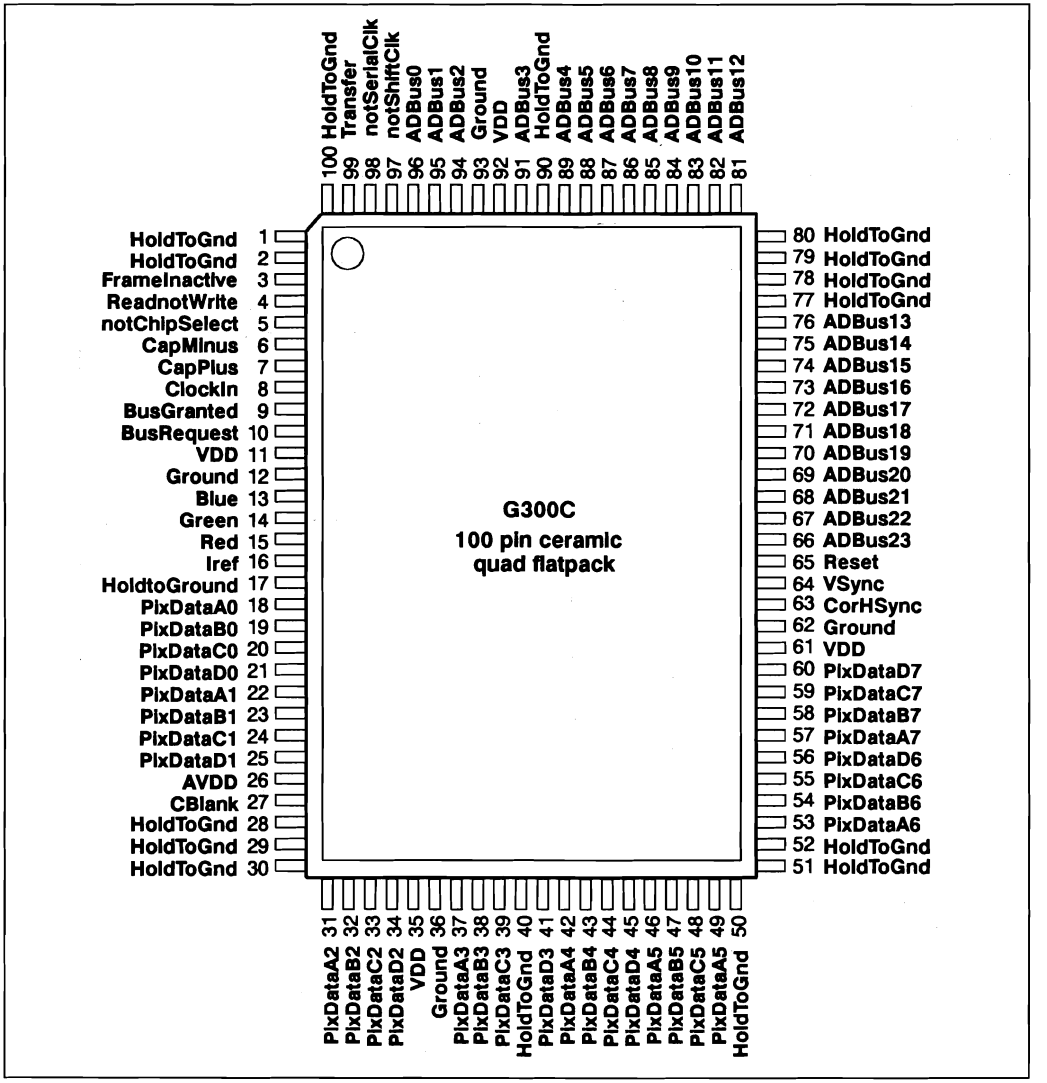
42 1469 00

July 1990

Analog performance of the IMS G300 package

With very high edge rates into the **PixData** pins of the IMS G300, there is a significant coupling between **PixDataA0** and **Iref** on both the Pin Grid Array (PGA) and Ceramic Quad Flat Pack (CQFP) packages. In order to remove this problem the IMS G300C is offered with an internally modified PGA package with no change to the pinout. In the CQFP version the pinout has been changed to conform to the diagram below. This diagram replaces figure 6.34 in the IMS G300B datasheet.

For both package variants the change introduces a grounded screen between the **PixData** pins and **Iref** – eliminating the problem.



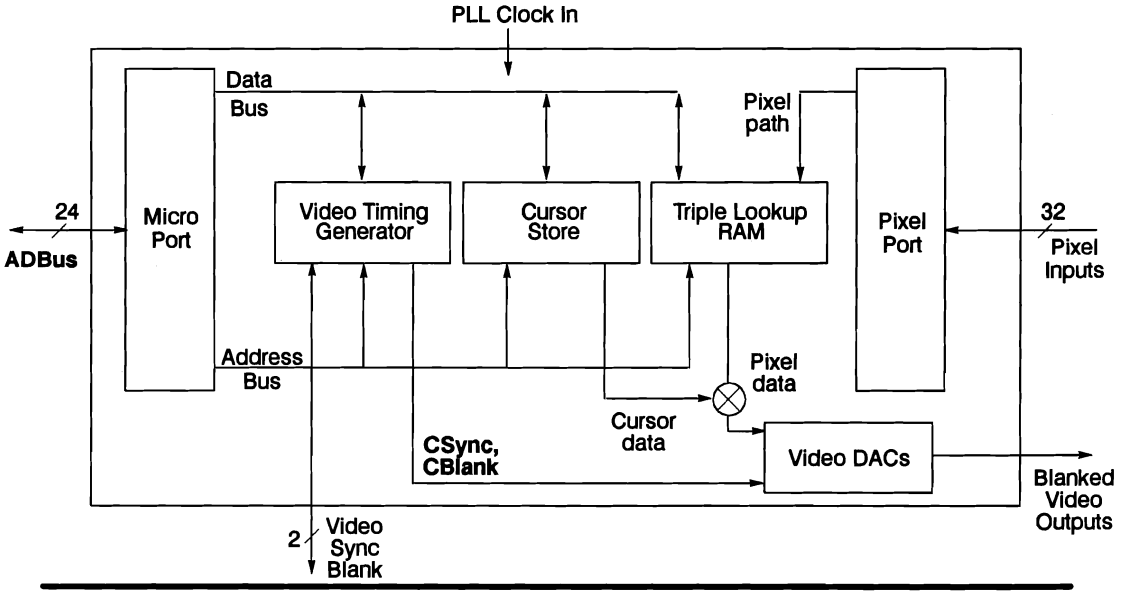
IMS G300C 100 pin ceramic quad flatpack pin configuration

NOTE! In all other respects the G300B and G300C are identical.

For future designs use IMS G300C revision. Unless IMS G300B revision is specified when ordering, the IMS G300C revision will be shipped. The IMS G300B revision will eventually be discontinued. The IMS G300B is marked as the IMS G300 and the IMS G300C will be marked as the IMS G300C.

IMS G332
colour video controller

Preliminary data



FEATURES

Video rates up to 110 MHz, (135MHz available 1991)
Software configurable video timing generator
64×64×3 colour hardware cursor
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

Variable multiplexed pixel input
1, 2, 4 and 8 bit pseudo colour pixels
15 or 16 bits per pixel gamma corrected colour
On chip triple lookup table with anti-sparkle
Triple high speed 8 bit video DACs
CCIR and EIA 343-A compatible

General purpose Video RAM support
Synchronous VRAM Data Transfer strobing
Video RAM Row address auto-increment
Screen width independent of VRAM architecture
On-chip phase-locked loop (PLL)

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

7.1 Introduction

The IMS G332 provides all the necessary functions to control real-time operation of a raster scan video display, using dual-ported video RAMs.

The device consists of a 32 bit variable multiplexed pixel interface, a programmable video timing generator (VTG), a 256 location colour lookup RAM (LUT) with variable addressing modes, triple 8 bit video DACs, a 64×64×2 bit cursor store and 3 location cursor LUT, a programmable cursor positioning/insertion controller, a video memory control system and phase-locked loop clock generator.

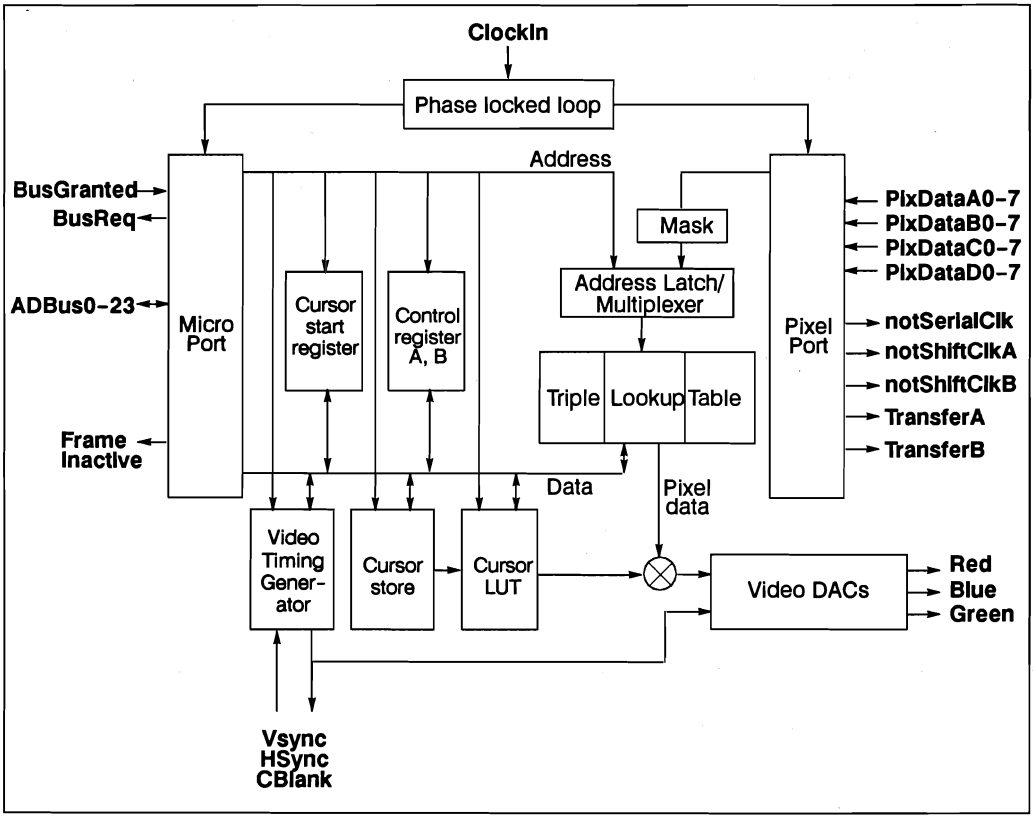


Figure 7.1 IMS G332 Block Diagram

7.2 Pin function reference guide

7.2.1 Micro port

Pin name	I/O	Page No.	Comments
FrameInactive	O	158	Timing signal which is high during vertical blanking.
BusReq **BusGranted**	O I	157	DMA control signals used in conjunction with **TransferA** and **TransferB** when refreshing the VRAM shift registers.
ReadnotWrite **notOutputEnable** **notChipSelect** **Wait**	I I I O	156	Microport control signals. Wait is used to extend cycle times if necessary.
ADBus0-23	I/O	156	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied either on **ADBus2-11** or on **ADBus3-12** depending on the word width.The port is also used to drive out the 24 bit VRAM transfer address.

7.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk	O	159	**notSerialClk** runs at one quarter the video frequency. This signal must be buffered
notShiftClkA **notShiftClkB**	O O	159	VRAM clocks running under the control of the timing generator. The clocks run in anti-phase in interleaved mode; only **notShiftClkA** runs in non-interleaved mode. These clocks must be buffered.
TransferA **TransferB**	O O	157	VRAM shift register transfer strobes. TransferA and B are synchronised to **notShiftClkA** and **notShiftClkB** respectively.
CBlank	I/O	150	**CBlank** is a composite blanking pin. Direction is soft selectable.
PixDataA0-7 **PixDataB0-7** **PixDataC0-7** **PixDataD0-7**	I I I I	159	Pixel input ports A – D. Port A is least significant; port D is most significant. Internally, pixel data is latched synchronous to **notSerialClk.**

7.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	154	Active high, must be held active with clocks running for at least 500ns.

7.3 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus **CapMinus**	N/A	162	Phase locked loop decoupling pins, also used to select external dot rate clock source by connecting **CapPlus** to **CapMinus**.
ClockIn	I	162	Clock input for both PLL and times-one operation.

7.3.1 Video signals

Pin name	I/O	Page No.	Comments
Red **Green** **Blue**	O O O	159, 163	Blanked video outputs. Drive into doubly terminated 75Ω load.
Iref	I	163	Video DAC reference current.
notVSync **notCorHSync**	I/O I/O	155	Digital sync signals for system synchronisation. They are inputs in slave mode and outputs in master mode. They are soft configurable.

7.3.2 Supplies

Pin name	I/O	Page No.	Comments
AVDD **AGND**	N/A N/A	164	**AVDD/AGND** supplies analogue portions of chip.
VDD	N/A	164	**VDD/GND** supplies digital portions of chip.
GND	N/A		

7.4 Register function reference guide

Register	Address	Page No.	Comments
Boot Location	#X000	146	Startup location to which must be written the clock multiplication factor, whether PLL or ×1 mode, and the 32/64 bit address alignment selection.
Datapath Registers	#X021 to #X02E	144	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Mask Register	#X040	160	24 bit pixel address mask register. Read/write accessible at all times. (Operates only on pseudo colour pixels)
Control Registers	#X060 and #X070	145	Read/write control registers contains configuration information. Unassigned bits must be written with zero and are not valid on read. Read/write accessible at all times.
Top of Screen	#X080		Read/write register giving ability to reprogram the top of screen pointer at any time.
Cursor palette	#X0A1 to #X0A3	161	3×24 bit cursor colour registers. Read or write accessible at all times.
Checksum registers	#X0C0 to #X0C2	161	RGB frame checksums.
Colour Palette	#X100 to #X1FF	160	256 locations of 24 bit colours read/write accessible at all times.
Cursor store	#X200 to #X3FF	161	512 locations of 16 bit words, each containing 8 packed 2-bit pixel colour values.
Cursor position	#X0C7	161	24 bit register storing the x-y position of the cursor.

All other addresses in the range are reserved and must not be written to.

Note: #X = Hexadecimal address.

Word addresses are user-selectable to align with 64-bit or 32-bit words. In 32 bit mode, addresses must be supplied on **ADBus2-11**; in 64 bit mode they must be supplied on **ADBus3-12**. The addresses given above must be multiplied by the appropriate scale factor (4 in 32 bit mode, 8 in 64 bit mode) to obtain the corresponding byte addresses.

7.5 Datapath register allocation

Register	Address	Units	Notes
Half sync	#X021	Screen units	1
Back porch	#X022	Screen units	
Display	#X023	Screen units	
ShortDisplay	#X024	Screen units	
BroadPulse	#X025	Screen units	
VSync	#X026	Half lines	
VPreEqualise	#X027	Half lines	
VPostEqualise	#X028	Half lines	
VBlank	#X029	Half lines	
VDisplay	#X02A	Half lines	
LineTime	#X02B	Screen units	
Line Start	#X02C	Screen units	
MemInit	#X02D	Screen units	
TransferDelay	#X02E	Screen units	2

Notes

1 1 screen unit = 4 pixels horizontally = 1 Serial Clock period.

2 Transfer Delay equates to a real time, and the value will therefore depend on the serial clock period.

7.6 The control registers and boot location

There is provision for two 24-bit control registers, one of which is initially populated.

Bit	Function	Comments
0	Enable VTG	0 = VTG disabled 1 = VTG enabled
1	Screen format	0 = non-interlaced 1 = interlaced
2	Interlace standard	0 = EIA format 1 = CCIR format
3	Operating mode	0 = master mode 1 = slave mode
4	Frame flyback pattern	0 = tesselated sync 1 = plain sync
5	Digital sync format	0 = composite sync 1 = separate sync
6	Analogue video format	0 = composite video + sync 1 = video only
7	Blank level	0 = no blank pedestal 1 = blanking pedestal
8	Blank I/O	0 = CBlank is input 1 = CBlank is output
9	Blank function switch	0 = delayed CBlank at pad 1 = Undelayed ClkDisable, at pad
10	Force blanking (irrespective of bit 11)	0 = no action 1 = screen blanked
11	Turn off blanking	0 = blanking enabled 1 = blanking disabled
12-13	VRAM address increment	see definition (section 7.10.5)
14	Turn off DMA	0 = DMAs enabled 1 = DMAs disabled
15-17	Sync delay	Delays sync and blank by 0 - 7 VTG clock cycles
18	Pixel port interleaving	0 = non-interleaved 1 = interleaved
19	Delayed sampling	see definition (section 7.11.2)
20-22	Bits per pixel	see definition (section 7.11.3)
23	Cursor disable	0 = cursor enabled 1 = cursor disabled

Table 7.1 Control register A bit allocations (Address #X060)

Bit	Function	Comments
0-23	All bits reserved	Write zero

Table 7.2 Control register B bit allocations (Address #X070)

Bit	Function	Comments
0–4	PLL multiplier	Binary coded PLL multiplication factor
5	Clock source select	0 = external (×1) clock 1 = PLL clock
6	Micro port address alignment	0 = 32 bit 1 = 64 bit
7–23	Reserved	Write zero

Table 7.3 Boot location bit allocations (Address #X000)

The boot location must be written on power-up before attempting to access any other locations from the micro port. The timing of this first cycle is asynchronous; the value substituted for the serial clock period in the timing parameters should be the minimum allowable for that device see table 7.8

7.7 Micro port timing reference guide

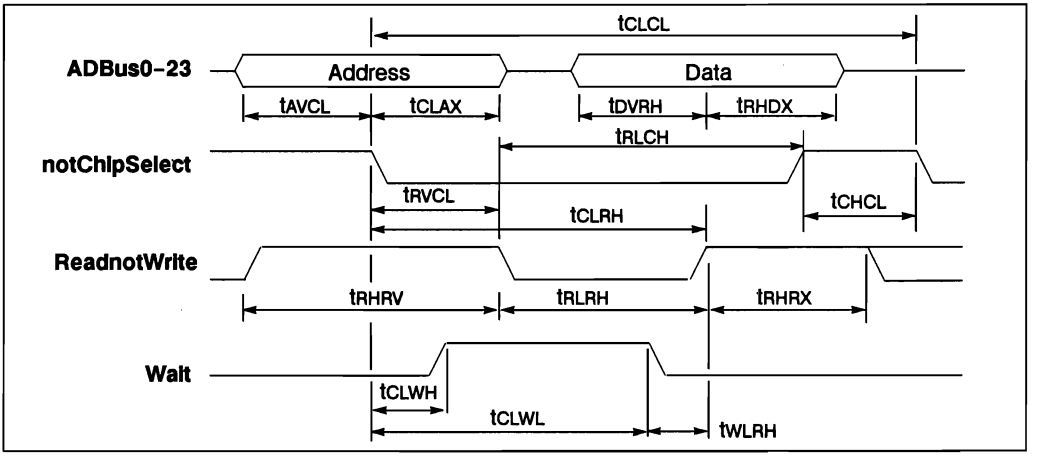


Figure 7.2 Micro port write cycle

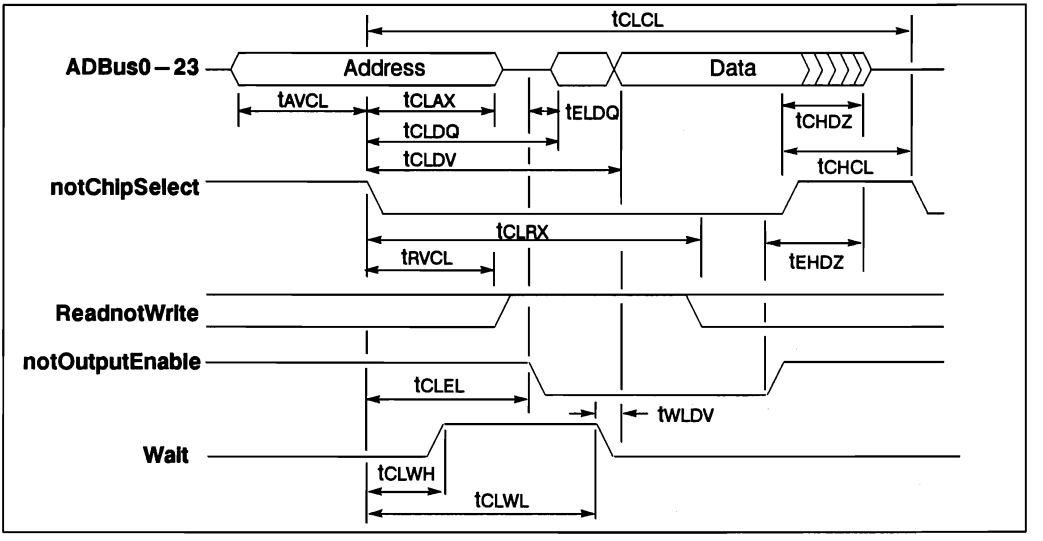


Figure 7.3 Micro port read cycle

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	20		ns
tCLAX	Address hold time	10		ns
tRVCL	**ReadnotWrite** setup time	-1		periods SClk
tCLRH	**ReadnotWrite** hold time	3		periods SClk
tRLRH	**ReadnotWrite** low time	2		periods SClk
tRLCH	**ReadnotWrite** low to **notChipSelect** high	2		periods SClk
tDVRH	Write data setup time	20		ns
tRHDX	Write data hold time	10		ns
tCLCL	Cycle time	4		periods SClk
tCLWH	**notChipSelect** low to wait high	0	20	ns
tCLWL	**notChipSelect** low to wait low	3		periods SClk
tWLRH	**ReadnotWrite** hold time	0		ns
tRHRX	**ReadnotWrite** high time	1		periods SClk
tCHCL	**notChipSelect** high time	2		periods SClk
Note: These figures are not characterised and are subject to change				

Table 7.4 Micro port write cycle parameters

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	20		ns
tCLAX	Address hold time	10		ns
tRVCL	**ReadnotWrite** setup time	-1		periods SClk
tCLRX	**ReadnotWrite** hold time	3		periods SClk
tCHDZ	Output hold time from **notChipSelect**	5	20	ns
tELDQ	Output turn on delay		20	ns
tEHDZ	Output hold time from **notOutputEnable**	5	20	ns
tCLEL	**notChipselect** to **OutptEnable** delay	20		ns
tCLDV	**notChipselect** access time		4 SClk + 10	ns
tCLCL	Cycle time	7		periods SClk
tCLWH	**notChipSelect** low to wait high	0	20	ns
tCLWL	**notChipSelect** low to wait low	4 SClk + 10		ns
tWLDV	Wait to data valid		10	ns
tCHCL	**notCS** high time	2		periods SClk
Note: These figures are not characterised and are subject to change				

Table 7.5 Micro port read cycle parameters

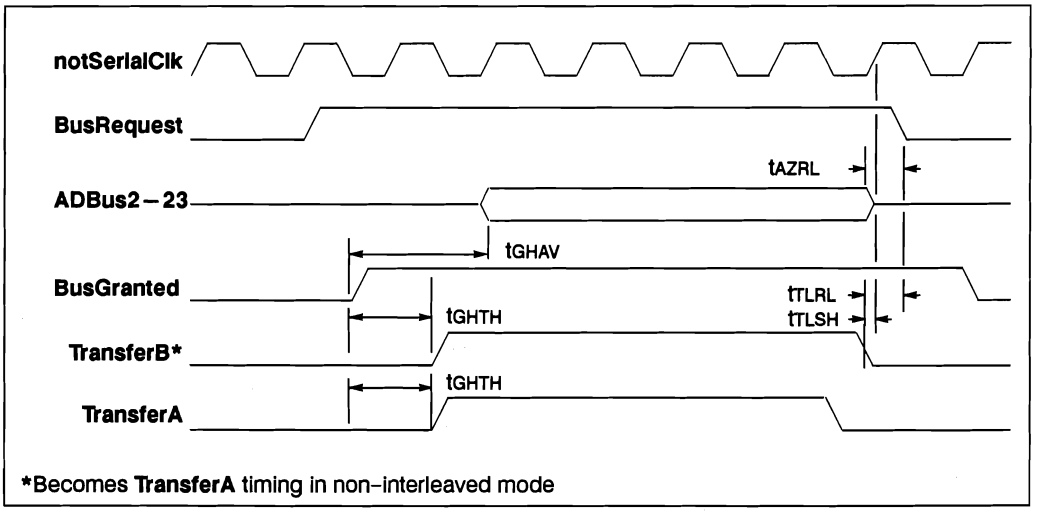


Figure 7.4 Micro port DMA and data transfer timings

Symbol	Description	Min.	Max.	Unit
tSHRH	**notSerialClk** to **BusRequest** skew	-5	5	ns
tGHTH	**BusGranted** high to **Transfer** high	15	30	ns
tGHAQ	**Transfer** address turn on delay	15		ns
tGHAV	**Transfer** address access time		4 SClk + 15	ns
tTLSH	**Transfer** to **notSerialClk** skew	-5	5	ns
tTLRL	**Transfer** to **BusRequest** low	1 SClk	1 SClk + 15	ns
tTLAZ	**Transfer** address hold time	0		ns
tRLCL	**BusRequest** low to **Chipselect** low	0		ns
tAZRL	Address hi-Z to **BusRequest** low	1 SClk-10		ns
Note: These figures are not characterised and are subject to change				

Table 7.6 Micro port DMA and transfer timing parameters

Symbol	Description	Min.	Max.	Unit
tΔSync	**VSync** to **CSync** skew	-5	5	ns
tΔASync	Digital **CSync** to analogue **CSync** skew	TBD	TBD	ns
tΔABlank	Digital **CBlank** to analogue **CBlank** skew	TBD	TBD	ns
Note: These figures are not characterised and are subject to change				

Table 7.7 Micro port **Sync** and **Blank** timing parameters

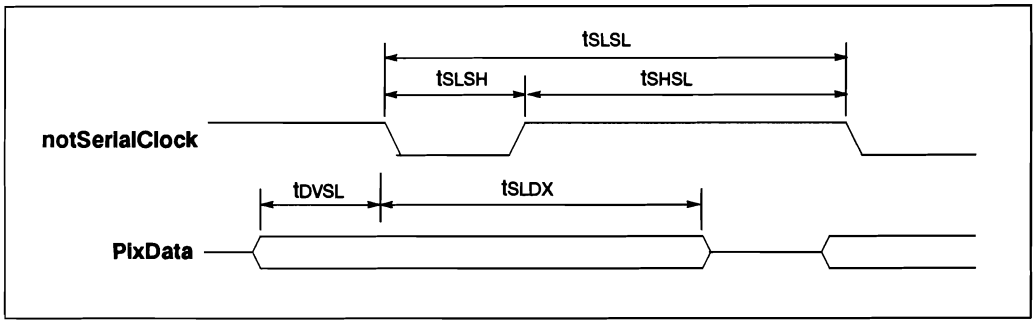


Figure 7.5 Pixel port timing diagram

Symbol	Description	-66	-85	-100	-110	Unit
tSLSL	**notSerialClk** period	61	47	40	36	ns
tSLSH	**notSerialClk** low time	10	10	10	10	ns
tSHSL	**notSerialClk** high time	10	10	10	10	ns
tDVSL	Data set up time	1	1	1	1	ns
tSLDX	Data hold time	9	9	9	9	ns
Note: These figures are not characterised and are subject to change						

Table 7.8 Pixel port timing parameters

7.8 Video Timing Generator

The Video Timing Generator is a programmable finite state machine. It provides composite sync and blanking to the on-chip video DACs, it controls the timing of **BusReq** and **TransferA/B** and it starts and stops **notShiftClkA/B** to control the flow of pixel data. It also provides **FrameInactive** which is asserted during frame flyback enabling the controlling processor to perform screen updates invisibly, and **CBlank** which is asserted during frame or line flyback.

The timing generator can be configured to control an interlaced or non-interlaced monitor, and to generate the synchronising waveforms required by the EIA-343 (NTSC) and CCIR (PAL) studio television standards. These options are selectable in software and are controlled by the contents of the control register. Also controlled by this register is the operating mode of the device. it can be set to free run, in which case it will drive the synchronising signals out, or it can be set into slave mode when it will lock onto externally supplied vertical and horizontal sync pulses.

Programming of the timing generator is achieved by writing a set of screen description parameters to the timing registers. Its resolution is one quarter that of the individual pixels hence the scan lines must be described in 'screen units' of four pixels each. (i.e. a line with 1024 pixels is described as having 256 screen units.)

7.8.1 The display screen

In a raster scan display system, the picture is built up of a number of visible lines, which are displayed and a much smaller number of frame flyback lines, which are blanked. Each of the displayed lines has a single, visible, display period and a blanked line flyback period made up of front and back porch plus line sync. The total linetime is the sum of the displayed and blanked periods.

The frame timing periods are specified in multiples of half a linetime while the line timings are specified in screen units of four pixels duration each.

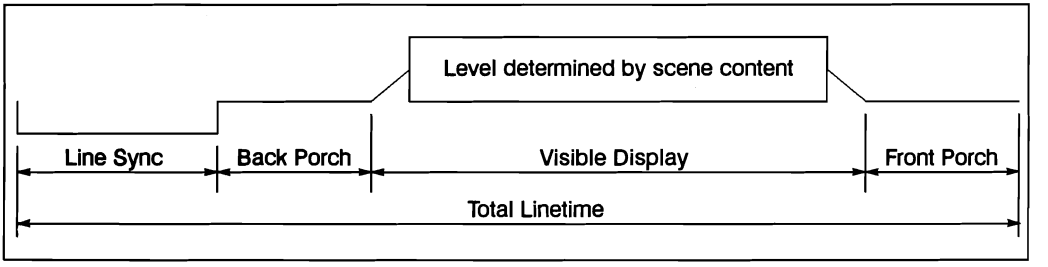


Figure 7.6 Scan line segments

Each displayed scan line of the raster is built up of the sections shown in figure 7.6. The visible portion is contained within the period 'display', so that, if a screen width of 1024 visible pixels (equal to 256 screen units) is required, then 256 is the number written to the 'display' register. For the remainder of the scan, the display is in line flyback and is therefore blanked.

The total linetime is the sum of all the sections of figure 7.6 and this is the number written to the 'linetime' register.

7.8.2 Line timing parameters

The line segments shown in figure 7.6 map directly to timing generator registers with two exceptions. First, the line synchronising pulse is split into two periods of equal duration which are used in immediate succession — the parameter used for this is 'halfsync' — and second, there is no register for frontporch, rather the total line time is programmed into a separate register and the end of the scan line occurs when this timebase period expires.

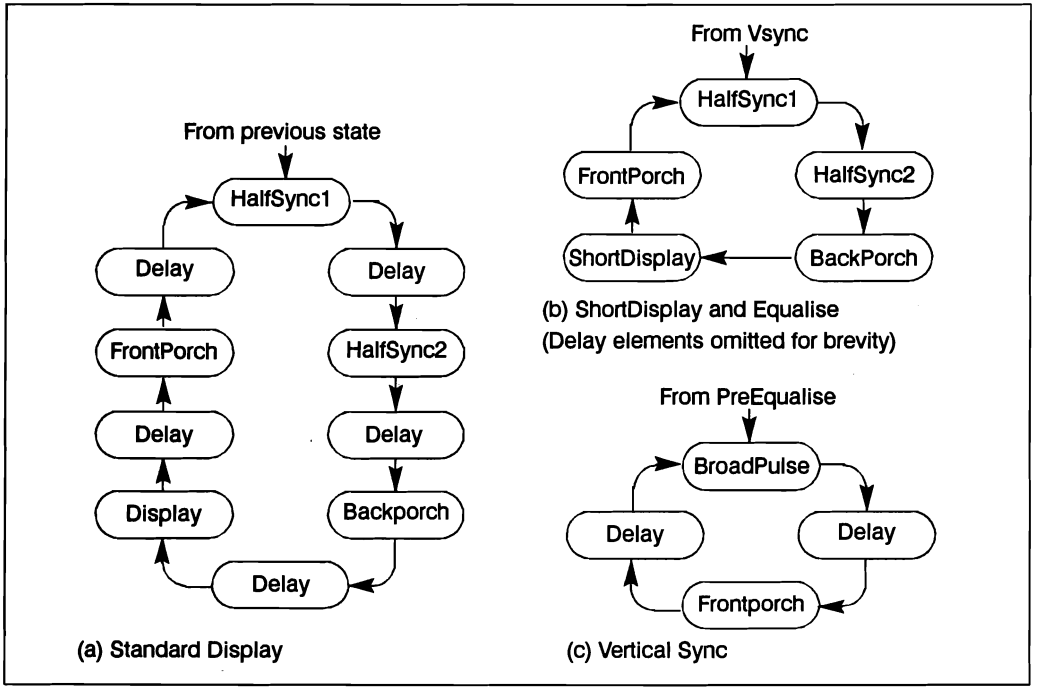


Figure 7.7 Flow diagrams for video timing generator

Figure 7.7 (a) shows the flowchart of a standard displayed or blanked scan line (as distinct from the truncated unscanned lines used in vertical sync and equalisation). The state machine proceeds from one state

to the next according to the delay programmed in by the user; on entering a new state the Sync and blanking outputs are modified depending on which part of the cycle is being executed.

Figure 7.8 (a) shows the relationship of the screen description parameters to a full scan line. Note that front-porch is undefined and halfsync is used twice in succession to construct the line sync pulse.

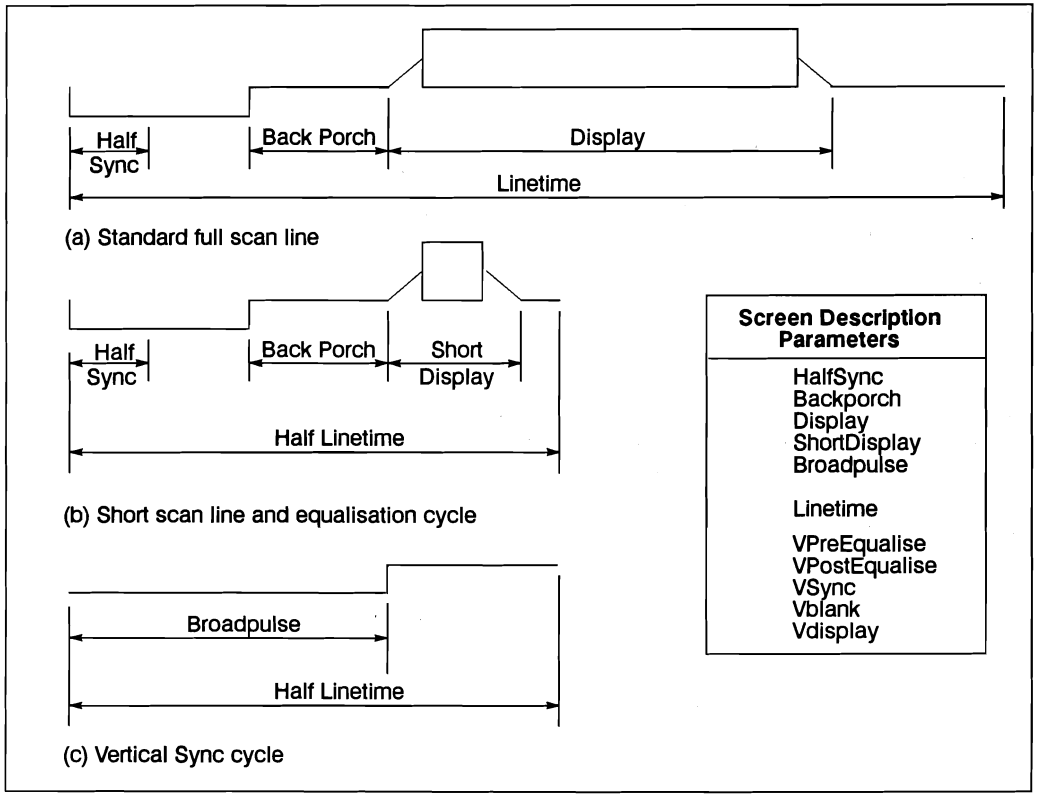


Figure 7.8 Screen description parameter definitions

7.8.3 Frame timing parameters

The G332 generates synchronising signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating the ordinary frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tesselated sync signals for an interlaced television system (see figure 7.9).

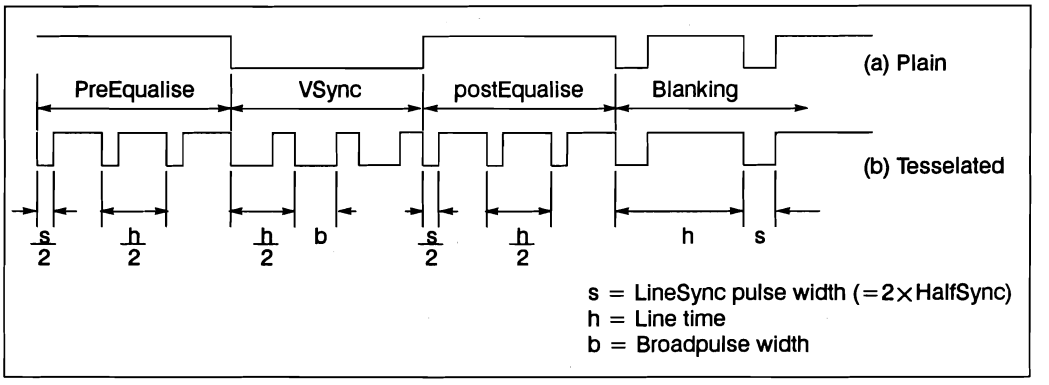


Figure 7.9 Composite Sync frame flyback waveforms

A further requirement of the television standards is that each frame must contain an odd number of scan lines. As a result, the frame timing parameters need to be specified in terms of half line times. Thus a non-interlaced screen of 1024 visible lines has the value 2048 written to the VDisplay register. (An interlaced screen of 625 lines would have 625 in that register since in interlace, the VDisplay register decribes the vertical display *field* rather than the entire frame – see table 7.9).

Screen Type	Lines per Frame	Value in VDisplay Register	Lines per Field
non-Interlace	1024	2048	1024
Interlace	1024	illegal	illegal
non-Interlace	625	1250	625
Interlace	625	625	312.5

Table 7.9 Frame programming examples

The duration of preEqualise, postEqualise, VSync and VBlank are also defined as multiples of half lines. The total frame blanking period is the sum of these four.

In order to generate the tesselated equalisation and blanking waveforms shown in figure 7.9(b), some additions to the basic line parameters are needed. The low period during VSync is defined as 'broadpulse' with its duration stored in the 'broadpulse' register. The shorter low period during pre and post equalisation is equal to half the line sync period and hence uses the value stored in the 'halfsync' register.

Reference to figure 7.7(b) and (c) shows that, on entering frame flyback, the state machine loop shortens to give a period of half a linetime. In equalisation, this is achieved simply by substituting 'shortdisplay' for 'display' in the sequence, whereas in vsync the sequence is changed to include only 'broadpulse' and 'frontporch'.

7.8.4 Parameter calculation

Calculation of the frame timing parameters is simple and direct – to produce the flyback waveform in figure 7.9(a) the parameters VSync, preEqualise and postEqualise are set to 3 – and the line parameters are derived from the equations in table 7.10.

During a full line cycle (VBlank, VDisplay)		
Halfsync	=	Horizontal Sync/2
BackPorch	=	BackPorch
Display	=	Display
Linetime	>	(2×HalfSync + BackPorch + Display)
During an equalisation cycle		
ShortDisplay	<	Linetime/2 – (2×HalfSync + BackPorch)
Low period	=	HalfSync
High period	=	Linetime/2 - HalfSync
During a VSync cycle		
BroadPulse	=	Linetime/2 - Pulse width*
Low Period	=	BroadPulse
High period	=	Pulse width

Table 7.10 Screen description line parameter equations

* Note: Pulse width = duration of serration pulse high time

The following restrictions on parameter values must be observed:

- All parameters must be greater than 1.
- Linetime must be an even multiple of the period of **notSerialClk**.
- 2×HalfSync + BackPorch + Display > Linetime/2 > 2×HalfSync + BackPorch.
- The total number of displayed lines in each frame must be a whole number. In interlace, this must be an odd whole number.
- Backporch must exceed TransferDelay by at least one **notSerialClk** period; also it must exceed 16 SClk periods in total.
- Transfer delay must not exceed ShortDisplay.

(The parameter TransferDelay is described in section 7.10.4).

7.8.5 The startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is accomplished while the timing generator is disabled.

On startup, after reset, the host processor must write a configuration pattern to the G332 bootstrap location. The effect of this is to set the PLL multiplication factor, clock source (PLL or external crystal) and microport address alignment. It must then initialise the VTG by writing a 0 to bit 0 in control register A.

Startup sequence:

1 Assert, then deassert **Reset**.
—Wait 50ns

2 Write configuration pattern to bootstrap location.

3 Write to control register to initialise VTG.

After this the screen parameters and colour table data can be written to the appropriate locations in any order. The processor must then make another write to the control register to enable the VTG which will then start up immediately at the beginning of frame sync. The G332 can be reprogrammed without asserting Reset.

The reprogramming sequence has three steps:

1 Write zero to bit 0 of the control register, disabling VTG.

2 Write to the screen parameter registers chosen for redefinition.

3 Write one to bit 0 of the control register, (redefining modes if necessary by modifying the relevant register bits) and enabling the VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed the full startup procedure must be followed, including reset.

7.9 Synchronising and blanking signals

7.9.1 Introduction

The video timing generator produces sync and blank signals to a pattern specified by a combination of the operating mode of the G332 and the screen description parameters. Internally, composite sync and blank are supplied to the three DACs by default. However, both of these functions can be disabled by setting bits 6 and 11 of Control RegisterA, respectively.

The internal sync and blank signals are automatically scheduled according to the operating mode. An additional programmable delay of 0 - 7 serial clock cycles may be added to sync and blank if it is required to add pipeline delays in the pixel path.

7.9.2 Master mode

When running in master (internal sync) mode, the **notVSync** and **notCorHSync** pins are outputs and the G332 drives them active low. Untesselated frame sync always appears on the **notVSync** pin, while the **notCorHSync** pin is switchable to supply one of line sync, plain composite sync, or tesselated composite sync:

Register Bits 5	4	notVSync	notCorHSync	
			notHSync	notCSync
0	0	Plain	-	Tesselated
0	1	Plain	-	Plain
1	0	Plain	Plain	-
1	1	Plain	Plain	-

7.9.3 Slave mode

In slave mode, the **notVSync** and **notCorHSync** pins are designated as inputs, and the G332 will use them to determine when to start a frame. In such a scheme two or more devices can be synchronised together.

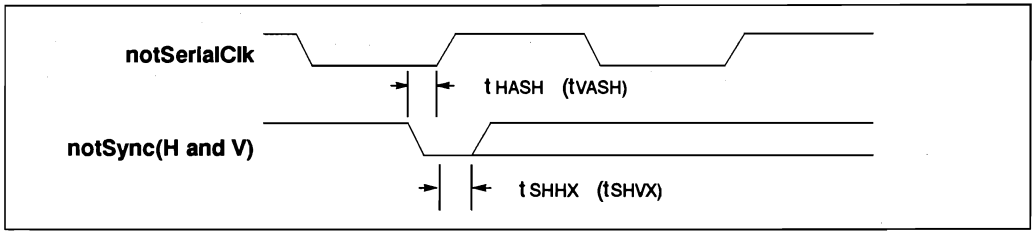


Figure 7.10 External synchronisation

Symbol	Description	Min.	Max.	Unit
tVASH	**notVsync** setup time	SClk/4	3SClk/4	ns
tHASH	**notHsync** setup time	SClk/4	3SClk/4	ns
tSHVX	**notVsync** hold time	0		ns
tSHHX	**notHsync** hold time	0		ns
Note: These figures are not characterised and are subject to change				

Table 7.11 External sync waveform timings

7.10 The micro port

7.10.1 Introduction

The micro port is a bidirectional 24 bit interface, consisting of a multiplexed address and data bus and several control signals. It is used for programming the VTG screen description registers, colour and cursor lookup tables, cursor store, and other registers.

As well as serving as a programming port the interface is also capable of performing a video RAM shift register transfer operation using a fully handshaked DMA. The timing of this operation is synchronous with the pixel port and is arranged so that seamless update of the video RAM shift register is possible.

7.10.2 Word alignment

The IMS G332 is designed for use with 32 and 64 bit processors, and therefore supports both 32 and 64 bit word alignment. With 32 bit alignment selected, the least significant address bit is on **ADBus2**; with 64-bit alignment selected it is on **ADBus3**. This applies both on host processor accesses to the microport and on DMA transfer cycles.

7.10.3 Micro port read/write cycles

Four signals control the flow of address and data in and out of the device on **ADBus0-23**.

Signal	I/O	Function
notChipSelect	I	The falling edge latches the address and samples **ReadnotWrite.** The cycle is initiated. The rising edge terminates the cycle, and tristates the **ADBus** drivers on a read cycle.
ReadnotWrite	I	If this signal is low shortly after **notChipSelect** goes low, the cycle is a write; if it is high the cycle is a read. Additionally on a write cycle, the rising edge of **ReadnotWrite** strobes in the data.
notOutputEnable	I	This signal is used only during read cycles, and enables the read data onto the **ADBus**. It should be kept high at all other times.
Wait	O	Wait eliminates the need for an external wait state generator. It is driven high shortly after **notChipSelect** goes low, and is driven back low when the G332 is ready for write data to be strobed by **ReadnotWrite** or read data is about to become valid on the **ADBus**.

7.10.4 DMA transfer operation

The IMS G332 provides three signals; **BusReq**, **TransferA** and **TransferB**, to control the synchronous reloading of the VRAM shift registers. Both **TransferA** and **TransferB** are used in interleaved mode, **TransferA** only is used in non-interleaved mode.

The G332 asserts **BusReq** to obtain use of the **ADBus** to perform a DMA cycle. The host processor asserts **BusGranted** to acknowledge the request. **TransferA** and **TransferB** (if used) are driven high simultaneously by the G332, and trigger the external generation of RAS, address mux and CAS signals to the VRAMs. **TransferA** goes low synchronous with **notShiftClkA**, and **TransferB** is synchronised to **notShiftClkB**. This performs the transfer operation.

The exact time at which the transfer occurs is critical, since mid-line updates must be seamless. The time taken from assertion of **BusReq** to the transfer taking place is a sum of various system delays, some of which are variable. The parameter **Transfer Delay** (Micro port address #X02D) must be set thus:

Transfer Delay $\geq$ The maximum possible system DMA latency + VRAM access + 4 SClk

The G332 has a further requirement, that:

$$\textbf{TransferDelay} \leq \text{Backporch} - 1$$

to ensure that there is data loaded ready for the first scan line to begin.

Another parameter, **MemInit** (Microport Address #X02C), determines the frequency of DMA transfer cycles. The sum of **MemInit** and **TransferDelay** defines the interval between successive Bus Requests.

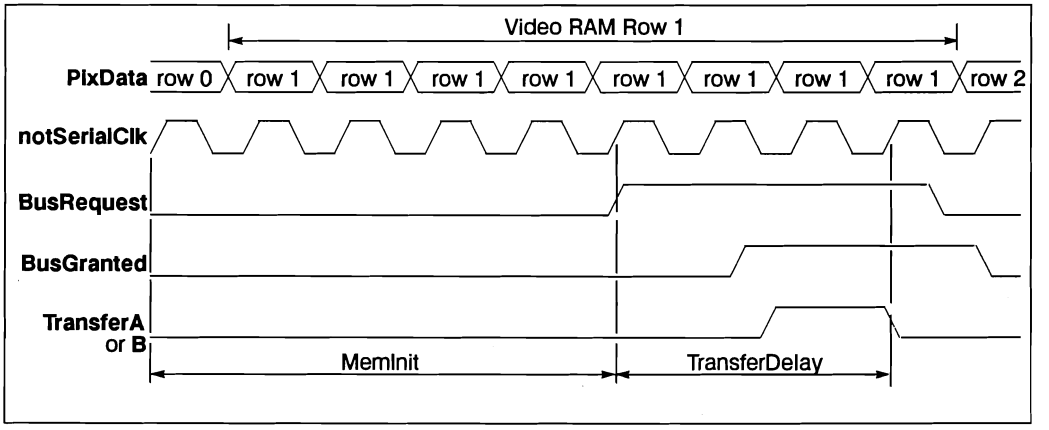


Figure 7.11 Data transfer sequence

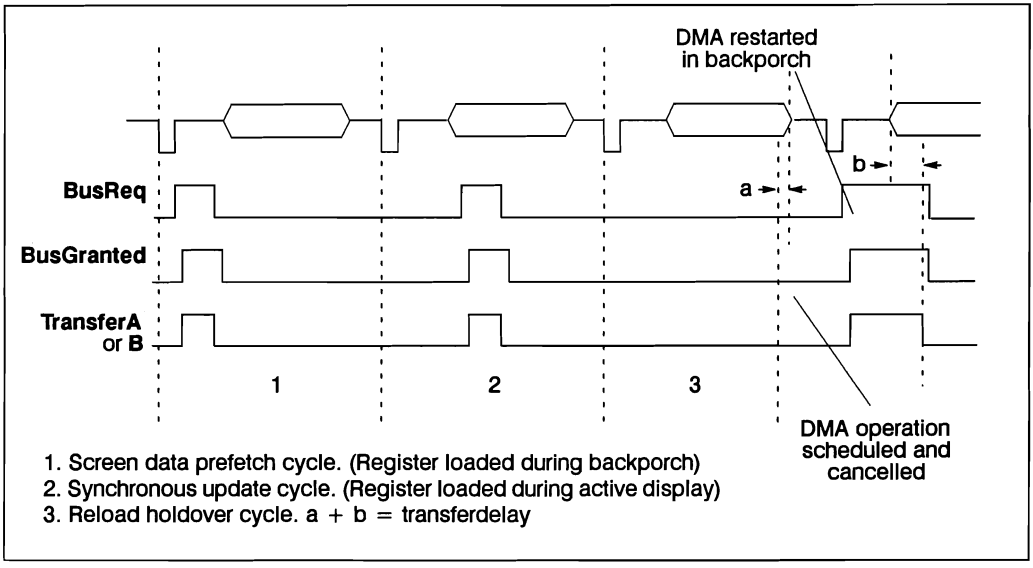


Figure 7.12 Data transfer operational behaviour

Figure 7.11 shows the sequence of events during a synchronised VRAM row transfer operation performed by the G332 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers.

7.10.5 VRAM address increment

To allow either the existing VRAM row or column address latches to be used for the row address during DMA transfer cycles, several address increments are provided, both for interlaced and non-interlaced modes. They are selected from Control Register A.

Register Bit			Description	Format	Second field
13	12	1			
0	0	0	Increment by 1.	Non-interlace format.	
0	0	1	Increment by 1.	Interlace format.	Every second field offset by 1.
0	1	0	Increment by 256.	Non-interlace format.	
0	1	1	Increment by 2.	Interlace format.	Every second field offset by 1.
1	0	0	Increment by 512.	Non-interlace format.	
1	0	1	Increment by 512.	Interlace format.	Every second field offset by 256.
1	1	0	Increment by 1024.	Non-interlace format.	
1	1	1	Increment by 1024.	Interlace format.	Every second field offset by 512.

Table 7.12

7.10.6 FrameInactive

A further timing signal, **FrameInactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **FrameInactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

7.11 The pixel port

The 32 bit pixel port takes in pixel data from the video RAM and has various modes of operation.

7.11.1 Interleaved/non-interleaved operation

Because of the very high video rates supported by the G332 it is not possible in some situations to supply pixel data fast enough from a single bank of video RAMs. An interleaved mode has been provided to allow two banks of VRAM to be used, each running at half the frequency required when using one bank. 32 bits of pixel data are loaded alternately from one VRAM bank then the other.

In interleaved mode, two **notShiftClk** and two **Transfer** signals are used to control the two banks, the shift clocks running in anti-phase. **notShiftClkA** and **TransferA** control the lower numbered pixels, and not-**ShiftClkB** and **TransferB** control the higher numbered pixels. On DMA transfer cycles both banks have their shift registers reloaded, which means that these cycles are required at half the frequency compared with non-interleaved mode.

In non-interleaved mode only **notShiftClkA** and **TransferA** are used, and true-colour pixel modes are not available.

7.11.2 Pixel sampling

The point at which pixels are sampled by the G332 varies according to the pixel mode selected (refer to section 7.11.3). In 8 bit per pixel non-interleaved mode and 15/16 bit per pixel interleaved mode, pixels are sampled one not serial clock period **(SClk)** after **notShiftClkA** or **B.** In all other modes sampling is optionally delayed by a further 1/2 **ShiftClk**.

7.11.3 Pixel multiplexing

The G332 supports 6 pixel modes in interleaved mode and 4 in non-interleaved mode selected from control register A, as follows:

Non-interleaved mode

Register bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
0	1	1	0	8	1 SClk	4:1	Pseudo colour
0	1	0	0	4	2 SClks	8:1	Pseudo colour
0	0	1	0	2	4 SClks	16:1	Pseudo colour
0	0	0	0	1	8 SClks	32:1	Pseudo colour

Interleaved mode

Register bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
1	0	1	1	16	1 SClk	2:1	Gamma corrected true colour
1	0	0	1	15	1 SClk	2:1	Gamma corrected true colour
0	1	1	1	8	2 SClks	4:1	Pseudo colour
0	1	0	1	4	4 SClks	8:1	Pseudo colour
0	0	1	1	2	8 SClks	16:1	Pseudo colour
0	0	0	1	1	16 SClks	32:1	Pseudo colour

7.11.4 True colour modes (15 and 16 bits per pixel)

Each pair of pixel ports (A and B, and C and D) supply a two-byte pixel value which is split into red, green and blue fields as illustrated below. In 15 bits per pixel mode bits 0-4 are blue, 5-9 are green, and 10-14 are red. In 16 bits per pixel mode bits 0-3 are blue, 4-9 are green, and 10-15 are red.

Each colour field addresses the LUT which may contain a suitable gamma correction table for that colour. The unused LUT address bits in 15 and 16 bit per pixel modes are the lowest order bits, which avoids the need to change the gamma-correction table when switching between true colour modes. If no gamma correction is required the LUT must be written with data = address.

Port	A	A	A	A	A	A	A	A		B	B	B	B	B	B	B	B		C	C	C	C	C	C	C	C		D	D	D	D	D	D	D	D
Bit	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7
15bpp																																				
Pixel	Pixel 0																		Pixel 1																	
Colour	B	B	B	B	B	G	G	G		G	G	R	R	R	R	R	X		B	B	B	B	B	G	G	G		G	G	R	R	R	R	R	X
Bit	0	1	2	3	4	0	1	2		3	4	0	1	2	3	4	-		0	1	2	3	4	0	1	2		3	4	0	1	2	3	4	-
16bpp																																				
Pixel	Pixel 0																		Pixel 1																	
Colour	B	B	B	B	G	G	G	G		G	G	R	R	R	R	R	R		B	B	B	B	G	G	G	G		G	G	R	R	R	R	R	R
Bit	0	1	2	3	0	1	2	3		4	5	0	1	2	3	4	5		0	1	2	3	0	1	2	3		4	5	0	1	2	3	4	5
Key: R = Red, G = Green, B = Blue and X = bit not used																																				

Figure 7.13 Pixel mapping diagram

7.11.5 Pseudo colour modes (1, 2, 4 and 8 bits per pixel)

The pixel data is latched from ports A, B, C and D in that order. Each pixel is masked by 8 bits of the mask register before the output is used to address all three LUTs which contain the pseudo colour palette.

8 bits per pixel mode:

Each port supplies 1 pixel. Bits 0-7 of the port correspond to LUT address bits 0-7 respectively. All 256 locations in the LUT are used.

4 bits per pixel mode:

Each port supplies 2 pixels. Bits 0-3 of the port are the first pixel displayed, bits 4-7 are the second pixel displayed. Both correspond to LUT address bits 0-3 respectively. Only locations 0 to 15 of the LUT are used.

2 bits per pixel mode:

Each port supplies 4 pixels. Bits 0-1 of the port are the the first pixel displayed, bits 6-7 the last pixel displayed. Each pair of pixel inputs corresponds to LUT address bits 0-1. Only locations 0 to 3 of the LUT are used.

1 bit per pixel mode:

Each port supplies 8 pixels. Bit 0 of the port is the first pixel displayed, bit 7 the last pixel displayed. Each pixel input corresponds to LUT address bit 0. Only locations 0 and 1 of the LUT are used.

7.11.6 Mask register

(micro port address #X040)

The 24 bit mask register masks the pseudo colour pixel inputs to the three LUTs. Bits 0-7 mask the blue data, 8-15 the green data, and 16-23 the red data. Setting a bit in the mask register to zero causes the corresponding LUT address bit to be set to zero.

7.12 Hardware cursor

The G332 hardware cursor consists of a 64×64×2 bit RAM, addressed as a sequence of consecutive 16 bit words. Each word is formatted into 8 pixels as below, and is randomly addressable at any time.

Pixel	7		6		5		4		3		2		1		0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Cursor position is held in a single 24 bit register as an x-y location relative to the top left of the screen. The position defined is that of the topmost, leftmost pixel of the cursor. The most significant half of the cursor position word (bits 12-23) is its x-address (horizontal position) and the least significant half (bits 0-11) is its y-address (vertical position). The cursor position is held in the CursorStart register at microport address #X0C7. The x-address and y-address are two's complement values in the range -64 to 2303.

The 2 bit cursor pixels address a 3 location cursor look-up table as follows:

Pixel value	Format
0 0	Cursor transparent. Background colour displayed.
0 1	Colour from cursor LUT location 1
1 0	Colour from cursor LUT location 2
1 1	Colour from cursor LUT location 3

The cursor is enabled/disabled via bit 23 in Control RegisterA.

7.13 Anti-sparkle colour palette

The IMS G332 includes a 256×24bit colour look-up table which is mapped directly into the micro port address space. Complete colour values are written by a single write cycle on the micro port. In order to minimise picture disturbance whilst a colour palette entry is being accessed, the previous pixel is repeated at the DACs.

7.14 Checksum registers

There are three 24 bit checksum registers, one for each colour channel. Their purpose is to facilitate testing the device and systems containing it. The checksum is located directly before the DACs, and after the colour and cursor palettes. The checksum value is dependent on the cursor position and whether or not interlaced mode is selected, but independent of sync modes and flyback patterns.

The checksum registers are reset by the falling edge of **FrameInactive**. They accumulate only those pixels which are visible on the screen, i.e. those pixels which are unblanked. The registers should be read during the first part of frame flyback. At the end of this period they are being reset, and at other times they are being accumulated and are consequently invalid.

The checksum registers are addressed from the microport as 24 bit words containing low, middle and high bytes, as follows:

Micro port address	Bits 16-23	Bits 8-15	Bits 0-7
#X0C0	Red bits 0-7	Green bits 0-7	Blue bits 0-7
#X0C1	Red bits 8-15	Green bits 8-15	Blue bits 8-15
#X0C2	Red bits 16-23	Green bits 16-23	Blue bits 16-23

7.15 Clocks

The IMS G332 has two alternate clocking schemes. The primary clocking system uses a phase locked loop (PLL) on the chip to multiply up the low frequency (<10MHz) input clock to the required video data rate. Alternatively a full dot-rate clock may be supplied (×1 mode).

7.15.1 PLL mode

In PLL mode, a 1μF capacitor must be connected between **CapPlus** and **CapMinus.** A ceramic capacitor is preferred, with an impedance of less than 3Ω between 100kHz and 10MHz. If a polarised capacitor is used, the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm.

The multiplication factor is determined from the binary value written to bits 0..4 of the boot location (#X000). Values from 5 to 31 are permitted. Also, the clock source select bit (bit 5) in the Boot Location (#X000) must be set to a '1'.

ClockIn must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. ClockIn must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits.

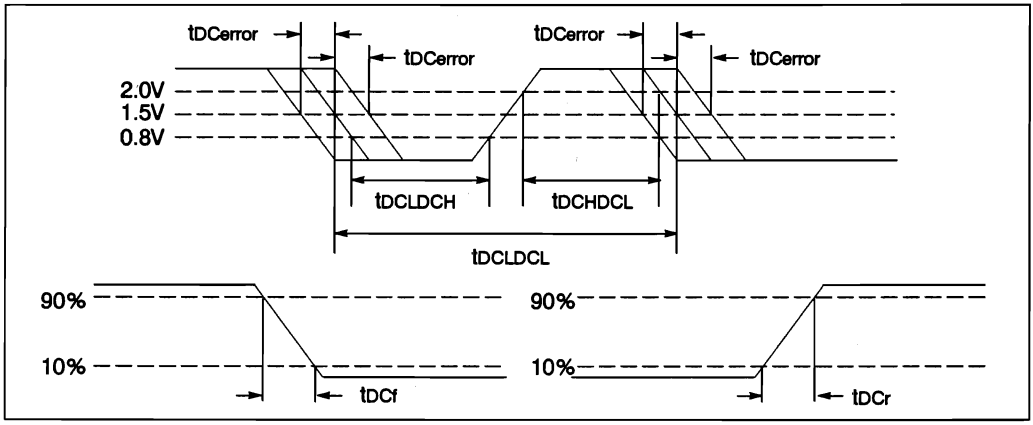


Figure 7.14 ClockIn timing

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
tDCLDCH	ClockIn pulse width low	20			ns	
tDCHDCL	ClockIn pulse width high	20			ns	
tDCLDCL	ClockIn period	100		200	ns	1
tDCerror	ClockIn timing error			±0.015	%	2
tDCr	ClockIn rise time			10	ns	3
tDCf	ClockIn fall time			8	ns	3
Note: These figures are not characterised and are subject to change						

Table 7.13 ClockIn timings in PLL mode

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their normal times.

3 Clock transitions must be monotonic within the range **VIH** to **VIL**.

Note: These figures are not characterised and are subject to change.

7.15.2 'Times 1' mode

The external ×1 clock can be selected in one of two ways. Either the terminals **CapPlus** and **CapMinus** should be shorted together, or the clock source select bit in the boot location should be written to a '0'.

7.16 The video DACs

7.16.1 General

The video DACs have 8 bit resolution, and are designed to drive a doubly terminated 75Ω transmission line and produce analogue outputs compatible with RS170 and RS343 video standards.

The DACs work by sourcing a current proportional to their digital input. The DAC unit current for each digital increment is defined by an external **Iref** current source;

$$1\ \text{DACunit} = \textbf{Iref}/120$$

The video information output by each gun ranges from 0 to 255 units under the control of the digital input from the colour palette or the pixel pin.

A sync pedestal of 108 DAC units and a blanking pedestal of 20 DACunits are provided. The sync pedestal allows superposition of the sync timing signals on the video outputs. The blanking pedestal ensures that no visible trace appears on the screen during flyback.

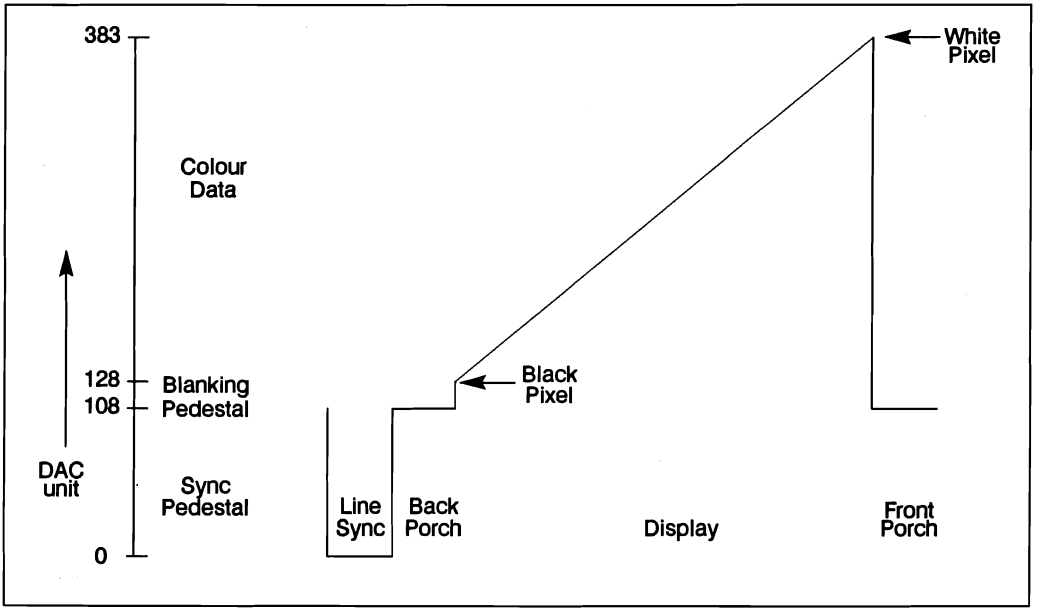


Figure 7.15 DAC output levels

7.16.2 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
	Resolution	8	8	8	bits	
VO(max)	Output voltage			1.5	V	2
IO(max)	Output current			34	mA	VO≤1V
	Full scale error			± 5	%	2, 3
	Sync pedestal error			±10	%	2
	Blank level pedestal error			±10	%	2
	DAC to DAC correlation error			± 2.5	%	2, 4
	Integral Linearity error			± 1	LSB	2, 5
	Glitch Energy		75		pVSec	2, 6, 7
Iref	Reference current	7		10	mA	
Vref	Reference voltage	VDD −3V		VDD	Volts	
Note: These figures are not characterised and are subject to change						

Notes

1 All voltages with respect to **GND** unless specified otherwise.

2 Tested over the operating temperature range and at nominal supply voltage with **Iref** = −8.88mA.

3 From the value predicted by the design equation, sync and black level pedestals off.

4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.

5 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

6 Load = 37.5Ω +30 pF with **Iref** = −8.88mA.

7 This parameter is sampled not 100% tested.

7.16.3 Power supply and reference circuit

7.16.4 Power supply and current reference

It is recommended that a high frequency decoupling capacitor (preferably a chip capacitor) in parallel with a larger tantalum capacitor (22μF to 47μF) be placed between **AVDD** and **GND** to provide the best possible supply to the analogue circuitry of the DACs.

It is further recommended that the IMS G332 is soldered directly into the PCB without using a socket in order to minimise inductance.

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 7.16 shows four designs of current reference.

If the board **VDD** supply is very noisy, then it is advisable to provide a quiet supply for just the IMS G332. This may be done by supplying both **VDD** and **AVDD** through a small inductor (1-5μH). This will act as an ac filter for high frequency noise. However, if this is done care should be taken to ensure the power rating of this inductor is not exceded.

Figure 7.16(d) shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 7.16(a)-(c) are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current **Iref** through a transistor. In circuits 7.16(b) and 7.16(c) the thermal variations in

the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 7.16(c)).

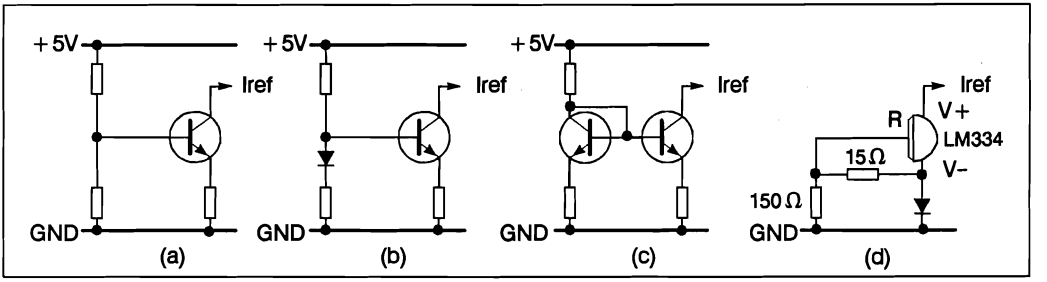


Figure 7.16

7.16.5 Current reference – decoupling

The DACs in the IMS G332 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current **Iref**.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the **Iref** input to VDD. This will enable the current reference to track both low and high frequency variations in the supply.

7.16.6 Analogue output – line driving

The G332 is designed to drive a doubly terminated 75Ω line. This arrangement is illustrated in figure 7.17. The effective load seen by the G332 video outputs with this circuit is 37.5Ω.

The connection beteween the DAC outputs on the G332 and the input to the colour monitor should be regarded as a transmission line. Impedance changes along this line will result in reflection of part of the video signal back along the line. These reflections can result in a degradation of the picture displayed by the monitor. To ensure good fidelity RF techniques should be used; in particular the PCB trace from the G332 video output pins to the video sockets on the graphics board should be kept short (less than 3 inches is ideal). If this is done then any reflections due to a mismatched impedance at the video connectors will occur within the risetime of the DAC waveform and will not cause a degradation of the image quality.

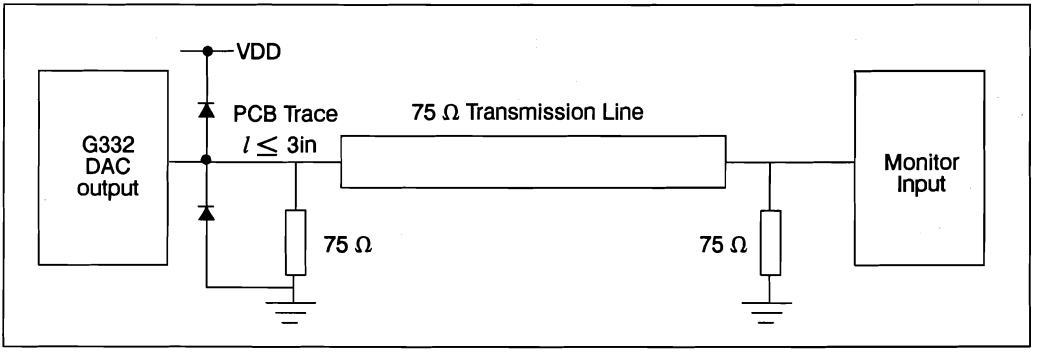


Figure 7.17 DAC output loading

7.16.7 Analogue output – protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G332 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G332 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection diodes to the power rails are recommended at this exposed interface.

7.17 General parametric conditions and characteristics

7.17.1 Absolute Maximum ratings

Symbol	Parameter	Min.	Max.	Units	Notes
AVDD/VDD	DC Supply Voltage		7	Volts	
	Voltage on other pins	VSS–1	VDD + 0.5	Volts	
TS	Storage temperature (ambient)	–65	150	°C	
TA	Temperature under bias	–40	85	°C	
PDmax	Power dissipation		TBD	W	
Iref	Reference current		15	mA	
	Analogue O/P current		45	mA	1
	DC Digital O/P current		25	mA	

Notes

1 Per output

7.17.2 Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	1
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD + 0.5	Volts	
VIL	Input Logic '0' Voltage	–0.5		0.8	Volts	
TPQFP	Case Temperature	TBD		TBD	°C	2
TCQFP	Case Temperature	TBD		TBD	°C	2
Note: These figures are not characterised and are subject to change						

Notes

1 AVDD = VDD

2 Measured on the lid of the package at maximum power dissipation.

7.17.3 Operating characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
IDD	Power Supply Current		TBD	TBD	mA	
IIN	Digital Input Current			±10	µA	
IOZ	TriState Dig Output Current			±50	µA	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	−5			mA	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOL	Output Logic '0' Current	5			mA	
Note: These figures are not characterised and are subject to change						

7.17.4 Output drive capability

Parameter	Min.	Max.	Units	Notes
notShiftClkA		25	pF	1
notShiftClkB		25	pF	1
notSerialClk		25	pF	1
TransferA		25	pF	
TransferB		25	pF	
ADBus [0..23]		25	pF	

Notes

1 **These loadings must be strictly adhered to in order to avoid a degradation in picture quality.**

7.18 Package specifications

7.18.1 100 pin ceramic quad flatpack package

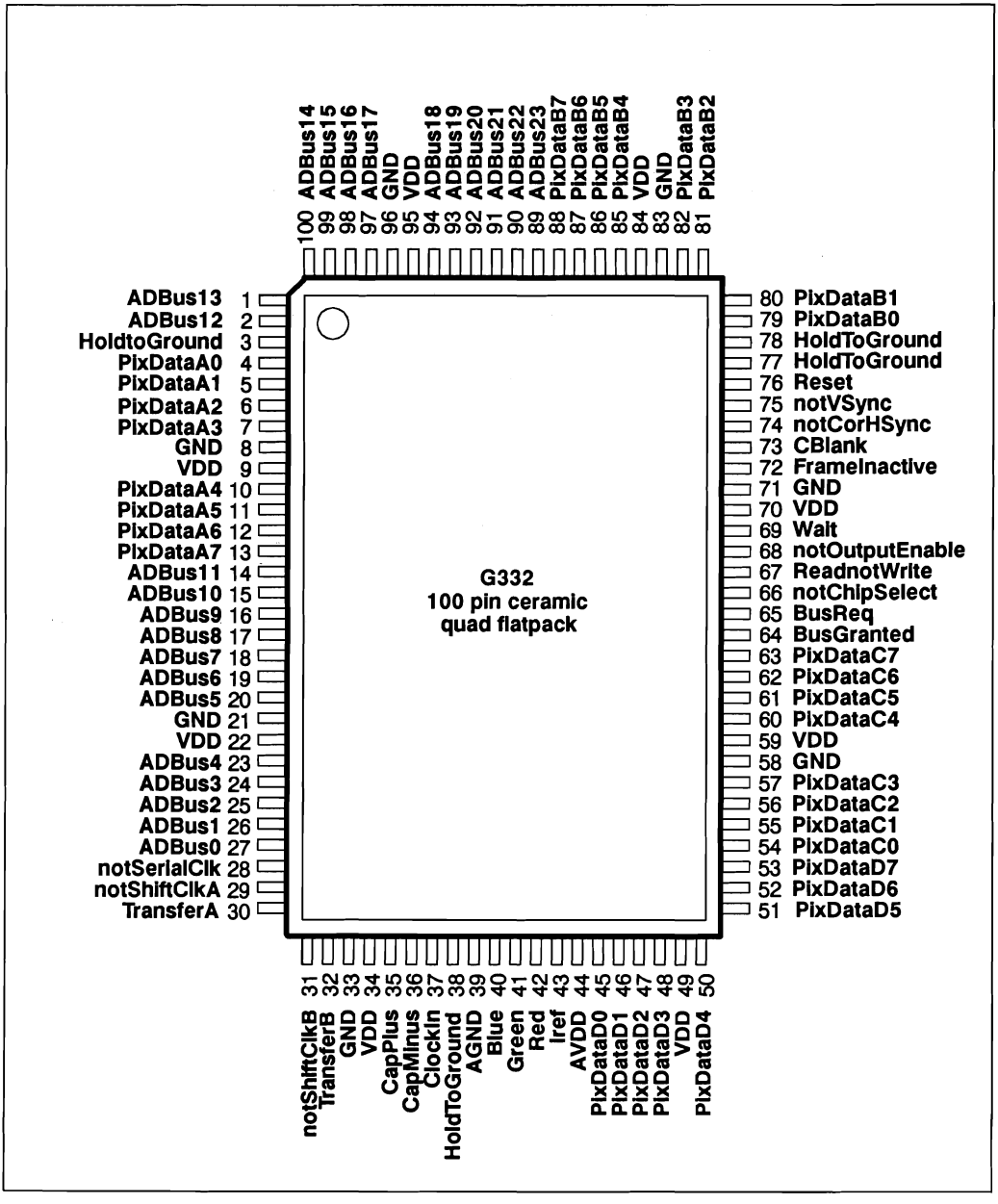


Figure 7.18 IMS G332 pin configuration

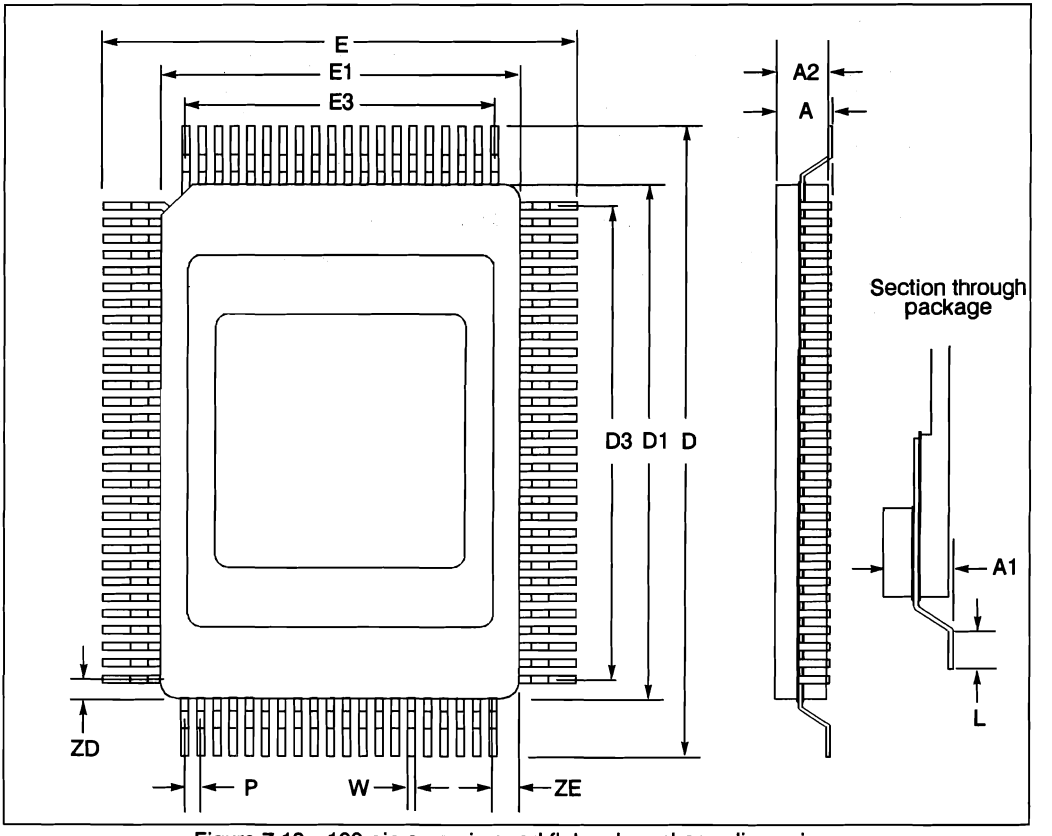


Figure 7.19 100 pin ceramic quad flatpack package dimensions

Dim	Millimetres			Inches			Notes
	Min	Nom	Max	Min	Nom	Max	
A			3.300			0.130	
A1	0.000		0.250	0.000		0.010	
A2	2.550	2.800	3.050	0.100	0.110	0.120	
D	23.650	23.900	24.150	0.931	0.941	0.951	
D1	19.900	20.000	20.100	0.783	0.787	0.791	
D3		18.850			0.742		Ref.
ZD		0.580			0.023		Ref.
E	17.650	17.900	18.150	0.695	0.705	0.715	
E1	13.900	14.000	14.100	0.547	0.551	0.555	
E3		12.350			0.486		Ref.
ZE		0.830			0.033		Ref.
L	0.650	0.800	0.950	0.026	0.031	0.037	
P		0.650			0.026		BSC
W	0.220		0.380	0.087		0.015	

Table 7.14 100 pin ceramic quad flatpack package dimensions

7.18.2 Ordering information

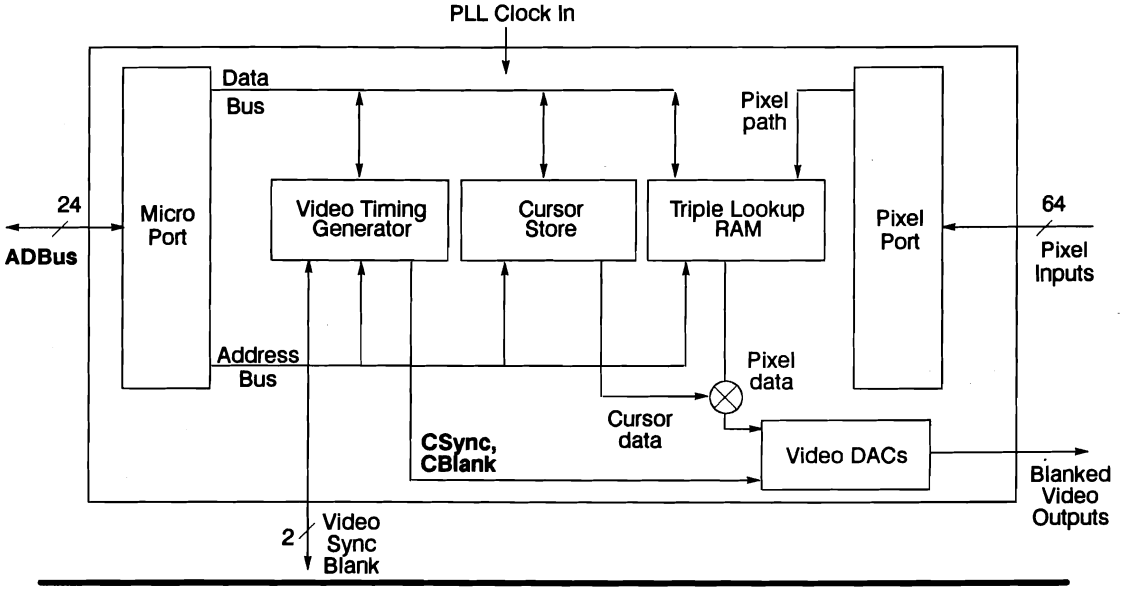
Device	Clock rate	Package	Part number
IMS G332	85 MHz	100 pin ceramic quad flatpack	IMS G332F-85S
IMS G332	100 MHz	100 pin ceramic quad flatpack	IMS G332F-10S
IMS G332	110 MHz	100 pin ceramic quad flatpack	IMS G332F-11S
*IMS G332	135 MHz	100 pin ceramic quad flatpack	IMS G332F135S
Note: PQFP for this device is currently under development			

* Available 1991

IMS G364
colour video controller

inmos®

Preliminary data



FEATURES

Video rates up to 110 MHz, (135MHz available in 1991)
Software configurable video timing generator
64×64×3 colour hardware cursor
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

Variable multiplexed pixel input
1, 2, 4 and 8 bit pseudo colour pixels
15, 16 or 24 bits per pixel gamma corrected colour
On chip triple lookup table with anti-sparkle
Triple high speed 8 bit video DACs
CCIR and EIA 343-A compatible

General purpose Video RAM support
Synchronous VRAM Data Transfer strobing
Video RAM Row address auto-increment
Screen width independent of VRAM architecture
On-chip phase-locked loop (PLL)

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

8.1 Introduction

The IMS G364 provides all the necessary functions to control real-time operation of a raster scan video display, using dual-ported video RAMs.

The device consists of a 32 bit variable multiplexed pixel interface, a programmable video timing generator (VTG), a 256 location colour lookup RAM (LUT) with variable addressing modes, triple 8 bit video DACs, a 64×64×2 bit cursor store and 3 location cursor LUT, a programmable cursor positioning/insertion controller, a video memory control system and phase-locked loop clock generator.

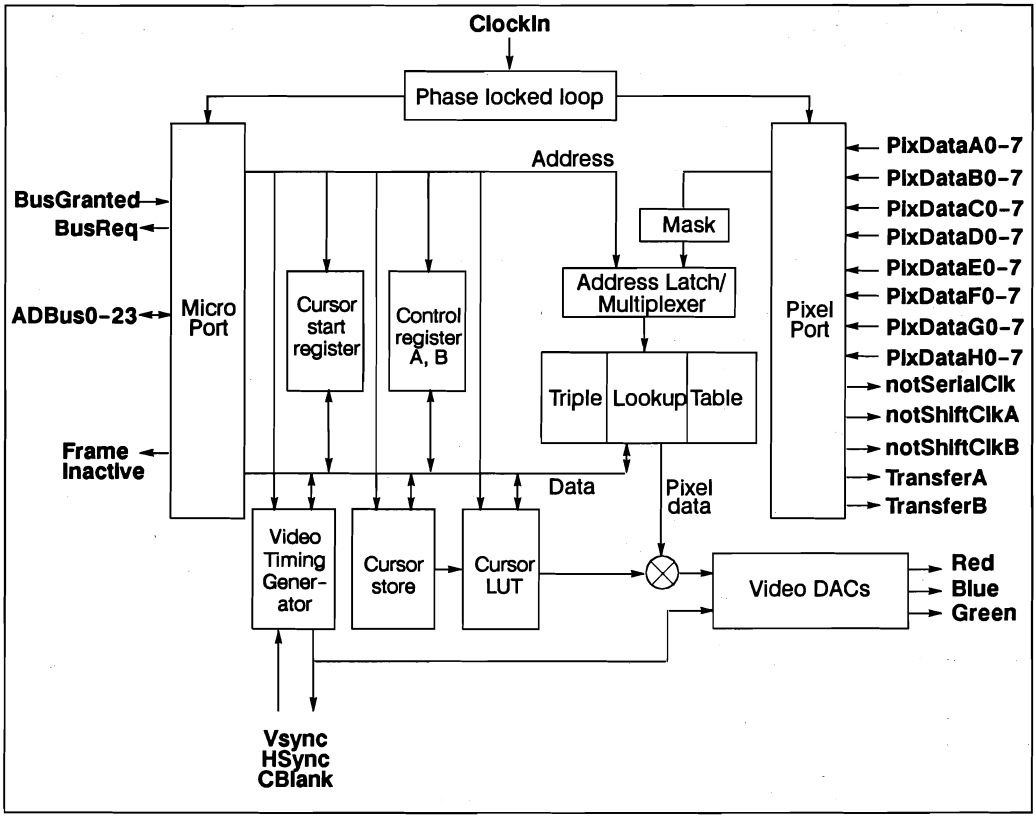


Figure 8.1 IMS G364 Block Diagram

8.2 Pin function reference guide

8.2.1 Micro port

Pin name	I/O	Page No.	Comments
FrameInactive	O	190	Timing signal which is high during vertical blanking.
BusReq **BusGranted**	O I	189	DMA control signals used in conjunction with **TransferA** and **TransferB** when refreshing the VRAM shift registers.
ReadnotWrite **notOutputEnable** **notChipSelect** **Wait**	I I I O	188	Microport control signals. Wait is used to extend cycle times if necessary.
ADBus0-23	I/O	188	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied either on **ADBus2-11** or on **ADBus3-12** depending on the word width.The port is also used to drive out the 24 bit VRAM transfer address.

8.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk	O	191	**notSerialClk** runs at one quarter the video frequency. This signal must be buffered
notShiftClkA **notShiftClkB**	O O	191	VRAM clocks running under the control of the timing generator. The clocks run in anti-phase in interleaved mode; only **notShiftClkA** runs in non-interleaved mode. These clocks must be buffered.
TransferA **TransferB**	O O	189	VRAM shift register transfer strobes. TransferA and B are synchronised to **notShiftClkA** and **notShiftClkB** respectively.
CBlank	I/O	182	**CBlank** is a composite blanking pin. Direction is soft selectable.
PixDataA0-7 **PixDataB0-7** **PixDataC0-7** **PixDataD0-7** **PixDataE0-7** **PixDataF0-7** **PixDataG0-7** **PixDataH0-7**	I I I I I I I I	191	Pixel input ports A–H. Port A is least significant; port H is most significant. Internally, pixel data is latched synchronous to **notSerialClk.**

8.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	186	Active high, must be held active with clocks running for at least 500ns.

8.3 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus **CapMinus**	N/A	195	Phase locked loop decoupling pins, also used to select external dot rate clock source by connecting **CapPlus** to **CapMinus**.
ClockIn	I	195	Clock input for both PLL and times-one operation.

8.3.1 Video signals

Pin name	I/O	Page No.	Comments
Red **Green** **Blue**	O O O	192, 196	Blanked video outputs. Drive into doubly terminated 75Ω load.
Iref	I	196	Video DAC reference current.
notVSync **notCorHSync**	I/O I/O	187	Digital sync signals for system synchronisation. They are inputs in slave mode and outputs in master mode. They are soft configurable.

8.3.2 Supplies

Pin name	I/O	Page No.	Comments
AVDD **AGND**	N/A N/A	197	**AVDD/AGND** supplies analogue portions of chip.
VDD **GND**	N/A N/A	197	**VDD/GND** supplies digital portions of chip.

8.4 Register function reference guide

Register	Address	Page No.	Comments
Boot Location	#X000	178	Startup location to which must be written the clock multiplication factor, whether PLL or ×1 mode, and the 32/64 bit address alignment selection.
Datapath Registers	#X021 to #X02E	176	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Mask Register	#X040	193	24 bit pixel address mask register. Read/write accessible at all times. (Operates only on pseudo colour pixels)
Control Registers	#X060 and #X070	177	Read/write control registers contains configuration information. Unassigned bits must be written with zero and are not valid on read. Read/write accessible at all times.
Top of Screen	#X080		Read/write register giving ability to reprogram the top of screen pointer at any time.
Cursor palette	#X0A1 to #X0A3	194	3×24 bit cursor colour registers. Read or write accessible at all times.
Checksum registers	#X0C0 to #X0C2	194	RGB frame checksums.
Colour Palette	#X100 to #X1FF	192	256 locations of 24 bit colours read/write accessible at all times.
Cursor store	#X200 to #X3FF	194	512 locations of 16 bit words, each containing 8 packed 2-bit pixel colour values.
Cursor position	#X0C7	194	24 bit register storing the x-y position of the cursor.

All other addresses in the range are reserved and must not be written to.

Note: #X = Hexadecimal address.

Word addresses are user-selectable to align with 64-bit or 32-bit words. In 32 bit mode, addresses must be supplied on **ADBus2-11**; in 64 bit mode they must be supplied on **ADBus3-12**. The addresses given above must be multiplied by the appropriate scale factor (4 in 32 bit mode, 8 in 64 bit mode) to obtain the corresponding byte addresses.

8.5 Datapath register allocation

Register	Address	Units	Notes
Half sync	#X021	Screen units	1
Back porch	#X022	Screen units	
Display	#X023	Screen units	
ShortDisplay	#X024	Screen units	
BroadPulse	#X025	Screen units	
VSync	#X026	Half lines	
VPreEqualise	#X027	Half lines	
VPostEqualise	#X028	Half lines	
VBlank	#X029	Half lines	
VDisplay	#X02A	Half lines	
LineTime	#X02B	Screen units	
Line Start	#X02C	Screen units	
MemInit	#X02D	Screen units	
TransferDelay	#X02E	Screen units	2

Notes

2 1 screen unit = 4 pixels horizontally = 1 Serial Clock period.

3 TransferDelay equates to a real time, and the value will therefore depend on the serial clock period.

8.6 The control registers and boot location

There is provision for two 24-bit control registers, one of which is initially populated.

Bit	Function	Comments
0	Enable VTG	0 = VTG disabled 1 = VTG enabled
1	Screen format	0 = non-interlaced 1 = interlaced
2	Interlace standard	0 = EIA format 1 = CCIR format
3	Operating mode	0 = master mode 1 = slave mode
4	Frame flyback pattern	0 = tesselated sync 1 = plain sync
5	Digital sync format	0 = composite sync 1 = separate sync
6	Analogue video format	0 = composite video + sync 1 = video only
7	Blank level	0 = no blank pedestal 1 = blanking pedestal
8	Blank I/O	0 = CBlank is input 1 = CBlank is output
9	Blank function switch	0 = delayed CBlank at pad 1 = Undelayed ClkDisable, at pad
10	Force blanking (irrespective of bit 11)	0 = no action 1 = screen blanked
11	Turn off blanking	0 = blanking enabled 1 = blanking disabled
12-13	VRAM address increment	see definition (section 8.10.5)
14	Turn off DMA	0 = DMAs enabled 1 = DMAs disabled
15-17	Sync delay	Delays sync and blank by 0 - 7 VTG clock cycles
18	Pixel port interleaving	0 = non-interleaved 1 = interleaved
19	Delayed sampling	see definition (section 8.11.2)
20-22	Bits per pixel	see definition (section 8.11.3)
23	Cursor disable	0 = cursor enabled 1 = cursor disabled

Table 8.1 Control register A bit allocations (Address #X060)

Bit	Function	Comments
0-23	All bits reserved	Write zero

Table 8.2 Control register B bit allocations (Address #X070)

Bit	Function	Comments
0–4	PLL multiplier	Binary coded PLL multiplication factor
5	Clock source select	0 = external (×1) clock 1 = PLL clock
6	Micro port address alignment	0 = 32 bit 1 = 64 bit
7–23	Reserved	Write zero

Table 8.3 Boot location bit allocations (Address #X000)

The boot location must be written on power-up before attempting to access any other locations from the micro port. The timing of this first cycle is asynchronous; the value substituted for the serial clock period in the timing parameters should be the minimum allowable for that device see table 8.8

8.7 Micro port timing reference guide

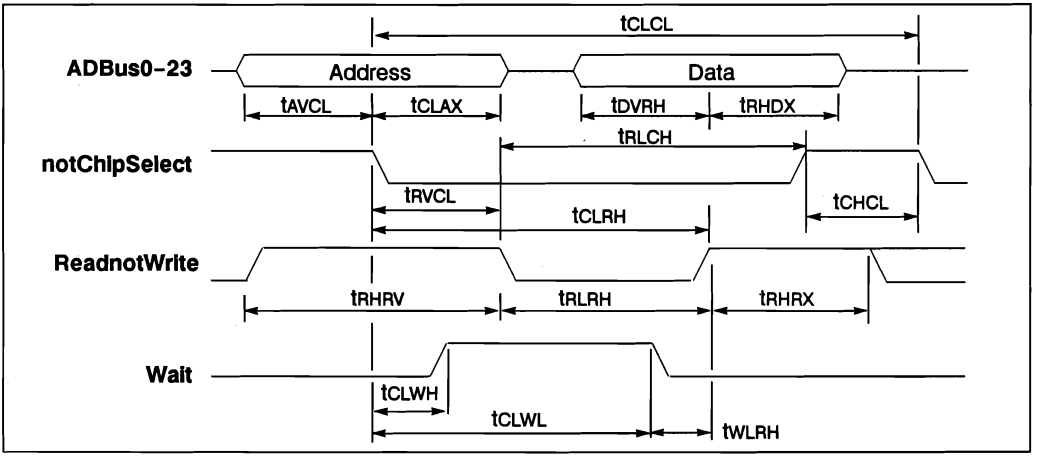


Figure 8.2 Micro port write cycle

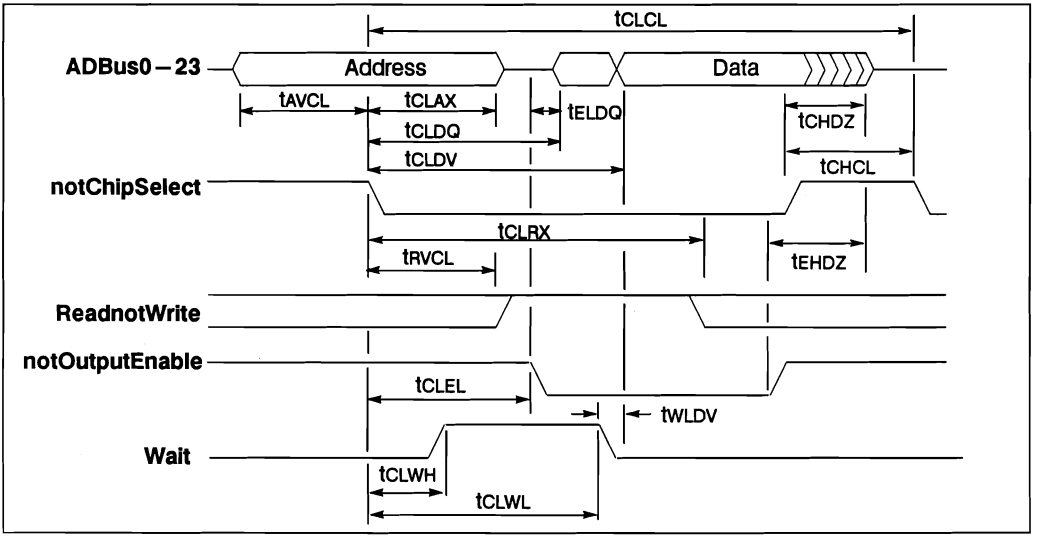


Figure 8.3 Micro port read cycle

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	20		ns
tCLAX	Address hold time	10		ns
tRVCL	**ReadnotWrite** setup time	-1		periods SClk
tCLRH	**ReadnotWrite** hold time	3		periods SClk
tRLRH	**ReadnotWrite** low time	2		periods SClk
tRLCH	**ReadnotWrite** low to **notChipSelect** high	2		periods SClk
tDVRH	Write data setup time	20		ns
tRHDX	Write data hold time	10		ns
tCLCL	Cycle time	4		periods SClk
tCLWH	**notChipSelect** low to wait high	0	20	ns
tCLWL	**notChipSelect** low to wait low	3		periods SClk
tWLRH	**ReadnotWrite** hold time	0		ns
tRHRX	**ReadnotWrite** high time	1		periods SClk
tCHCL	**notChipSelect** high time	2		periods SClk
Note: These figures are not characterised and are subject to change				

Table 8.4 Micro port write cycle parameters

Symbol	Description	Min.	Max.	Unit
tAVCL	Address setup time	20		ns
tCLAX	Address hold time	10		ns
tRVCL	**ReadnotWrite** setup time	-1		periods SClk
tCLRX	**ReadnotWrite** hold time	3		periods SClk
tCHDZ	Output hold time from **notChipSelect**	5	20	ns
tELDQ	Output turn on delay		20	ns
tEHDZ	Output hold time from **notOutputEnable**	5	20	ns
tCLEL	**notChipselect** to **OutptEnable** delay	20		ns
tCLDV	**notChipselect** access time		4 SClk + 10	ns
tCLCL	Cycle time	7		periods SClk
tCLWH	**notChipSelect** low to wait high	0	20	ns
tCLWL	**notChipSelect** low to wait low	4 SClk + 10		ns
tWLDV	Wait to data valid		10	ns
tCHCL	**notCS** high time	2		periods SClk
Note: These figures are not characterised and are subject to change				

Table 8.5 Micro port read cycle parameters

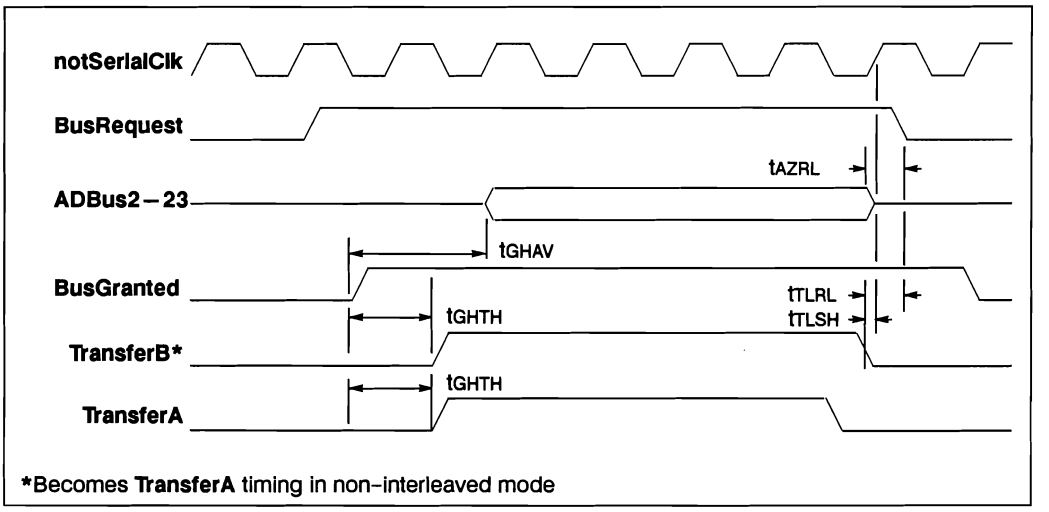


Figure 8.4 Micro port DMA and data transfer timings

Symbol	Description	Min.	Max.	Unit
tSHRH	**notSerialClk** to **BusRequest** skew	-5	5	ns
tGHTH	**BusGranted** high to **Transfer** high	15	30	ns
tGHAQ	**Transfer** address turn on delay	15		ns
tGHAV	**Transfer** address access time		4 SClk + 15	ns
tTLSH	**Transfer** to **notSerialClk** skew	-5	5	ns
tTLRL	**Transfer** to **BusRequest** low	1 SClk	1 SClk + 15	ns
tTLAZ	**Transfer** address hold time	0		ns
tRLCL	**BusRequest** low to **Chipselect** low	0		ns
tAZRL	Address hi-Z to **BusRequest** low	1 SClk-10		ns
Note: These figures are not characterised and are subject to change				

Table 8.6 Micro port DMA and transfer timing parameters

Symbol	Description	Min.	Max.	Unit
tΔSync	**VSync** to **CSync** skew	-5	5	ns
tΔASync	Digital **CSync** to analogue **CSync** skew	TBD	TBD	ns
tΔABlank	Digital **CBlank** to analogue **CBlank** skew	TBD	TBD	ns
Note: These figures are not characterised and are subject to change				

Table 8.7 Micro port **Sync** and **Blank** timing parameters

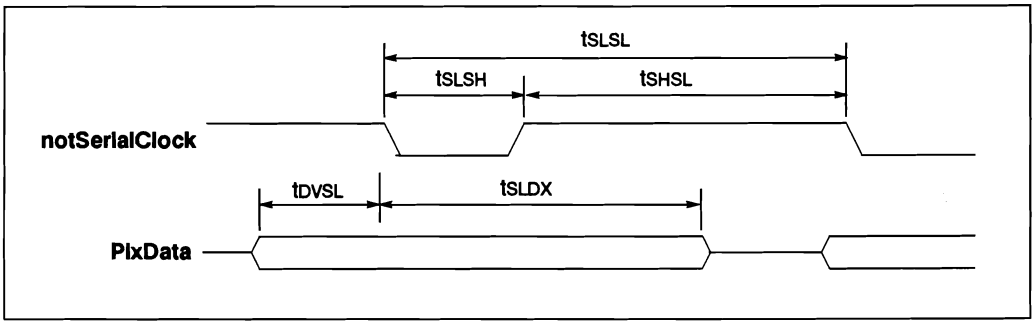


Figure 8.5 Pixel port timing diagram

Symbol	Description	-66	-85	-100	-110	Unit
tSLSL	**notSerialClk** period	61	47	40	36	ns
tSLSH	**notSerialClk** low time	10	10	10	10	ns
tSHSL	**notSerialClk** high time	10	10	10	10	ns
tDVSL	Data set up time	1	1	1	1	ns
tSLDX	Data hold time	9	9	9	9	ns
Note: These figures are not characterised and are subject to change						

Table 8.8 Pixel port timing parameters

8.8 Video Timing Generator

The Video Timing Generator is a programmable finite state machine. It provides composite sync and blanking to the on-chip video DACs, it controls the timing of **BusReq** and **TransferA/B** and it starts and stops **notShiftClkA/B** to control the flow of pixel data. It also provides **FrameInactive** which is asserted during frame flyback enabling the controlling processor to perform screen updates invisibly, and **CBlank** which is asserted during frame or line flyback.

The timing generator can be configured to control an interlaced or non-interlaced monitor, and to generate the synchronising waveforms required by the EIA-343 (NTSC) and CCIR (PAL) studio television standards. These options are selectable in software and are controlled by the contents of the control register. Also controlled by this register is the operating mode of the device. it can be set to free run, in which case it will drive the synchronising signals out, or it can be set into slave mode when it will lock onto externally supplied vertical and horizontal sync pulses.

Programming of the timing generator is achieved by writing a set of screen description parameters to the timing registers. Its resolution is one quarter that of the individual pixels hence the scan lines must be described in 'screen units' of four pixels each. (i.e. a line with 1024 pixels is described as having 256 screen units.)

8.8.1 The display screen

In a raster scan display system, the picture is built up of a number of visible lines, which are displayed and a much smaller number of frame flyback lines, which are blanked. Each of the displayed lines has a single, visible, display period and a blanked line flyback period made up of front and back porch plus line sync. The total linetime is the sum of the displayed and blanked periods.

The frame timing periods are specified in multiples of half a linetime while the line timings are specified in screen units of four pixels duration each.

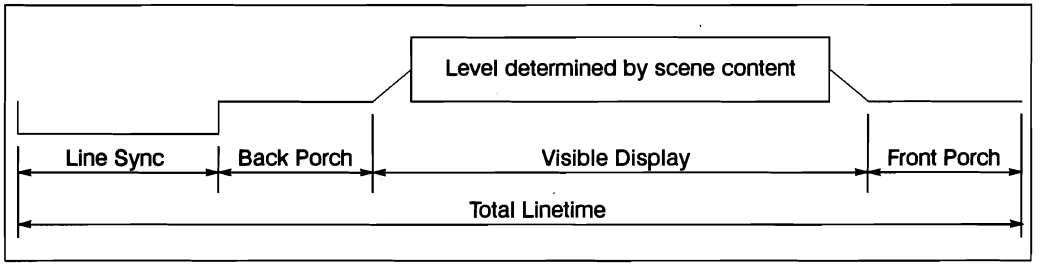


Figure 8.6 Scan line segments

Each displayed scan line of the raster is built up of the sections shown in figure 8.6. The visible portion is contained within the period 'display', so that, if a screen width of 1024 visible pixels (equal to 256 screen units) is required, then 256 is the number written to the 'display' register. For the remainder of the scan, the display is in line flyback and is therefore blanked.

The total linetime is the sum of all the sections of figure 8.6 and this is the number written to the 'linetime' register.

8.8.2 Line timing parameters

The line segments shown in figure 8.6 map directly to timing generator registers with two exceptions. First, the line synchronising pulse is split into two periods of equal duration which are used in immediate succession – the parameter used for this is 'halfsync' – and second, there is no register for frontporch, rather the total line time is programmed into a separate register and the end of the scan line occurs when this timebase period expires.

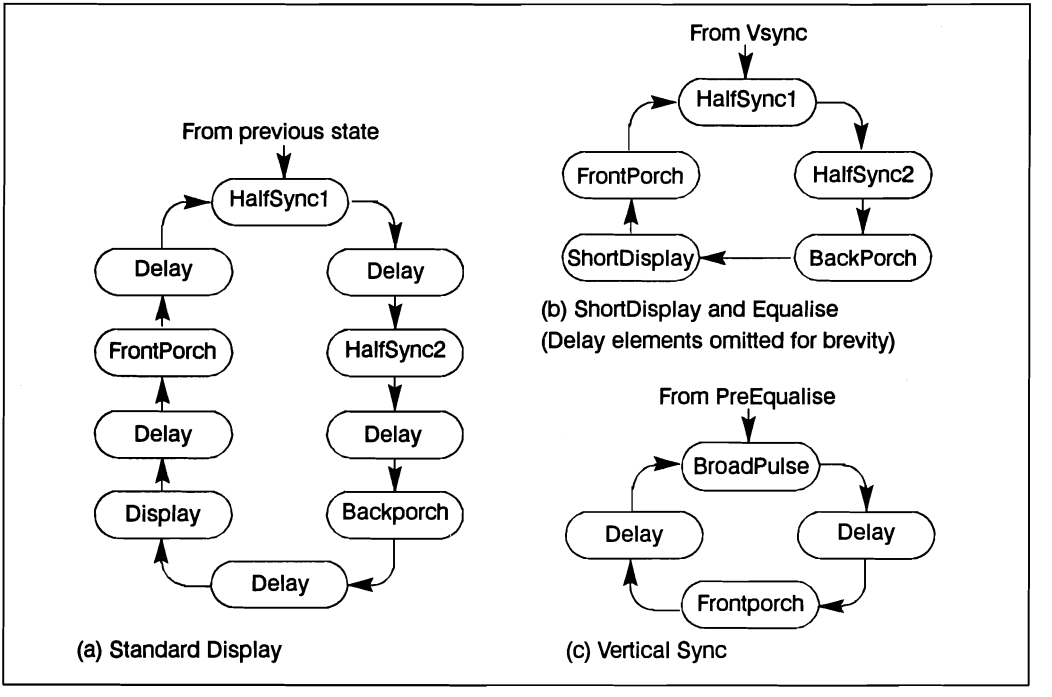


Figure 8.7 Flow diagrams for video timing generator

Figure 8.7 (a) shows the flowchart of a standard displayed or blanked scan line (as distinct from the truncated unscanned lines used in vertical sync and equalisation). The state machine proceeds from one state

to the next according to the delay programmed in by the user; on entering a new state the Sync and blanking outputs are modified depending on which part of the cycle is being executed.

Figure 8.8 (a) shows the relationship of the screen description parameters to a full scan line. Note that front-porch is undefined and halfsync is used twice in succession to construct the line sync pulse.

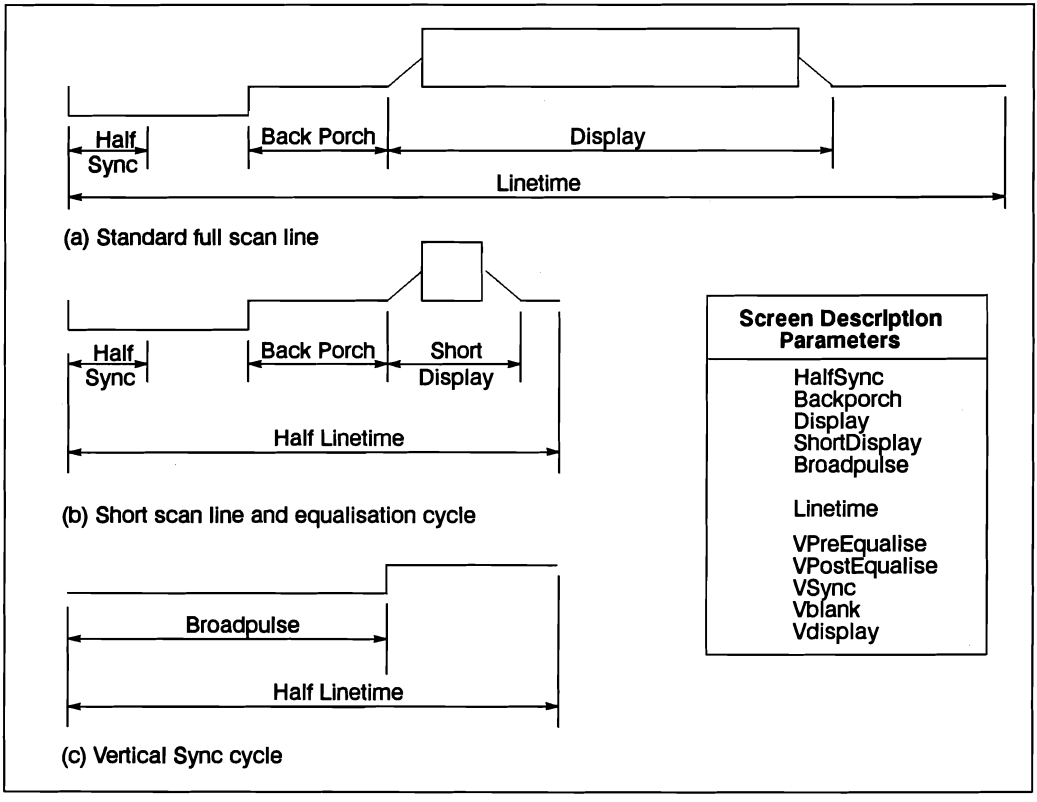


Figure 8.8 Screen description parameter definitions

8.8.3 Frame timing parameters

The G364 generates synchronising signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating the ordinary frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tesselated sync signals for an interlaced television system (see figure 8.9).

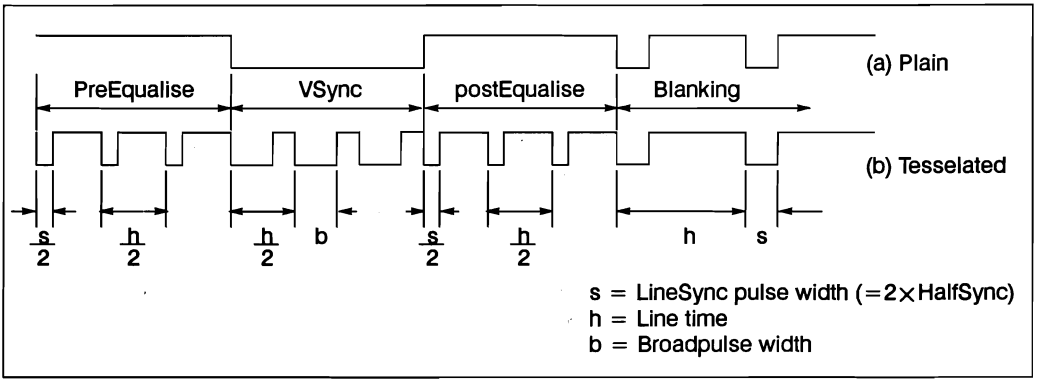


Figure 8.9 Composite Sync frame flyback waveforms

A further requirement of the television standards is that each frame must contain an odd number of scan lines. As a result, the frame timing parameters need to be specified in terms of half line times. Thus a non-interlaced screen of 1024 visible lines has the value 2048 written to the VDisplay register. (An interlaced screen of 625 lines would have 625 in that register since in interlace, the VDisplay register decribes the vertical display *field* rather than the entire frame – see table 8.9).

Screen Type	Lines per Frame	Value in VDisplay Register	Lines per Field
non-Interlace	1024	2048	1024
Interlace	1024	illegal	illegal
non-Interlace	625	1250	625
Interlace	625	625	312.5

Table 8.9 Frame programming examples

The duration of preEqualise, postEqualise, VSync and VBlank are also defined as multiples of half lines. The total frame blanking period is the sum of these four.

In order to generate the tesselated equalisation and blanking waveforms shown in figure 8.9(b), some additions to the basic line parameters are needed. The low period during VSync is defined as 'broadpulse' with its duration stored in the 'broadpulse' register. The shorter low period during pre and post equalisation is equal to half the line sync period and hence uses the value stored in the 'halfsync' register.

Reference to figure 8.9(b) and (c) shows that, on entering frame flyback, the state machine loop shortens to give a period of half a linetime. In equalisation, this is achieved simply by substituting 'shortdisplay' for 'display' in the sequence, whereas in vsync the sequence is changed to include only 'broadpulse' and 'frontporch'.

8.8.4 Parameter calculation

Calculation of the frame timing parameters is simple and direct – to produce the flyback waveform in figure 8.9(a) the parameters VSync, preEqualise and postEqualise are set to 3 – and the line parameters are derived from the equations in table 8.10.

During a full line cycle (VBlank, VDisplay)		
Halfsync	=	Horizontal Sync/2
BackPorch	=	BackPorch
Display	=	Display
Linetime	>	(2×HalfSync + BackPorch + Display)
During an equalisation cycle		
ShortDisplay	<	Linetime/2 – (2×HalfSync + BackPorch)
Low period	=	HalfSync
High period	=	Linetime/2 - HalfSync
During a VSync cycle		
BroadPulse	=	Linetime/2 - Pulse width*
Low Period	=	BroadPulse
High period	=	Pulse width

Table 8.10 Screen description line parameter equations

* Note: Pulse width = duration of serration pulse high time

The following restrictions on parameter values must be observed:

- All parameters must be greater than 1.
- Linetime must be an even multiple of the period of **notSerialClk**.
- 2×HalfSync + BackPorch + Display > Linetime/2 > 2×HalfSync + BackPorch.
- The total number of displayed lines in each frame must be a whole number. In interlace, this must be an odd whole number.
- Backporch must exceed TransferDelay by at least one **notSerialClk** period; also it must exceed 16 SClk periods in total.
- Transfer delay must not exceed ShortDisplay.

(The parameter TransferDelay is described in section 8.10.4).

8.8.5 The startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is accomplished while the timing generator is disabled.

On startup, after reset, the host processor must write a configuration pattern to the G364 bootstrap location. The effect of this is to set the PLL multiplication factor, clock source (PLL or external crystal) and microport address alignment. It must then initialise the VTG by writing a 0 to bit 0 in control register A.

Startup sequence:

1 Assert, then deassert **Reset**.
—Wait 50ns

2 Write configuration pattern to bootstrap location.

3 Write to control register to initialise VTG.

After this the screen parameters and colour table data can be written to the appropriate locations in any order. The processor must then make another write to the control register to enable the VTG which will then start up immediately at the beginning of frame sync. The G364 can be reprogrammed without asserting Reset.

The reprogramming sequence has three steps:

1 Write zero to bit 0 of the control register, disabling VTG.

2 Write to the screen parameter registers chosen for redefinition.

3 Write one to bit 0 of the control register, (redefining modes if necessary by modifying the relevant register bits) and enabling the VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed the full startup procedure must be followed, including reset.

8.9 Synchronising and blanking signals

8.9.1 Introduction

The video timing generator produces sync and blank signals to a pattern specified by a combination of the operating mode of the G364 and the screen description parameters. Internally, composite sync and blank are supplied to the three DACs by default. However, both of these functions can be disabled by setting bits 6 and 11 of Control RegisterA, respectively.

The internal sync and blank signals are automatically scheduled according to the operating mode. An additional programmable delay of 0 – 7 serial clock cycles may be added to sync and blank if it is required to add pipeline delays in the pixel path.

8.9.2 Master mode

When running in master (internal sync) mode, the **notVSync** and **notCorHSync** pins are outputs and the G364 drives them active low. Untesselated frame sync always appears on the **notVSync** pin, while the **notCorHSync** pin is switchable to supply one of line sync, plain composite sync, or tesselated composite sync:

Register Bits		notVSync	notCorHSync	
5	4		notHSync	notCSync
0	0	Plain	-	Tesselated
0	1	Plain	-	Plain
1	0	Plain	Plain	-
1	1	Plain	Plain	-

8.9.3 Slave mode

In slave mode, the **notVSync** and **notCorHSync** pins are designated as inputs, and the G364 will use them to determine when to start a frame. In such a scheme two or more devices can be synchronised together.

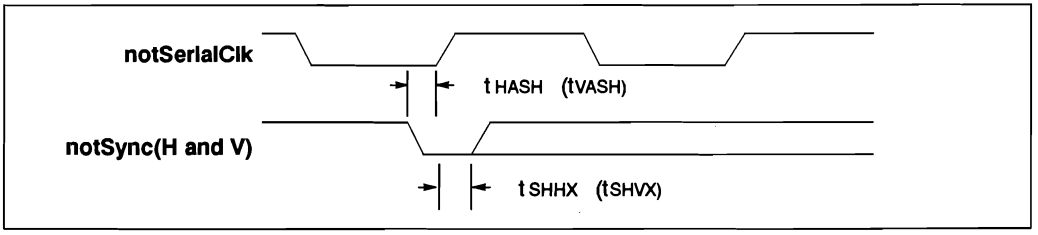


Figure 8.10 External synchronisation

Symbol	Description	Min.	Max.	Unit
tVASH	**notVsync** setup time	SClk/4	3SClk/4	ns
tHASH	**notHsync** setup time	SClk/4	3SClk/4	ns
tSHVX	**notVsync** hold time	0		ns
tSHHX	**notHsync** hold time	0		ns
Note: These figures are not characterised and are subject to change				

Table 8.11 External sync waveform timings

8.10 The micro port

8.10.1 Introduction

The micro port is a bidirectional 24 bit interface, consisting of a multiplexed address and data bus and several control signals. It is used for programming the VTG screen description registers, colour and cursor lookup tables, cursor store, and other registers.

As well as serving as a programming port the interface is also capable of performing a video RAM shift register transfer operation using a fully handshaked DMA. The timing of this operation is synchronous with the pixel port and is arranged so that seamless update of the video RAM shift register is possible.

8.10.2 Word alignment

The IMS G364 is designed for use with 32 and 64 bit processors, and therefore supports both 32 and 64 bit word alignment. With 32 bit alignment selected, the least significant address bit is on **ADBus2**; with 64-bit alignment selected it is on **ADBus3**. This applies both on host processor accesses to the microport and on DMA transfer cycles.

8.10.3 Micro port read/write cycles

Four signals control the flow of address and data in and out of the device on **ADBus0-23**.

Signal	I/O	Function
notChipSelect	I	The falling edge latches the address and samples **ReadnotWrite.** The cycle is initiated. The rising edge terminates the cycle, and tristates the **ADBus** drivers on a read cycle.
ReadnotWrite	I	If this signal is low shortly after **notChipSelect** goes low, the cycle is a write; if it is high the cycle is a read. Additionally on a write cycle, the rising edge of **ReadnotWrite** strobes in the data.
notOutputEnable	I	This signal is used only during read cycles, and enables the read data onto the **ADBus**. It should be kept high at all other times.
Wait	O	Wait eliminates the need for an external wait state generator. It is driven high shortly after **notChipSelect** goes low, and is driven back low when the G364 is ready for write data to be strobed by **ReadnotWrite** or read data is about to become valid on the **ADBus**.

8.10.4 DMA transfer operation

The IMS G364 provides three signals; **BusReq**, **TransferA** and **TransferB**, to control the synchronous reloading of the VRAM shift registers. Both **TransferA** and **TransferB** are used in interleaved mode, **TransferA** only is used in non-interleaved mode.

The G364 asserts **BusReq** to obtain use of the **ADBus** to perform a DMA cycle. The host processor asserts **BusGranted** to acknowledge the request. **TransferA** and **TransferB** (if used) are driven high simultaneously by the G364, and trigger the external generation of RAS, address mux and CAS signals to the VRAMs. **TransferA** goes low synchronous with **notShiftClkA**, and **TransferB** is synchronised to **notShiftClkB**. This performs the transfer operation.

The exact time at which the transfer occurs is critical, since mid-line updates must be seamless. The time taken from assertion of **BusReq** to the transfer taking place is a sum of various system delays, some of which are variable. The parameter **Transfer Delay** (Micro port address #X02D) must be set thus:

Transfer Delay $\geq$ The maximum possible system DMA latency + VRAM access + 4 SClk

The G364 has a further requirement, that:

TransferDelay $\leq$ Backporch -1

to ensure that there is data loaded ready for the first scan line to begin.

Another parameter, **MemInit** (Microport Address #X02C), determines the frequency of DMA transfer cycles. The sum of **MemInit** and **TransferDelay** defines the interval between successive Bus Requests.

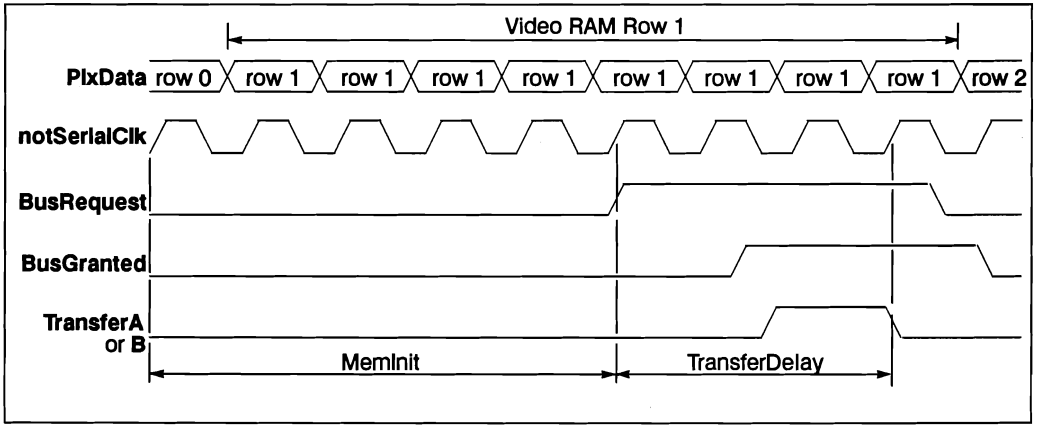


Figure 8.11 Data transfer sequence

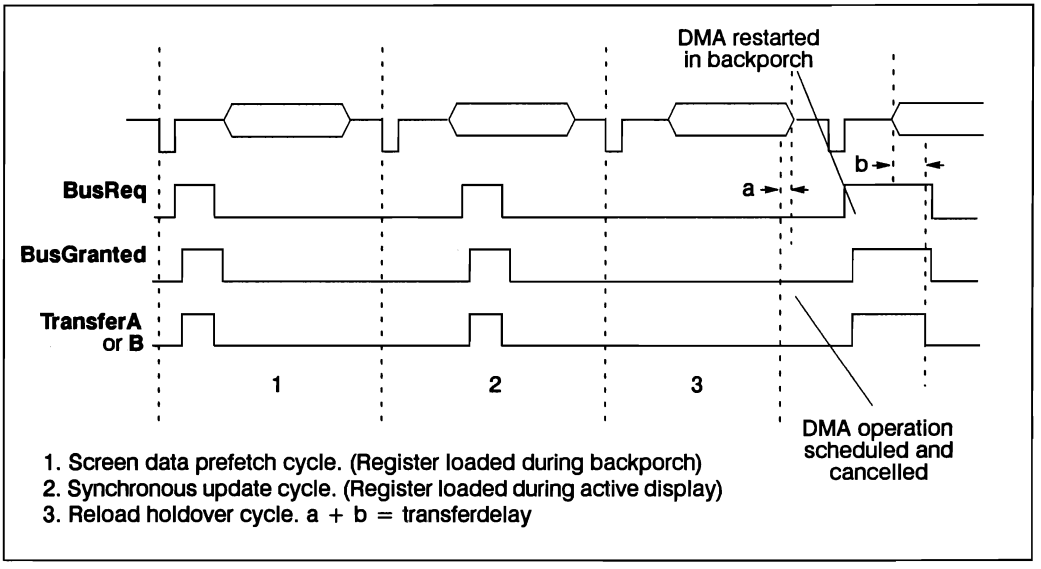


Figure 8.12 Data transfer operational behaviour

Figure 8.11 shows the sequence of events during a synchronised VRAM row transfer operation performed by the G364 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers.

8.10.5 VRAM address Increment

To allow either the existing VRAM row or column address latches to be used for the row address during DMA transfer cycles, several address increments are provided, both for interlaced and non-interlaced modes. They are selected from Control Register A.

Register Bit			Description	Format	Second field
13	12	1			
0	0	0	Increment by 1.	Non-interlace format.	
0	0	1	Increment by 1.	Interlace format.	Every second field offset by 1.
0	1	0	Increment by 256.	Non-interlace format.	
0	1	1	Increment by 2.	Interlace format.	Every second field offset by 1.
1	0	0	Increment by 512.	Non-interlace format.	
1	0	1	Increment by 512.	Interlace format.	Every second field offset by 256.
1	1	0	Increment by 1024.	Non-interlace format.	
1	1	1	Increment by 1024.	Interlace format.	Every second field offset by 512.

Table 8.12

8.10.6 FrameInactive

A further timing signal, **FrameInactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **FrameInactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

8.11 The pixel port

The 32 bit pixel port takes in pixel data from the video RAM and has various modes of operation.

8.11.1 Interleaved/non-interleaved operation

Because of the very high video rates supported by the G364 it is not possible in some situations to supply pixel data fast enough from a single bank of video RAMs. An interleaved mode has been provided to allow two banks of VRAM to be used, each running at half the frequency required when using one bank. 64 bits of pixel data are loaded alternately from one VRAM bank then the other.

In interleaved mode, two **notShiftClk** and two **Transfer** signals are used to control the two banks, the shift clocks running in anti-phase. **notShiftClkA** and **TransferA** control the lower numbered pixels, and not-**ShiftClkB** and **TransferB** control the higher numbered pixels. On DMA transfer cycles both banks have their shift registers reloaded, which means that these cycles are required at half the frequency compared with non-interleaved mode.

In non-interleaved mode only **notShiftClkA** and **TransferA** are used—24 bits per pixel mode is not available.

8.11.2 Pixel sampling

The point at which pixels are sampled by the G364 varies according to the pixel mode selected (refer to section 8.11.3). In 15 and 16 bit per pixel non-interleaved mode and 24 bit per pixel interleaved mode, pixels are sampled one not serial clock period **(SClk)** after **notShiftClkA** or **B.** In all other modes sampling is optionally delayed by a further 1/2 **ShiftClk**.

8.11.3 Pixel multiplexing

The G364 supports 7 pixel modes in interleaved mode and 6 in non-interleaved mode selected from control register A, as follows:

Non-interleaved mode

Register bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
1	0	1	0	16	1 SClk	4:1	Gamma corrected true colour
1	0	0	0	15	1 SClk	4:1	Gamma corrected true colour
0	1	1	0	8	2 SClks	8:1	Pseudo colour
0	1	0	0	4	4 SClks	16:1	Pseudo colour
0	0	1	0	2	8 SClks	32:1	Pseudo colour
0	0	0	0	1	16 SClks	64:1	Pseudo colour

Interleaved mode

Register bits				Bits per pixel	ShiftClk period	MUX ratio	Use of LUT
22	21	20	18				
1	1	0	1	24	1 SClk	2:1	Gamma corrected true colour
1	0	1	1	16	2 SClks	4:1	Gamma corrected true colour
1	0	0	1	15	2 SClks	4:1	Gamma corrected true colour
0	1	1	1	8	4 SClks	8:1	Pseudo colour
0	1	0	1	4	8 SClks	16:1	Pseudo colour
0	0	1	1	2	16 SClks	32:1	Pseudo colour
0	0	0	1	1	32 SClks	64:1	Pseudo colour

8.11.4 True colour modes (15, 16 and 24 bits per pixel)

The incoming pixel data is split into red, green, and blue fields as illustrated in figure 8.13. The colour modes bypass the mask register.

Each colour field addresses the LUT which may contain a suitable gamma correction table for that colour. The unused LUT address bits in 15 and 16 bit per pixel modes are the lowest order bits, which avoids the need to change the gamma-correction table when switching between true colour modes. If no gamma correction is required the LUT must be written with data = address.

24 bits per pixel mode

Ports A, B and C supply the first-displayed pixel of each pixel pair, ports E, F and G supply the second. Pixel data on ports D and H is ignored. Ports A and E supply blue data, B and F supply green data, and C and G supply red data.

16 bits per pixel mode

Each pair of pixel ports (A and B, C and D, E and F, G and H) supplies a 16 bit per pixel value. The pixel from ports A and B is displayed first and the pixel from G and H is displayed last. Of each 16 bit value, bits 0–3 are blue, 4–9 are green and 10–15 are red.

15 bits per pixel mode

Each pair of pixel ports (A and B, C and D, E and F, G and H) supplies a 15 bit per pixel value. The pixel from ports A and B is displayed first and the pixel from G and H is displayed last. Of each 15 bit value, bits 0–4 are blue, 5–9 are green and 10–14 are red. Bit 7 of ports B, D, F and H is unused.

Port	A	A	A	A	A	A	A	A		B	B	B	B	B	B	B	B		C	C	C	C	C	C	C	C		D	D	D	D	D	D	D	D
Port	E	E	E	E	E	E	E	E		F	F	F	F	F	F	F	F		G	G	G	G	G	G	G	G		H	H	H	H	H	H	H	H
Bit	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7

24bpp

Pixel	Pixel 0 and 1																															
Colour	B	B	B	B	B	B	B	B		G	G	G	G	G	G	G	G		R	R	R	R	R	R	R	R		X	X	X	X	X	X	X	X
Bit	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7		–	–	–	–	–	–	–	–

16bpp

Pixel	Pixel 0 and 2																Pixel 1 and 3															
Colour	B	B	B	B	G	G	G	G		G	G	R	R	R	R	R	R		B	B	B	B	G	G	G	G		G	G	R	R	R	R	R	R
Bit	0	1	2	3	0	1	2	3		4	5	0	1	2	3	4	5		0	1	2	3	0	1	2	3		4	5	0	1	2	3	4	5

15bpp

Pixel	Pixel 0 and 2																Pixel 1 and 3															
Colour	B	B	B	B	B	G	G	G		G	G	R	R	R	R	R	X		B	B	B	B	B	G	G	G		G	G	R	R	R	R	R	X
Bit	0	1	2	3	4	0	1	2		3	4	0	1	2	3	4	–		0	1	2	3	4	0	1	2		3	4	0	1	2	3	4	–

Key: R = Red, G = Green, B = Blue and X = bit not used

Figure 8.13 Pixel mapping diagram

8.11.5 Pseudo colour modes (1, 2, 4 and 8 bits per pixel)

The pixel data is latched from ports A, B, C, D, E, F, G and H and displayed in that order. Each pixel is masked by 8 bits of the mask register before the output is used to address all three LUTs which contain the pseudo colour palette.

8 bits per pixel mode:

Each port supplies 1 pixel. Bits 0–7 of the port correspond to LUT address bits 0–7 respectively. All 256 locations in the LUT are used.

4 bits per pixel mode:

Each port supplies 2 pixels. Bits 0–3 of the port are the first pixel displayed, bits 4–7 are the second pixel displayed. Both correspond to LUT address bits 0–3 respectively. Only locations 0 to 15 of the LUT are used.

2 bits per pixel mode:

Each port supplies 4 pixels. Bits 0–1 of the port are the the first pixel displayed, bits 6–7 the last pixel displayed. Each pair of pixel inputs corresponds to LUT address bits 0–1. Only locations 0 to 3 of the LUT are used.

1 bit per pixel mode:

Each port supplies 8 pixels. Bit 0 of the port is the first pixel displayed, bit 7 the last pixel displayed. Each pixel input corresponds to LUT address bit 0. Only locations 0 and 1 of the LUT are used.

8.11.6 Mask register

(micro port address #X040)

The 24 bit mask register masks the pseudo colour pixel inputs to the three LUTs. Bits 0–7 mask the blue data, 8–15 the green data, and 16–23 the red data. Setting a bit in the mask register to zero causes the corresponding LUT address bit to be set to zero.

8.12 Hardware cursor

The G364 hardware cursor consists of a 64×64×2 bit RAM, addressed as a sequence of consecutive 16 bit words. Each word is formatted into 8 pixels as below, and is randomly addressable at any time.

Pixel	7		6		5		4		3		2		1		0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Cursor position is held in a single 24 bit register as an x-y location relative to the top left of the screen. The position defined is that of the topmost, leftmost pixel of the cursor. The most significant half of the cursor position word (bits 12-23) is its x-address (horizontal position) and the least significant half (bits 0-11) is its y-address (vertical position). The cursor position is held in the CursorStart register at microport address #X0C7. The x-address and y-address are two's complement values in the range -64 to 2303.

The 2 bit cursor pixels address a 3 location cursor look-up table as follows:

Pixel value	Format
0 0	Cursor transparent. Background colour displayed.
0 1	Colour from cursor LUT location 1
1 0	Colour from cursor LUT location 2
1 1	Colour from cursor LUT location 3

The cursor is enabled/disabled via bit 23 in Control RegisterA.

8.13 Anti-sparkle colour palette

The IMS G364 includes a 256×24bit colour look-up table which is mapped directly into the micro port address space. Complete colour values are written by a single write cycle on the micro port. In order to minimise picture disturbance whilst a colour palette entry is being accessed, the previous pixel is repeated at the DACs.

8.14 Checksum registers

There are three 24 bit checksum registers, one for each colour channel. Their purpose is to facilitate testing the device and systems containing it. The checksum is located directly before the DACs, and after the colour and cursor palettes. The checksum value is dependent on the cursor position and whether or not interlaced mode is selected, but independent of sync modes and flyback patterns.

The checksum registers are reset by the falling edge of **FrameInactive**. They accumulate only those pixels which are visible on the screen, i.e. those pixels which are unblanked. The registers should be read during the first part of frame flyback. At the end of this period they are being reset, and at other times they are being accumulated and are consequently invalid.

The checksum registers are addressed from the microport as 24 bit words containing low, middle and high bytes, as follows:

Micro port address	Bits 16-23	Bits 8-15	Bits 0-7
#X0C0	Red bits 0-7	Green bits 0-7	Blue bits 0-7
#X0C1	Red bits 8-15	Green bits 8-15	Blue bits 8-15
#X0C2	Red bits 16-23	Green bits 16-23	Blue bits 16-23

8.15 Clocks

The IMS G364 has two alternate clocking schemes. The primary clocking system uses a phase locked loop (PLL) on the chip to multiply up the low frequency (<10MHz) input clock to the required video data rate. Alternatively a full dot-rate clock may be supplied (×1 mode).

8.15.1 PLL mode

In PLL mode, a 1μF capacitor must be connected between **CapPlus** and **CapMinus.** A ceramic capacitor is preferred, with an impedance of less than 3Ω between 100kHz and 10MHz. If a polarised capacitor is used, the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm.

The multiplication factor is determined from the binary value written to bits 0..4 of the boot location (#X000). Values from 5 to 31 are permitted. Also, the clock source select bit (bit 5) in the Boot Location (#X000) must be set to a '1'.

ClockIn must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. ClockIn must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits.

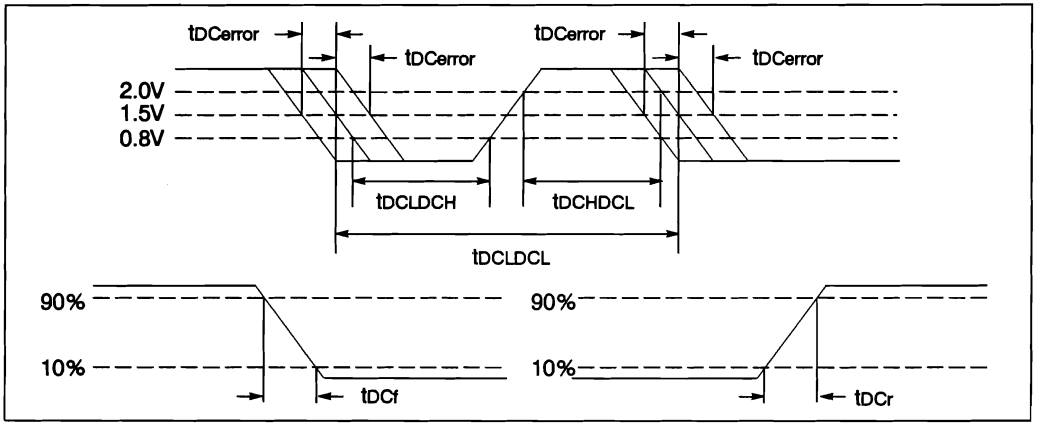


Figure 8.14 ClockIn timing

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
tDCLDCH	ClockIn pulse width low	20			ns	
tDCHDCL	ClockIn pulse width high	20			ns	
tDCLDCL	ClockIn period	100		200	ns	1
tDCerror	ClockIn timing error			±0.015	%	2
tDCr	ClockIn rise time			10	ns	3
tDCf	ClockIn fall time			8	ns	3
Note: These figures are not characterised and are subject to change						

Table 8.13 ClockIn timings in PLL mode

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their normal times.

3 Clock transitions must be monotonic within the range **VIH** to **VIL**.

Note: These figures are not characterised and are subject to change.

8.15.2 'Times 1' mode

The external ×1 clock can be selected in one of two ways. Either the terminals **CapPlus** and **CapMinus** should be shorted together, or the clock source select bit in the boot location should be written to a '0'.

8.16 The video DACs

8.16.1 General

The video DACs have 8 bit resolution, and are designed to drive a doubly terminated 75Ω transmission line and produce analogue outputs compatible with RS170 and RS343 video standards.

The DACs work by sourcing a current proportional to their digital input. The DAC unit current for each digital increment is defined by an external **Iref** current source;

$$1\ \text{DACunit} = \textbf{Iref}/120$$

The video information output by each gun ranges from 0 to 255 units under the control of the digital input from the colour palette or the pixel pin.

A sync pedestal of 108 DAC units and a blanking pedestal of 20 DACunits are provided. The sync pedestal allows superposition of the sync timing signals on the video outputs. The blanking pedestal ensures that no visible trace appears on the screen during flyback.

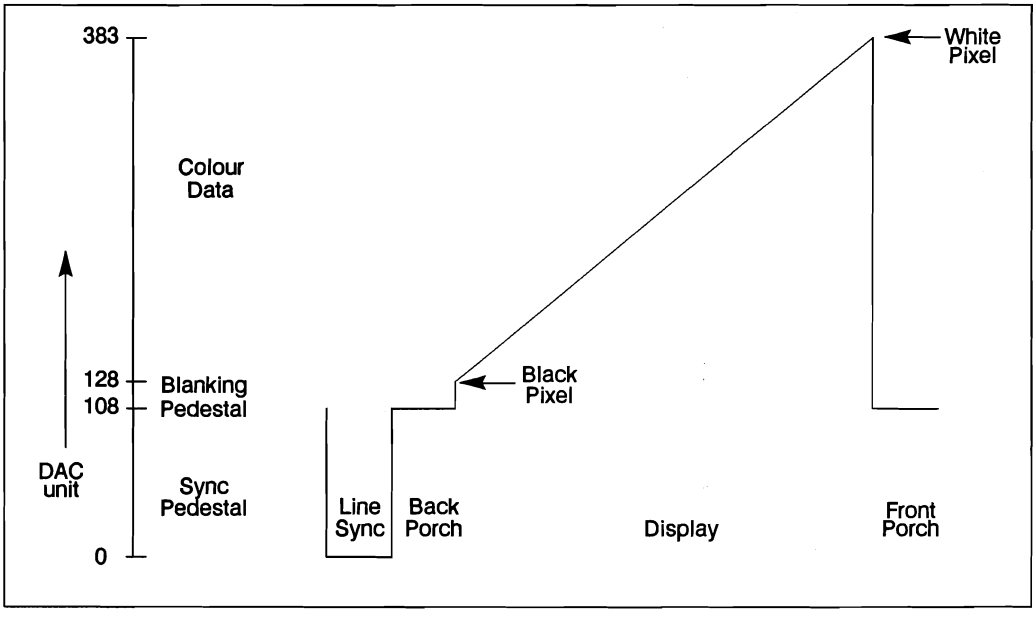


Figure 8.15 DAC output levels

8.16.2 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
	Resolution	8	8	8	bits	
VO(max)	Output voltage			1.5	V	2
IO(max)	Output current			34	mA	VO≤1V
	Full scale error			± 5	%	2, 3
	Sync pedestal error			±10	%	2
	Blank level pedestal error			±10	%	2
	DAC to DAC correlation error			± 2.5	%	2, 4
	Integral Linearity error			± 1	LSB	2, 5
	Glitch Energy		75		pVSec	2, 6, 7
Iref	Reference current	7		10	mA	
Vref	Reference voltage	VDD −3V		VDD	Volts	
Note: These figures are not characterised and are subject to change						

Notes

1 All voltages with respect to **GND** unless specified otherwise.

2 Tested over the operating temperature range and at nominal supply voltage with **Iref** = −8.88mA.

3 From the value predicted by the design equation, sync and black level pedestals off.

4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.

5 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

6 Load = 37.5Ω +30 pF with **Iref** = −8.88mA.

7 This parameter is sampled not 100% tested.

8.16.3 Power supply and reference circuit

8.16.4 Power supply and current reference

It is recommended that a high frequency decoupling capacitor (preferably a chip capacitor) in parallel with a larger tantalum capacitor (22μF to 47μF) be placed between **AVDD** and **GND** to provide the best possible supply to the analogue circuitry of the DACs.

It is further recommended that the IMS G364 be soldered directly into the PCB without using a socket in order to minimise inductance.

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 8.16 shows four designs of current reference.

If the board **VDD** supply is very noisy, then it is advisable to provide a quiet supply for just the IMS G364. This may be done by supplying both **VDD** and **AVDD** through a small inductor (1-5μH). This will act as an ac filter for high frequency noise. However, if this is done care should be taken to ensure the power rating of this inductor is not exceded.

Figure 8.16(d) shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 8.16(a)-(c) are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current **Iref** through a transistor. In circuits 6.28(b) and 6.28(c) the thermal variations in

the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 8.16(c)).

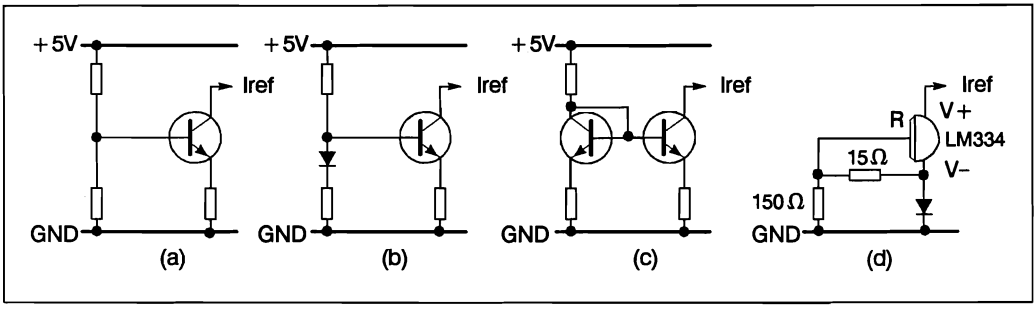


Figure 8.16

8.16.5 Current reference – decoupling

The DACs in the IMS G364 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current **Iref**.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the **Iref** input to **VDD**. This will enable the current reference to track both low and high frequency variations in the supply.

8.16.6 Analogue output – line driving

The G364 is designed to drive a doubly terminated 75Ω line. This arrangement is illustrated in figure 8.17. The effective load seen by the G364 video outputs with this circuit is 37.5Ω.

The connection beteween the DAC outputs on the G364 and the input to the colour monitor should be regarded as a transmission line. Impedance changes along this line will result in reflection of part of the video signal back along the line. These reflections can result in a degradation of the picture displayed by the monitor. To ensure good fidelity RF techniques should be used; in particular the PCB trace from the G364 video output pins to the video sockets on the graphics board should be kept short (less than 3 inches is ideal). If this is done then any reflections due to a mismatched impedance at the video connectors will occur within the risetime of the DAC waveform and will not cause a degradation of the image quality.

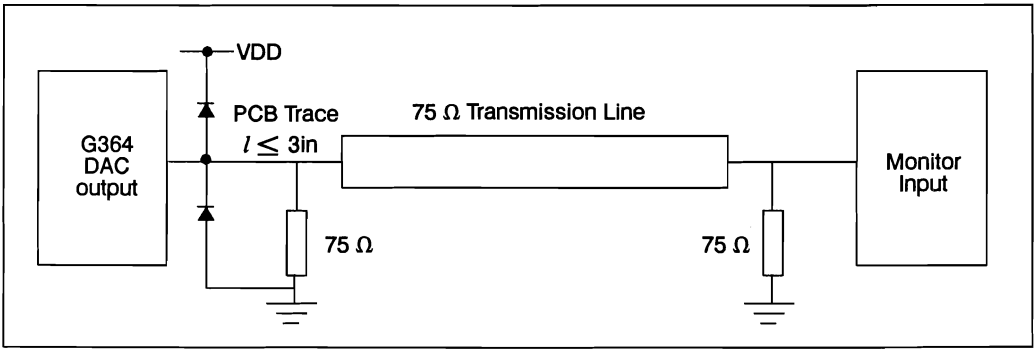


Figure 8.17 DAC output loading

8.16.7 Analogue output – protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G364 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G364 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection diodes to the power rails are recommended at this exposed interface.

8.17 General parametric conditions and characteristics

8.17.1 Absolute Maximum ratings

Symbol	Parameter	Min.	Max.	Units	Notes
AVDD/VDD	DC Supply Voltage		7	Volts	
	Voltage on other pins	Vss–1	VDD + 0.5	Volts	
TS	Storage temperature (ambient)	–65	150	°C	
TA	Temperature under bias	–40	85	°C	
PDmax	Power dissipation		TBD	W	
Iref	Reference current		15	mA	
	Analogue O/P current		45	mA	1
	DC Digital O/P current		25	mA	

Notes

1 Per output

8.17.2 Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	1
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD + 0.5	Volts	
VIL	Input Logic '0' Voltage	–0.5		0.8	Volts	
TPQFP	Case Temperature	TBD		TBD	°C	2
TCQFP	Case Temperature	TBD		TBD	°C	2
Note: These figures are not characterised and are subject to change						

Notes

1 AVDD = VDD

2 Measured on the lid of the package at maximum power dissipation.

8.17.3 Operating characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
IDD	Power Supply Current		TBD	TBD	mA	
IIN	Digital Input Current			±10	µA	
IOZ	TriState Dig Output Current			±50	µA	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	−5			mA	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOL	Output Logic '0' Current	5			mA	
Note: These figures are not characterised and are subject to change						

8.17.4 Output drive capability

Parameter	Min.	Max.	Units	Notes
notShiftClkA		25	pF	1
notShiftClkB		25	pF	1
notSerialClk		25	pF	1
TransferA		25	pF	
TransferB		25	pF	
ADBus [0..23]		25	pF	

Notes

1 **These loadings must be strictly adhered to in order to avoid a degradation in picture quality.**

8.18 Package specifications

8.18.1 132 pin grid array package

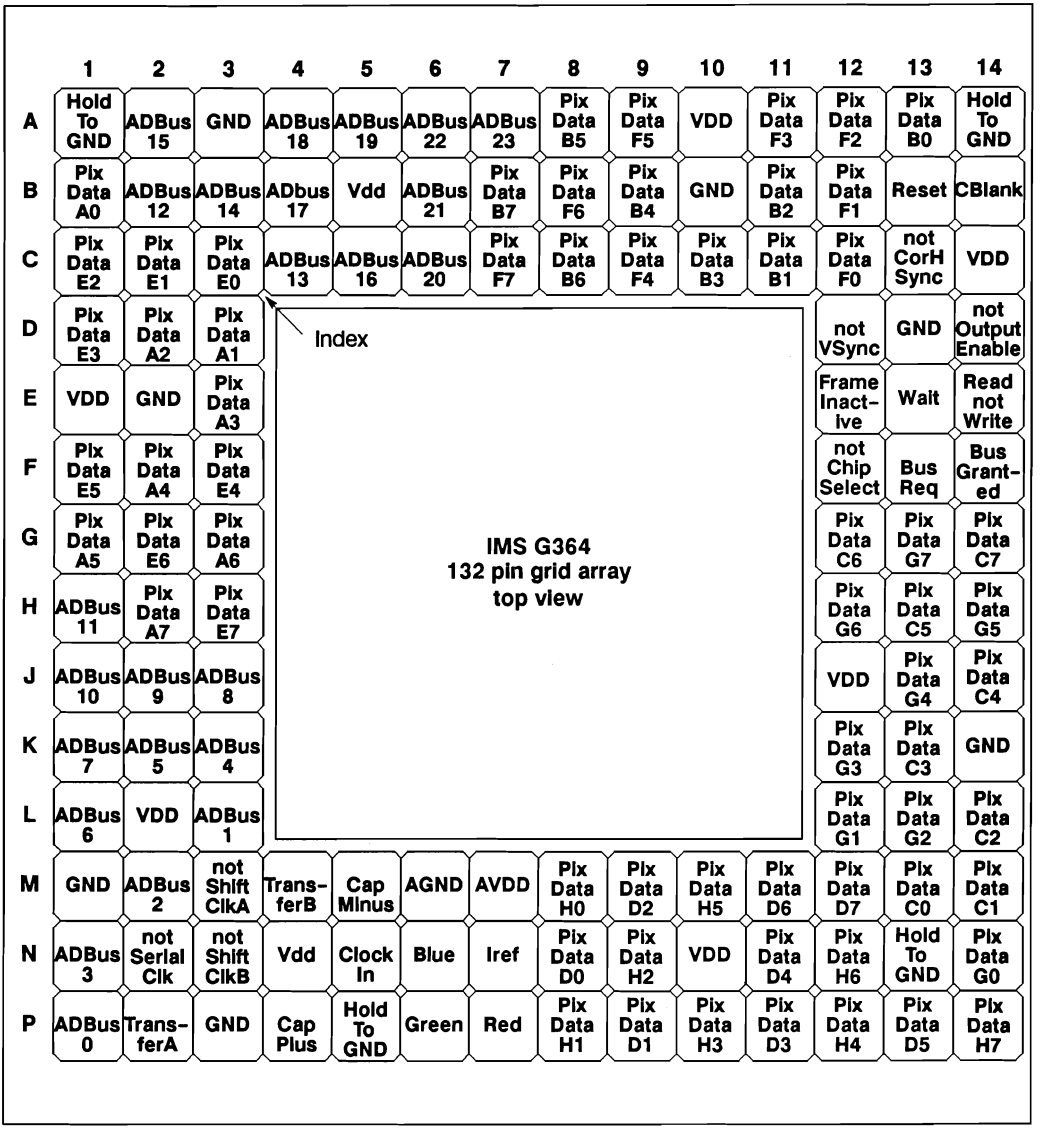


Figure 8.18 IMS G364 pin configuration

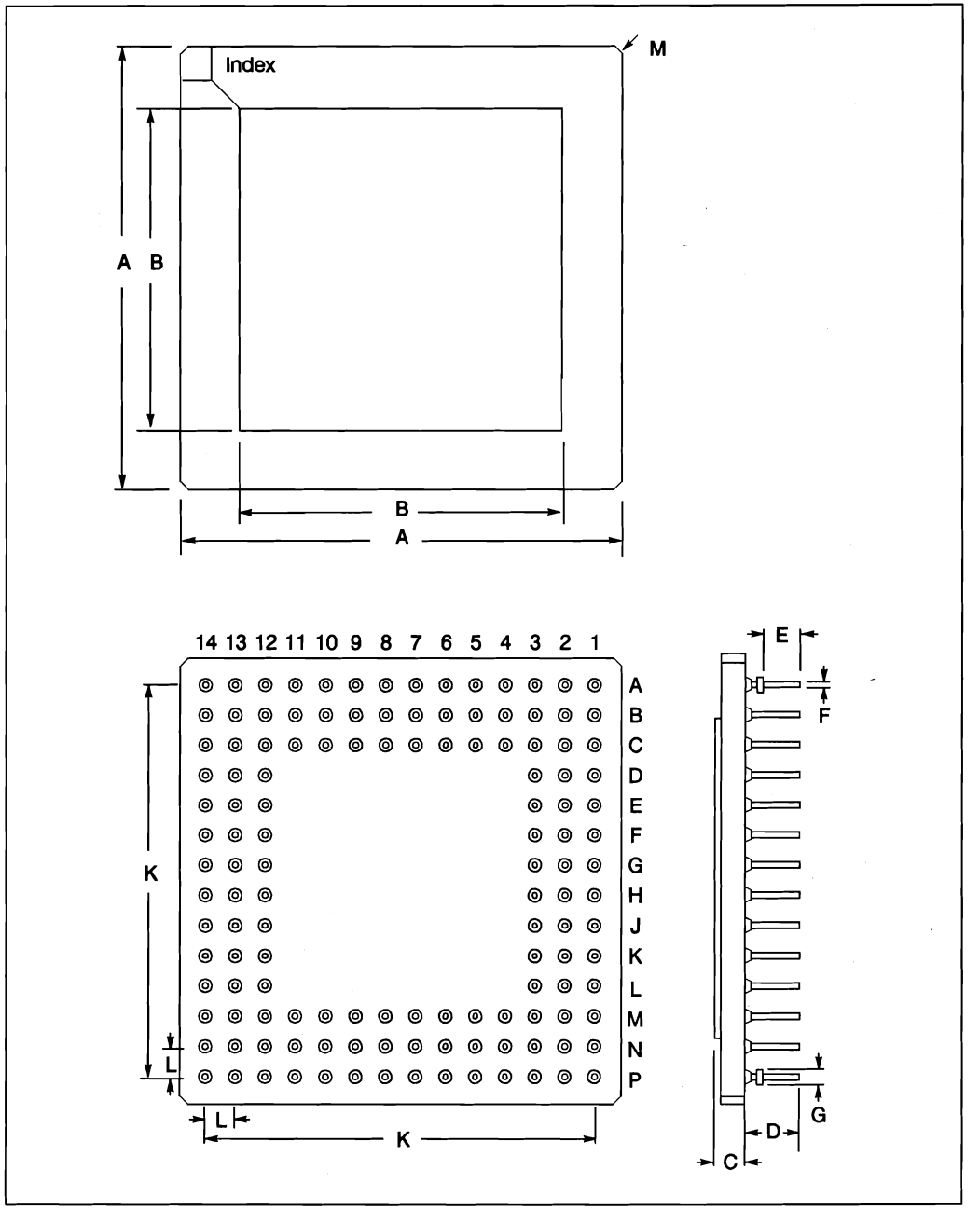


Figure 8.19 132 pin grid array package dimensions

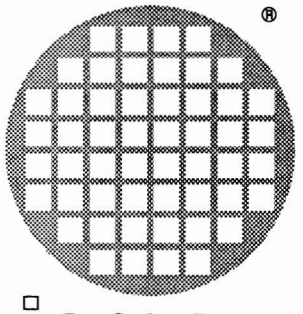
Dim	Millimetres		Inches		Notes
	Min	Max	Min	Max	
A	35.306	35.814	1.390	1.415	
B	17.069	17.474	0.672	0.688	
C	2.134	2.540	0.084	0.100	
D	4.445	4.699	0.175	0.185	
E	3.175	3.429	0.125	0.135	
F	0.406	0.508	0.016	0.020	Pin diameter
G	1.270		0.050		Flange diameter
K	3.277	3.327	1.290	1.310	
L	2.413	2.667	0.095	0.105	
M	0.508		0.020		Chamfer

Table 8.14 132 pin grid array package dimensions

8.18.2 Ordering information

Device	Clock rate	Package	Part number
IMS G364	85 MHz	132 pin grid array	IMS G364G-85S
IMS G364	100 MHz	132 pin grid array	IMS G364G-10S
IMS G364	110 MHz	132 pin grid array	IMS G364G-11S
*IMS G364	135MHz	132 pin grid array	IMS G364G135S
Note: CQFP for this device is currently under development			

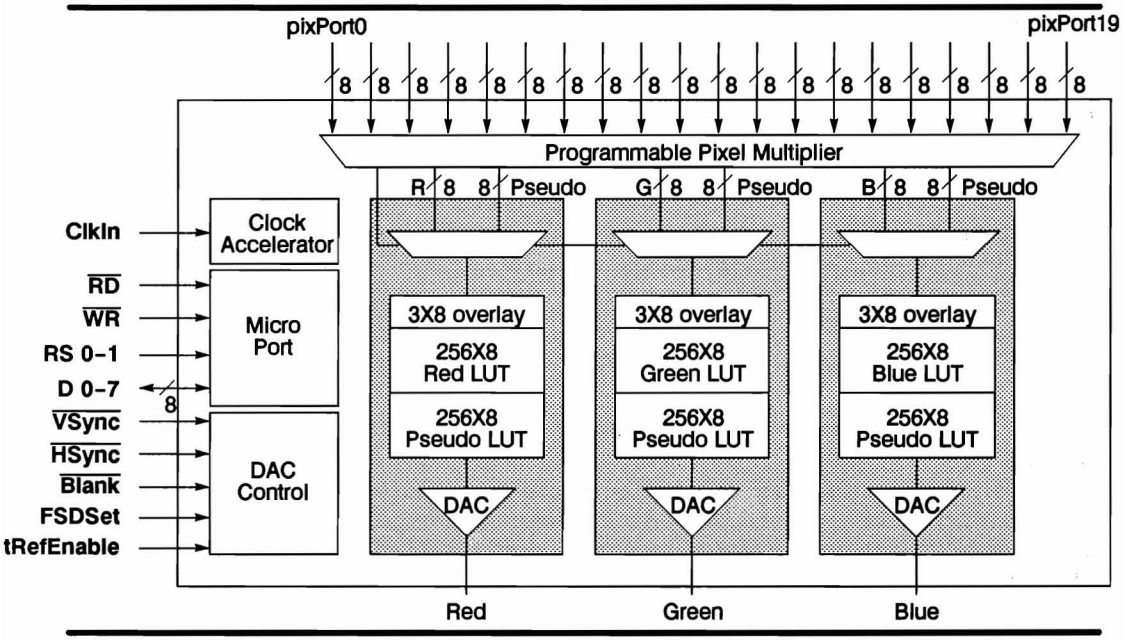
* Available 1991



IMS G180
IMS G181
Combined true-colour and pseudo-colour look-up table

inmos®

Advance information



FEATURES

- 8 bit, 16 bit or 32 bit pixels at up to 150MHz
- Pixel multiplex at 2,3,4 or 5:1 (G180)
- Pixel multiplex at 2:1 (G181)
- Matching clock acceleration using on-chip PLL
- Three 256×8 LUTs for pseudo colour image
- Three 256×8 LUTs for gamma correction of 24 bit RGB image
- Three 3×8 bit overlay tables for cursor display
- Three EIA343-A 8 bit video DACs
- Optional on-chip DAC reference circuitry
- Pixel dot-rate checksum test facility
- Hardware pixel panning facility
- Selectable zero, 1/4, 1/2 and full DAC intensity
- All input signals and clocks at TTL rates and levels
- Composite sync and blank pedestal control
- 224 pin package (IMS G180)
- 132 pin package (IMS G181)

DESCRIPTION

The IMS G180 and G181 both combine a versatile pixel multiplexer together with three independent colour channels, each comprising two 256×8 bit colour tables, a 3×8 bit overlay table and a high performance video DAC.

By programming the pixel multiplexer the parts can be configured to work with a range of pixel sizes : 8 bit pseudo colour, 16 bit RGB or 32 bit (24 bit RGB + 8 bit pseudo). Using the latter format, it is easy to mix 24 bit true-colour and 8 bit pseudo-colour images on the same screen (picture in picture).

The G181 comes in a 132 pin package and multiplexes pixels 2:1, whilst the G180 comes in a 224 pin package and can multiplex pixels by 2,3,4 or 5:1 selectable under software control. Neither the G180 or the G181 require video rate pixel data or clock signals; the only video rate signals are the DAC outputs.

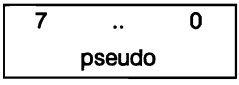
9.1 Device description

The IMS G180 and G181 are designed primarily for use in the output stages of high performance true-colour raster-scan video systems. They both contain three high-speed pipelined video channels, each containing two 256×8 bit colour look-up tables, a 3×8 bit overlay table and a video DAC (figure 9.1). All three channels are supplied with pixel data from a single programmable pixel multiplexer and are controlled from a single asynchronous 8 bit wide microprocessor interface.

9.1.1 Pixel modes

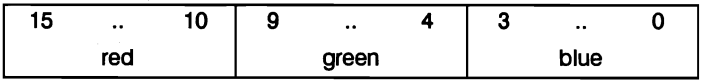
The G180 and G181 can work with pixels which are 8, 16 and 32 bits wide. In each case these pixels are multiplexed, 2:1 with the G181, and by 2, 3, 4 or 5:1 with the G180.

8 bit pixels are treated as pseudo-colour pixels and are mapped using the three 8 bit pseudo-colour tables before being displayed through the video DACs.



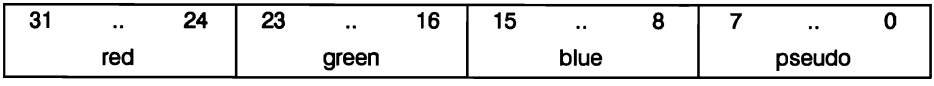
16 bit pixels are treated as true-colour pixels. 6 bits for red, 6 bits for green and 4 bits for blue. The least significant bits of each 8 bit component (red, green or blue) are set to zero and the resulting pixels are mapped using the three RGB colour tables.

The bits within a 16 bit pixel are interpreted as follows :-



32 bit pixels contain both a pseudo-colour field and a true-colour field. The pseudo-colour field contains 8 bits and is mapped with the pseudo-colour tables. The true-colour field contains 24 bits (8 bits each for red, green and blue) and is mapped using the RGB colour tables to provide gamma correction or a similar function. On each pixel cycle the part selects either the pseudo or the RGB field and translates with the appropriate colour table, before displaying the pixel using the video DACs.

A 32 bit pixel has two fields (pseudo and RGB) and is interpreted as follows :-



When operating in 32 bit pixel mode the G180 and G181 can be programmed so that the pixel select pins decide which field (RGB or pseudo) gets displayed by the video DACs. Alternatively, the decision can be based on the value of the pseudo field. In this mode if the pseudo field is 0 after masking, then the RGB field is displayed, if it is non-zero the masked pseudo field is displayed. The choice as to which method is used to switch between the two fields is made by writing to the compositing register. Both methods permit switching between RGB and pseudo streams on a pixel by pixel basis at any point in the screen, any number of times.

9.1.2 Clock acceleration

To simplify system design, both the G180 and the G181 incorporate a clock acceleration circuit. This circuit is used to multiply the **ClkIn** frequency by the same factor as the pixel data multiplexing.

This means that if for example 4:1 pixel multiplexing is selected, both the **ClkIn** and the pixel data are supplied at 1/4 of the video dot rate. This permits video operation at pixel rates of 150MHz, whilst avoiding

the need for any high speed ECL circuits outside the G180 or G181. System design is easier, cheaper and radiated emissions are kept to a minimum.

9.1.3 Overlays

The G180 and G181 both have overlay inputs. These can be used to overlay text or cursor information onto the final image. Overlays can be selectively enabled or disabled through the micro-port by writing to the overlay mask register. Overlay inputs are multiplexed by the same factor as the pixel inputs.

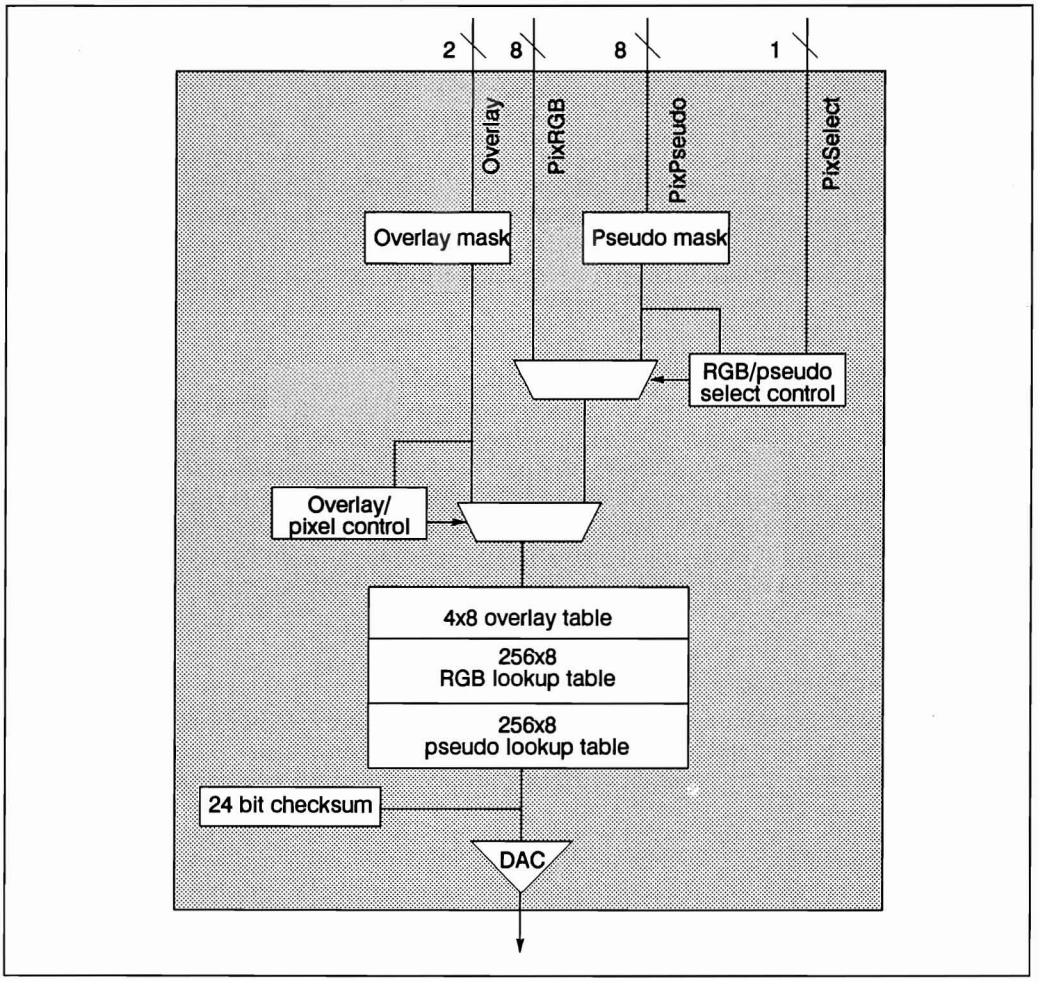


Figure 9.1 Colour Channel Architecture

9.1.4 Colour Channel Architecture

Figure 9.1 shows the architecture of each of the colour channels. The G180 and G181 each contain three such channels (i.e. one each for red, green and blue). The main pixel multiplexer takes pixel data from the pixel pins and passes this data to the inputs of the red, green and blue colour channels, under control of the pixel mode register.

Each colour channel has an RGB input, a pseudo-colour input, an overlay input and a pixSelect input. Each channel contains two 256 x 8 bit look-up tables, one for its RGB input and one for its pseudo-colour input and an overlay table containing 3 locations for the overlay input.

Pseudo pixel data is first masked with an 8 bit pseudo-colour mask. The mask register contents are bitwise ANDed with each pixel and the result passed on. By changing the contents of the pseudo-colour mask register rapid animation and flashing objects can be achieved on the screen.

The result of masking the pseudo pixel data may be compared with zero and the result of this compare is used to switch the pseudo/RGB multiplexer. If the result is zero the RGB field is selected and the RGB pixel will be mapped using the RGB colour table, if the result is non-zero then the pseudo field is selected and the pseudo pixel will be used to select a pixel value from the pseudo look-up table.

Alternatively, the RGB/pseudo multiplexer can be controlled directly by the **pixSelect** pins. The choice as to which method is used to switch between RGB and pseudo data is made by writing to the compositing register.

The final stage before the colour palette is the overlay logic. The overlay data from the pixel multiplexer is masked with the contents of the overlay mask register. The result of the masking operation is compared with zero. If the result is non-zero then the overlay multiplexer selects the overlay stream, and the overlay data will be mapped using the contents of the overlay table; if it is zero the RGB/pseudo stream is selected, and the resulting pixel will be displayed using either the pseudo or RGB colour tables. (Writing zero to the overlay mask register turns off the overlay function.)

9.1.5 Testability

All registers within the G180 and G181 can be read back through the microport. In addition, to assist in self-test and fault-finding on boards, a dot rate checksum facility is provided for each channel. This checksum resets on the rising edge of **$\overline{\text{VSync}}$** before the start of a frame and thereafter accumulates each 8 bit data value presented to the DAC inputs (except those for which **Blank** is active) into a single 24 bit checksum. This 24 bit checksum can then be read back during frame flyback before the checksum is reset and the next checksum value is computed. Thus all parts of the chip which affect the visible picture (with the exception of the DACs) are tested by this mechanism. There is a separate 24 bit checksum for each colour channel.

9.1.6 The DACS and reference circuitry

The 8 bit video DACs source current into external load resistors. They are designed to directly drive a doubly-terminated 75Ω transmission line. The DACs will drive a singly-terminated line but the edge rates, in particular the falling edge, will be slower. (Data sheet DAC parametrics are only guaranteed for double termination.)

The full-scale current of the DACs may be set by either an internal or an external reference. When using the internal reference all that is required is a single resistor, using an external reference requires a current source. The choice is determined by the **IntRefEnable** pin.

A DAC control register is provided for the selection of a variety of programmable features. These include optional **Sync** and **Blank** pedestals. In addition, the DACs can be restricted to operate in 6 bit mode, as well as being programmable to half, quarter or zero intensity.

9.1.7 Microprocessor Interface

The G180 and G181 are programmed through a simple 8 bit microprocessor programming interface. All registers are selected using two register select lines $RS_0 - RS_1$. The contents of the look-up tables and all the registers are defined by writing to the microprocessor interface. All registers are readable.

9.2 Pin function reference guide

9.2.1 Pixel interface

Pin name	I/O	Signal name	Comments
ClkIn	I	Input clock	The rising edge of this clock controls the sampling of the pixel, overlay, **HSync**, **VSync** and **Blank**. The video dot rate is 2,3,4 or 5 times the frequency of **ClkIn**, depending on the pixel mode selected.
Pix0$_{0-7}$ **Pix1$_{0-7}$** **Pix2$_{0-7}$** **Pix3$_{0-7}$** **Pix4$_{0-7}$** **Pix5$_{0-7}$** **Pix6$_{0-7}$** **Pix7$_{0-7}$** **Pix8$_{0-7}$** **Pix9$_{0-7}$** **Pix10$_{0-7}$** **Pix11$_{0-7}$** **Pix12$_{0-7}$** **Pix13$_{0-7}$** **Pix14$_{0-7}$** **Pix15$_{0-7}$** **Pix16$_{0-7}$** **Pix17$_{0-7}$** **Pix18$_{0-7}$** **Pix19$_{0-7}$**	I	Pixel data	These pins are the pixel input ports (0–19 on the G180 and 0–7 on the G181), each port is eight bits wide. New pixel data is loaded on every rising edge of **ClkIn.**
PixSelectA **PixSelectB** **PixSelectC** **PixSelectD** **PixSelectE**	I	Pixel select	When programmed to operate with 32 bit pixels, these pins determine whether the 24 bit full-colour pixel is displayed by the DACs or whether the pseudo-colour pixel is displayed. (Only **PixSelectA** and **PixSelectB** are present on the G181 which can only multiplex pixels by 2:1)
OverlayA$_{0-1}$ **OverlayB$_{0-1}$** **OverlayC$_{0-1}$** **OverlayD$_{0-1}$** **OverlayE$_{0-1}$**	I	Overlay data	The overlay data sampled on these ports may be programmed to optionally override the pixel data sampled on the pixel port and substitute an overlay colour for a pixel colour. Overlay operation is defined by the contents of the overlay mask register. (Only **OverlayA–B** on the G181.)
$\overline{\text{Blank}}$	I	Blank	A low logic level on this input will cause a colour value of zero to be applied to the inputs of the DACs and will cause an offset corresponding to 5% of the DAC full-scale output to be removed if **Blank** pedestal is enabled, regardless of the colour value of the current pixel or overlay.
$\overline{\text{HSync}}$	I	Horizontal sync	A low logic level on this input indicates the beginning of a horizontal line flyback period and will cause an offset corresponding to 35% of the DAC full-scale output to be removed if composite **Sync** is enabled in the DAC control register.
$\overline{\text{VSync}}$	I	Vertical sync	A low value on this input indicates the beginning of a vertical frame flyback period and will cause an offset corresponding to 35% of the DAC full-scale output to be removed if composite **Sync** is enabled in the DAC control register. This signal is also used to reset the three 24 bit checksum registers

9.2.2 Analogue Interface

Pin name	I/O	Signal name	Comments
Red **Green** **Blue**	O O O		These signals are the outputs of the 8 bit DACs. They deliver current into a doubly-terminated 75Ω transmission line.
IntRefEnable	I	Internal Reference Enable	This pin selects whether the internal reference is to be used or not. If it is held high then the internal reference is selected and a resistor should be wired between **FSDSet** and **VDD**. If it is held low then an external reference current of 2.094mA must be connected between **FSDSet** and **VDD**.
FSDSet	I	Full-scale deflection set	When using the internal reference the value of the resistor placed between this pin and **VDD**, in combination with an on-chip reference circuit, determines the full-scale current output of the video DACs. When using an external reference a current source must be connected between this pin and **VDD**. **Warning:** If external reference is selected but resistor is connected, the chip will be damaged beyond repair.

9.2.3 Microprocessor Interface

Pin name	I/O	Signal name	Comments
$\overline{\mathbf{WR}}$	I	Write enable	The write enable signal controls the writing of data to the part. The state of the **RS** pins is sampled on the falling edge of $\overline{\mathbf{WR}}$ and the write data on $\mathbf{D_{0-7}}$ is sampled on the rising edge of $\overline{\mathbf{WR}}$
$\overline{\mathbf{RD}}$	I	Read enable	The read enable signal controls read operations on the part. The state of the **RS** pins is sampled on the falling edge of $\overline{\mathbf{RD}}$ and read data ceases to be valid on $\mathbf{D_{0-7}}$ after the rising edge of $\overline{\mathbf{RD}}$.
$\mathbf{RS_0}$-$\mathbf{RS_1}$	I	Register select	The values on these inputs are sampled on the falling edge of read or write enable. They specify which of the internal registers is to be accessed.
$\mathbf{D_0}$-$\mathbf{D_7}$	I/O	Program data	Data is transferred between the 8 bit wide program data bus and the internal registers under control of the read and write enable signals.

9.2.4 Power supply

Pin name	Signal name	Comments
VDD	Power supply	Digital power is supplied from the **VDD** pins. All **VDD** pins must be connected to the **VDD** power plane.
AVDD	Analogue VDD	The DACs and internal reference are supplied from the **AVDD** pin.
GND	Digital ground	All **GND** pins should be connected to the **GND** plane.
AGND	Analogue GND	The analogue **GND** sinks the current from the DACs and reference circuitry.

9.3 Internal registers

All the registers within the G180 and the G181 are addressed by means of two address registers:- a set register and an index register. The set register specifies which data set is to be accessed and the index register specifies which location within the data set is to be accessed. Together the set register and the index register form a single 16 bit address which is used to access all registers.

The index register is auto-incrementing so that after the first read or write to a location within any given register set, the index register need not be re-written; successive locations in the register set may be written to or read from by repeatedly accessing the data register.

Where a register set only contains a single location the contents of the index register are ignored.

When the register set being addressed is one of the colour or overlay tables, the least-significant bit of the set register is used as a flag to indicate whether a read or a write to the register set is to be performed. This is necessary because accesses to the colour palette RAM and overlay palette RAM are internally pipelined. The read or write command must be passed down the pipeline.

Registers which are 24 bits wide are accessed one byte at a time in the order red, green and then blue. A internal counter controls this cycle and is reset to red each time a write is made to index register or the set register.

Unused bits in registers which are less than 8 bits wide are reserved and should be written with a data value of 0. When read back these reserved bits will return the data value 0 regardless of the data value written in.

The set register, the index register and all the data registers together are mapped into just three locations decoded from the state of the register select lines $\mathbf{RS_0}$-$\mathbf{RS_1}$ as follows :-

RS_1	RS_0	Register	Size
0	0	Set register	8
0	1	Index register	8
1	0	Data register	8
1	1	Reserved	-

Table 9.1 The G180 register mapping

Reading and writing to registers within the G180 is a three step operation, accessing these three registers in turn :-

1 Write to set register (also specifies read or write if accessing one of the pipelined LUTs)

2 Write to the index register

3 Read or write data from data register

For register sets with only one location step 2 may be omitted.

Set reg	Index register	Register set name	Read/Write	Size (of)
0	0..255	RGB LUT for write	W	24
1	0..255	RGB LUT for read	R	24
2	0..255	Pseudo LUT for write	W	24
3	0..255	Pseudo LUT for read	R	24
4-31	–	Reserved	–	–
32	0..3	Overlay LUT for write	W	24
33	0..3	Overlay LUT for read	R	24
34-63	–	Reserved	–	–
64	X	Pseudo mask register	R/W	8
65-66	X	Reserved	–	–
67	X	Overlay mask register	R/W	2(8)
68-69	X	Reserved	–	–
70	X	DAC control register	R/W	5(8)
71-72	X	Reserved	–	–
73	X	Pixel mode register	R/W	7(8)
74	X	Panning register	R/W	4(8)
75	X	Compositing control	R/W	2(8)
76-127	–	Reserved	–	–
128	X	Test checksum (lower byte)	R	24
129	X	Test checksum (middle byte)	R	24
130	X	Test checksum (upper byte)	R	24
131-255	–	Reserved	–	–

X = index register ignored

Table 9.2 The register set

9.3.1 Accessing the LUT and overlay tables

To write a set of LUT or overlay colour values the write address of the appropriate table is first written into the set register (0 for the RGB LUT, 2 for the pseudo-colour LUT or 32 for the overlay LUT). This must be followed by writing the first location to be accessed to the index register.

Red, green and blue values are then written in that order to the data register. After each group of three writes the index register will auto increment so that if a further three bytes are written to the data register the next location in each of the three colour tables will be updated. This makes updating a block of locations in the colour tables simple, since only the start address for a entire block of locations in the three colour tables need be written at the start of a sequence. (There is no facility for independently changing individual R,G or B colour components.)

Reading works in a similar way to writing. The read address of the look-up table to be accessed is written into the set register, followed by writing the address of the first location to be read to the index register. Successive reads of the data register will then return red, green and blue data in that order. Again the index register will auto-increment after three byte reads, so that if a further three bytes of data are read from the data register, the colour value data from the next location in each of the look-up tables will be returned.

9.3.2 The pseudo-colour mask and overlay mask registers

In each colour channel there is a pseudo-colour mask register which masks each bit of the pseudo-colour pixel address feeding each of the three pseudo-colour look-up tables. The contents of the mask is bit-wise ANDed with the 8 bit pixel address feeding each of the three pseudo-colour LUTs so that changing the contents of the mask register changes the address passed onto to each colour table. By changing the contents of the pseudo-colour mask register, rapid colour changes on the screen may be achieved. Also, by masking with zero the pseudo-stream may be disabled.

The overlay mask register enables or disables overlay operation. A one in a bit position in this register enables the respective overlay plane on each overlay port. If enabled, overlays operate on all pixels whether they are 8,16 or 32 bits wide.

Overlay mask register	Overlay inputs	Pixel data used
00	XX	Pixel data
01 01	X0 X1	Pixel data Overlay colour 1
10 10	0X 1X	Pixel data Overlay colour 2
11 11 11 11	00 01 10 11	Pixel data Overlay colour 1 Overlay colour 2 Overlay colour 3

Table 9.3 Overlay Operation

9.3.3 The pixel mode register

The pixel mode register controls how the part interprets the data presented at the pixel port. Pixel sizes of 8, 16 and 32 bits are supported on both the G180 and the G181.

The register is sub-divided into 3 fields (see table 9.4).

The first field, (bits 0-1) selects the pixel size, 8, 16 or 32 bits and is a binary coding of the number of bytes per pixel.

The second field (bits 2-4) selects the number of pixels which are loaded on every clock edge, ie the pixel acceleration factor. In addition to setting the pixel acceleration factor this field also sets the clock acceleration factor. For example if 4:1 acceleration is selected on the G180, 4 pixels are latched on every **ClkIn** edge and the **ClkIn** is multiplied internally by a factor of 4 to generate the video rate clock.

The third field (bits 5-6) determines the source of the pseudo-colour data fed to the colour-channels. The pixel multiplexor provides a 32 bit output to the three colour channels. These register bits select which of the 4 constituent bytes are driven to the channels as the pseudo-pixel data.

Operation			Comment
Bit 6, 5 Page mode	**Bit 4, 3, 2 Accel**	**Bit 1, 0 Pixel size**	
		00 01 10 11	32 bit pixel 8 bit pixel 16 bit pixel Reserved
	nnn		binary coded accel factor
00 01 10 11			pseudo→pseudo blue→pseudo green→pseudo red→pseudo

Table 9.4 The pixel mode register

8 bit pixels are treated as pseudo-colour pixels and are translated into RGB data using the contents of the pseudo-colour tables.

16 bit pixels are treated as true-colour pixels (6 bits red, 6 bits green and 4 bits blue). The lower bits of each colour component are set to 0, before being translated into RGB data by the RGB colour tables.

32 bit pixels have both a pseudo-colour and a true-colour field and the part can switch, on a pixel by pixel basis, between the two fields. This can be done either by controlling the **pixSelect** pins or by using the value of the pseudo field. If selected the pseudo-colour field will be displayed using the pseudo-colour table, otherwise the true-colour field will be displayed using the RGB colour tables.

The pixel port on the G180 (G181) can be viewed as 20 (8) 8 bit ports. Tables 9.5 and 9.6 show how the G180 (G181) can interpret pixel data presented at these ports. The letters in parentheses indicate ports that are used only if the multiplexing rate is high enough and which are therefore not available on the G181.

bits/pixel	Port number (each port is 8 bits wide)																			
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
32 bit	A				B				(C)				(D)				(E)			
16 bit	A		B		(C)		(D)		(E)		unused									
8 bit	A	B	(C)	(D)	(E)	unused														

Table 9.5 Scanning of pixel inputs for different multiplexing rates

bits/pixel	Bit position in word																			
	0			3	4			7	8	9	10			15	16			23	24	31
32 bpp:	P[0]....P[7]								B[0]....B[7]						G[0]....G[7]				R[0]....R[7]	
16 bpp:	B[4]..B[7]				G[2]..G[7]						R[2]..R[7]				unused					
8 bpp:	P[0]....P[7]								unused											

Note: P = Pseudo, R = Red, G = Green, B = Blue pixel data

Table 9.6 Assignment of bits in different pixel modes

9.3.4 The DAC control register

The DAC control register controls the operating features of the video DACs.

The features supported are:

- an optional **Blank** pedestal, an optional **Sync** pedestal
- a reduction in the DAC resolution from 8 to 6 bits
- reduced contrast DAC display modes, whereby the DACs may be programmed to output full intensity, half intensity or quarter intensity images as well as forcing blanked output.

Bits 4, 3	Bit 2	Bit 1	Bit 0	Operation
DAC contrast	8/6	Black lev	Sync	
			0	**Sync** pedestal on
			1	**Sync** pedestal off
		0		**Blank** pedestal on
		1		**Blank** pedestal off
	0			8 bit DAC operation
	1			6 bit DAC operation
00				Full intensity operation
01				Half intensity operation (stand-by)
10				Quarter intensity operation (stand-by)
11				DACS blanked

Table 9.7 The DAC control register

9.3.5 Panning register

This register allows the pixel pipeline of the **Sync**, **Blank** and **Overlay** inputs to be delayed by up to 7 pixels relative to the pixel data read in on the pixel ports. The user has the choice as to whether to delay the overlays or not.

By changing the contents of this register a smooth hardware horizontal pan can be easily achieved, provided the colour monitor is taking its **Sync** pulses from the DAC outputs and is not using a separate **Sync** line.

A value of 0 in the delay field sets the internal pipeline delay of the composite **Sync, Blank** and, optionally, the **Overlay** signals to be equal to the pipeline delay of the pixel information through the look-up tables. A value of one in this field delays these signals by one pixel relative to the pixel data, a value of two delays them by 2 pixels and so on.

Bit 3 selects whether the overlays pan or not. If it is set high then the overlays will pan with the picture, if it is set low the overlays will not pan with the picture i.e. are delayed with the **Syncs** and **Blanks**.

Bit 3	Bits 2, 1, 0	Blank delay relative to pixel data in units of pixels	Overlays
0			Pan with picture
1			Do not pan with picture
	000	0	
	001	1	
	..	..	
	110	6	
	111	7	

Table 9.8 The panning register

9.4 Compositing control register

The G180 provides several means for combining the pseudo and true-colour data streams. There are four options (numbered 0..3) controlled by bits 1 and 0 in the compositing control register.

Bits 1, 0	Operation
00	If the **pixSelect** pin is low, the true-colour image is selected irrespectively. If the **pixSelect** pin is high then the pseudo-colour image is selected, unless the pseudo-colour pixel is zero, in which case the true-colour image is selected.
01	If the pseudo data is zero the true-colour image is selected, otherwise the pseudo-colour image is selected.
10	If the **pixSelect** pin is high the pseudo image is selected, otherwise the true-colour image is displayed.
11	The pseudo-colour image is always selected.

9.5 Test checksum register

The G180 and G181 both have a pixel rate checksum test facility.

Each channel (red, green and blue) has a 24 bit checksum register which is reset on the rising edge of **VSync** and accumulates each data value thereafter into a 24 bit checksum register. (Pixel data supplied whilst **Blank** is asserted has no effect on the contents of the checksum register i.e. only visible pixels affect the value of the checksum.) The checksum works on one frame's worth of pixel data at a time.

At the end of a frame, during the flyback period, the microprocessor is able to read the three final checksum values for each channel. Like the 24 bit colour values the checksum values are read in the order red, green and blue. The data value must be read before the rising edge of the next **VSync** after which point the checksum will be reset ready for the next frame of data.

The checksum register is a linear feedback shift register. Data bytes are accumulated in pairs, before being exclusive OR'ed into the 24 bit checksum register.

The algorithm for the checksum can be expressed in C as follows :-

```
#define bitsincrc 24       /* number of bits in checksum */
#define tapmask 0x610000L /* generator polynomial for 24 bit checksum */
#define bitsindata 16      /* number of bits in data word */

long checksum, clipcrc, topbit;
int  dataword, clipdata, pixelnumber;

  topbit    = 1 << (bitsincrc-1);
  clipcrc   = (1<<bitsincrc) - 1;          /* for clipping crc to length */
  clipdata  = (1<<bitsindata)-1;           /* for clipping data to length */
  checksum  = clipcrc;                     /* initialise checksum */

                                           /* maxPixel = number of */
                                             visible pixels       */
  for (pixelnumber=0; pixelnumber < maxpixel;
                      pixelnumber = pixelnumber+2 )
    {
      dataword = getpixel(pixelnumber) | (getpixel(pixelnumber + 1) <<8);
      dataword = dataword & clipdata;
      checksum = checksum ^ dataword;

      if ((checksum & topbit) == 0)        /* if top bit clear */
        {
          checksum = checksum ^ tapmask; /* feedback to taps */
          checksum = checksum << 1 ;     /* shift left */
          checksum = checksum | 1;       /* set least significant bit */
        }
      else
        checksum = checksum << 1;       /* shift left and clear LSB */

      checksum = checksum & clipcrc;    /* clip to length */
    }
```

Designing with INMOS colour look–up tables

10.1 Using INMOS CLUTs

10.1.1 General board layout

To get the best performance from an analogue component such as a Colour Look-Up Table (CLUT) in the noisy environment of a graphics board, it is important to pay some attention to the board layout, in particular components surrounding the CLUT.

First and foremost, it is essential to use a four-layer board with VDD and GND planes separating the wiring planes. Large continuous power planes on adjacent layers ensure a good low-inductance power supply to all parts of the board with distributed capacitve coupling between the power planes across the board. This minimises undershoot on the digital signals routed round the board. In addition VDD and GND planes minimise the power radiated from signal tracks and thereby reduce the energy coupled into other sensitive conductors on the board, such as the the analogue outputs of the CLUT.

VDD and GND planes should be periodically coupled with high frequency (i.e. low series inductance) capacitors. Chip-capacitors in the range 100 - 500nF are the best for this; being leadless chip-capacitors have very low series inductance. If chip-capacitors are not available then ceramic capacitors with the absolute minimum lead length are the next best.

Other general hints include positioning the CLUT as close to the edge of the board as possible, keeping the current reference circuit close to the CLUT, not laying analogue output tracks over digital tracks and keeping the pixel input buffer as close to the CLUT as possible. A number of these points are explained further in later sections of this note.

10.1.2 The power supply to the CLUT

In order to minimise the noise on the the DAC outputs of a CLUT it is important to minimise the noise on the power supply to the CLUT since the DAC output current is referenced to the positive power supply — VDD. Ideally the noise should be no more than 200 - 300mV and preferably less.

A more important factor than the absolute magnitude of the noise is the ability of the current source to track the power supply noise on the IREF pin. This is because the instantaneous current out of the DAC is always set by the **voltage difference** between the VDD pin and the IREF pin. In practice then, it is quite possible to achieve a very clean analogue output, even with large noise fluctuations on the power supply, so long as the current source has a sufficiently fast response time to keep the voltage on IREF tracking these fluctuations, and so keep the voltage difference between VDD and the IREF pin constant. Clearly though, whilst a high speed tracking current reference will minimise power supply noise on the DAC outputs it is preferable to avoid the VDD noise in the first place.

In many systems which have a clean global power supply, achieving a noise free supply to the CLUT will require no more than a good high frequency coupling of the supplies right next to the device. Excessive PCB design work to provide separate digital and analogue VDD and GND planes would be uneccessary and unjustified. Again a high frequency 100nF capacitor in parallel with a larger 47μF capacitor (preferably tantalum) should be used.

10.1.3 Decoupling the CLUT supply

In situations where the main board supply is too noisy to achieve acceptable results by local capacitive coupling next to the CLUT, then it is possible to provide a locally decoupled supply for just the CLUT using a simple L-C circuit, figure 10.1.

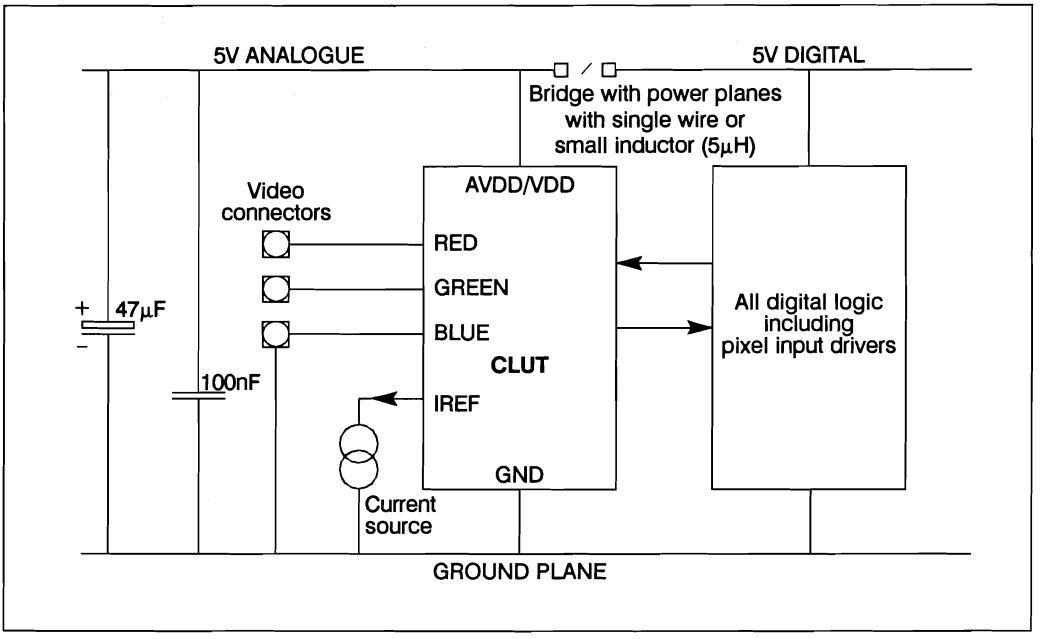


Figure 10.1 Locally decoupling the CLUT supply with an L-C circuit.

This separate CLUT supply should be maintained on a single island power plane. It should overlap just the analogue parts of the CLUT package: RED, GREEN, BLUE, the IREF circuitry and the VDD pin. This will ensure minimum pick-up from the other digital circuitry and wiring.

A practical value for the inductor is in the region 1-5μH. Small PCB and surface mount inductors in this range are readily available with current ratings sufficient to supply the 150-200mA supply current required by INMOS CLUTs. The capacitor should be 47μF, but again a 100nF low inductance capacitor should be used in parallel.

In the case of a part with a separate analogue power pin AVDD as well as a digital VDD pin, (such as the G176 in a surface mount package), both pins should be taken to the separate quiet power plane.

10.1.4 The pixel inputs

Edge rates on the pixel inputs should be kept as slow as possible, consistent with the timing requirements on the pixel port; this will ensure the minimum of clock noise pick up on the analogue outputs. On many graphics boards the major source of noise on the DAC outputs will be noise coupled through from the pixel lines and the pixel clock itself.

Since both the pixel clock and the pixel data lines run at the full video rate it is preferable to keep these lines short (less than 3 inches.) Ideally the buffers which drive these lines should be positioned close to the CLUT to reduce the reflection time and thereby minimise undershoot and ringing.

If board layout constraints make long tracks unavoidable, or if very fast drivers have to be used to meet the required timing specification, then series termination at the buffer output is recommended to minimise undershoot. Typically a resistor around 100Ω placed in series with the output will improve the matching between the buffer output impedance and the impedance of the PCB track. To achieve perfect matching the characteristic impedence of the lines should be determined empirically, and a series resistor of the same value used. Parallel termination may also be used with the same value of resistors, but this has the disadvantage of consuming D.C. power and may load the pixel buffer outputs beyond their drive capability.

10.1.5 The DAC outputs

The analogue outputs of all INMOS CLUTs come from switched current sources drawing current from the positive supply. The output may drive either a singly or doubly terminated 75Ω load according to the device used. Double termination is the preferred method since, with both ends of the transmission line being cor-

rectly matched, outputs are less likely to suffer from reflections returning from any mismatch along the length of the transmission line between DAC outputs and the monitor. With long monitor cables, mismatches will lead to reflected components returning to the monitor after the first pixel edge and degrading the quality of the image. Another advantage is that it gives sharper DAC edge rates (due to the lower RC time-constant). Double termination is illustrated in figure 14.2.

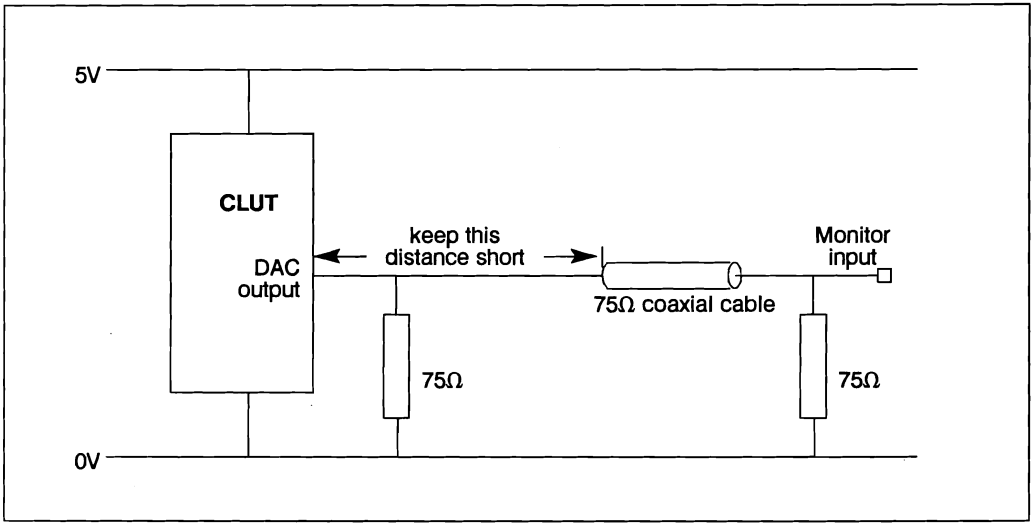


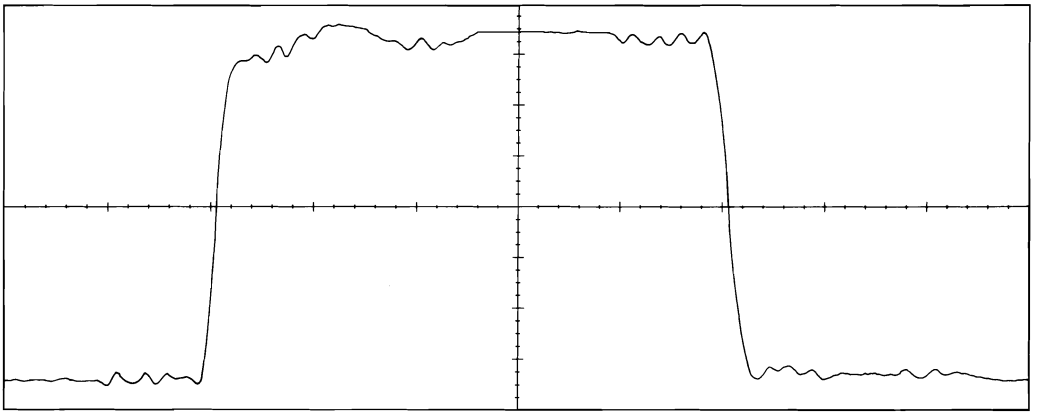
Figure 10.2 Double termination of DAC output.

The resistors used should be high-accuracy metal or carbon film types. Often the monitor will contain its own terminating impedance which can be switched in, so only the resistors at the CLUT outputs will be of concern to the board designer.

DAC output traces should also be treated as transmission lines and mismatches anywhere in the path leading from the analogue output pins on the CLUT package to the monitor RGB inputs will degrade the final image quality. In most systems the simplest way of ensuring minimal reflections is to keep the distance from the DAC output pins on the CLUT to the video connectors on the PCB down to the absolute minimum – less than 2–3 inches is ideal. If this is done then any reflected components coming back from the video connectors will occur well within the risetime of the pixel edge and little or no loss of image quality will result. The ideal position for a CLUT on a graphics board is at the edge of the board with the video connectors feeding out from the edge. This will also serve to minimise noise pickup on the analogue output traces.

As with any other CMOS device, members of the IMS g17X family can be damaged if exposed to high electrostatic voltages. Once assembled into a system they are much less exposed, though the analogue outputs are usually still made available externally through the connector to the monitor. If these are likely to be subject to stray electrostatic voltages, particularly if cables to the monitor are frequently connected and disconnected, then some kind of protection device should be considered on these outputs. Any fast silicon diode is usually sufficient, e.g. 1N4148's have been found to be a cheap and effective solution.

Figure 14.3 shows a typical DAC output waveform generated by a G176 device. The DAC is shown switching through its full range 0–63. The voltage amplitude is approximately 650mV and the edge rates are between 2 and 3ns.



Ch.1 = 100.0mV/div

Timebase = 10ns/div

Figure 10.3 DAC output waveform showing reflection and clock noise.

A minor reflection after the rising and falling edges is clearly visible, as is a small component of clock and pixel noise.

10.1.6 Current sources

All INMOS CLUTs require a simple current source to provide a reference current for the DAC outputs. This current is drawn from the positive rail. The principal considerations when designing a current source for a CLUT are accuracy, thermal stability and a fast AC response. A number of different circuits are possible, and there is the usual tradeoff between cost and performance to consider. Some recommended current sources are described below which cover the range of cost and performance.

1 The simplest and cheapest reference circuit can be made with just a transistor and 3 resistors, as shown in Figure 14.4. This is appropriate in very cost sensitive designs where accuracy and stability are not critical.

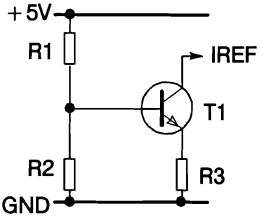


Figure 10.4

In this circuit IREF is set by the potential divider of R_1 and R_2. There is no compensation for variations in the base-emitter voltage of T_1. Assuming a high gain transistor the equation for this circuit is:

$$V_{CC} \times \frac{R_2}{R_1 + R_2} - 0.6 = IREF \times R_3$$

2 Figure 14.5 shows a current source based on the TL431 voltage reference. Note that it is only appropriate when there is a negative supply rail VNEG available, such as used for disk drives or communication ports.

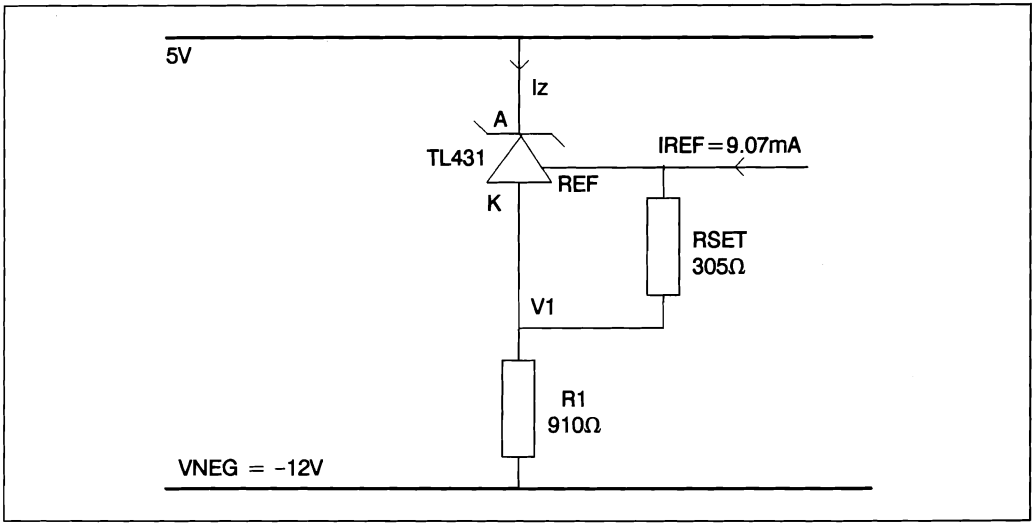


Figure 10.5 Current reference based on the TL431 voltage reference.

This circuit requires just two resistors together with the 431. The 431 works by maintaining the voltage across RSET at 2.75V. Since the current into the reference pin of the 431 is negligible (it never exceeds 10μA), the value of RSET determines the IREF drawn from the CLUT:

$$IREF = \frac{2.75V}{RSET}$$

IREF is summed with the regulator current Iz flowing through the 431 and passes to the negative rail through R1. The value of R1 should be chosen so that Iz comfortably exceeds 2mA (say 5mA); this ensures that the 431 is biased correctly. For IREF currents in the range 4 to 10mA, the voltage on the IREF pin will typically be around 3V. Subtracting the 2.75V developed across RSET means that the voltage V1 will be around 0.25V. Knowing the voltage of the negative supply, R1 can be chosen to set the current Iz to approximately 5mA:

$$R1 = \frac{0.25V - VNEG}{IREF + Iz}$$

The component values shown in the figure are again chosen to set IREF at 9.07mA and Iz at approximately 4.6mA. Clearly, VNEG need not necessarily be -12V, a -5V rail could just as well be used provided R1 is chosen to keep Iz well above 2mA.

3 Figure 14.6 shows a current reference based on the LM-334 device.

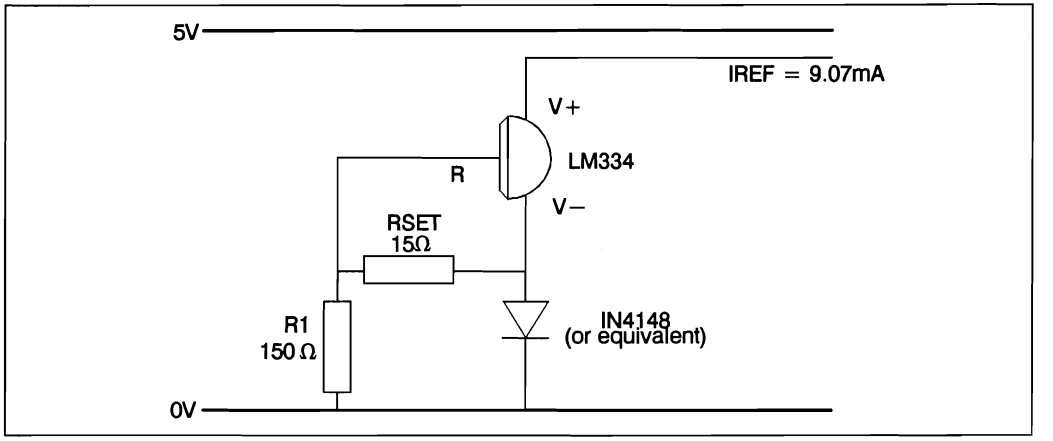


Figure 10.6 Current reference based on the LM334.

The device is used in its zero temperature coefficient mode. This device can supply reference currents up to 10mA. The value of RSET sets the basic current drawn, and must be a precision resistor, with the second resistor R1 and the silicon diode (IN4148) providing temperature compensation. From the LM-334 datasheet the relevant calculations are:

$$RSET = \frac{66.7mV \times 2}{IREF}$$

$$R_1 = 10 \times RSET$$

The component values shown in the above figure are chosen to set the reference current at 9.07mA. This is the normal reference current for INMOS CLUTs used with doubly terminated DAC outputs to give a peak white signal of 0.7V.

10.1.7 Current versus voltage reference comparison

The IMS G17X family of Colour Look-Up Tables (CLUTs) and IMS G3XX Colour Video Controllers (CVCs) all require a stable reference current for the DAC outputs. This is provided by an external current reference circuit.

The major considerations to be taken into account when choosing or designing this circuit are :-

1 The accuracy of the reference current

2 The stability of the current over the operating temperature range

3 A fast AC response to track any VDD noise on the board

4 Board area

5 Cost

INMOS provides a number of recommended circuits in the INMOS graphics data-book and datasheets, ranging from simple, single transistor circuits, which are very cheap and give adequate performance, to a dedicated temperature-stabilised three-terminal IC which gives excellent performance for a slightly greater cost.

Other manufacturers of IMS G171 compatible CLUTs offer parts which allow for the use of either a current reference **or** a voltage reference. They clearly believe that for **their** parts, the voltage reference is a better choice. They believe it provides better noise immunity and requires less external components.

This application note discusses both the INMOS recommended current reference circuit and compares it with a typical recommended voltage reference circuit.

The INMOS recommended circuit

The INMOS recommended circuit uses the LM334 programmable current source. This is a three terminal precision current source with temperature compensation. To build a current reference using this circuit requires just three extra components, two resistors and a silicon diode.

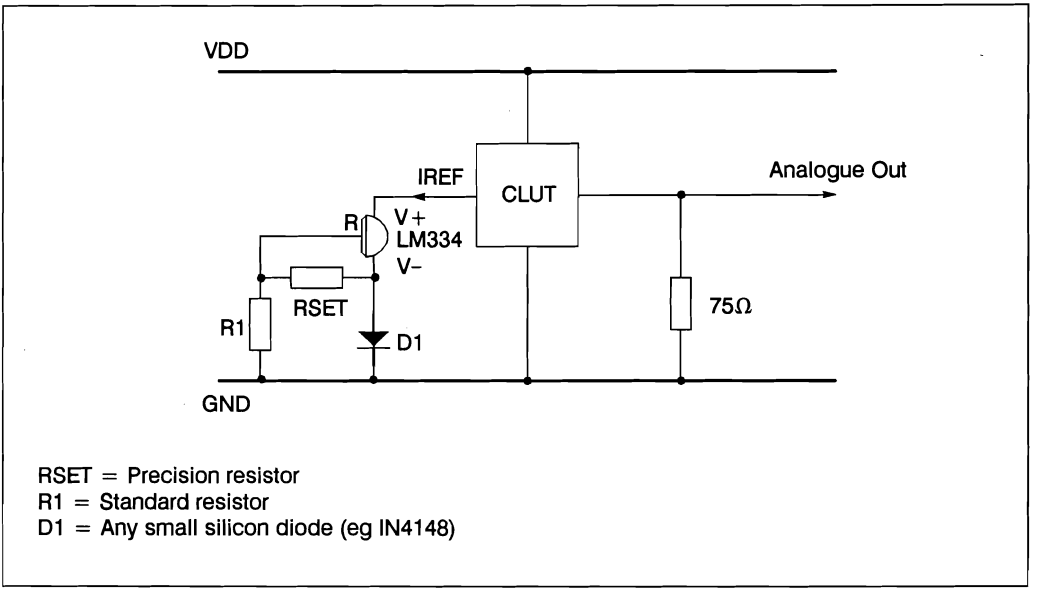


Figure 10.7 INMOS recommended circuit

The resistor RSET determines the basic reference current through the LM334 so it should be a precision resistor. The resistor R1 in combination with the diode provide temperature compensation. The value of R1 should be approximately 10×RSET, but this value is less critical and so may be a standard tolerance resistor.

The reference current is given by the equation :

$$-\text{IREF} = 66.7\text{mV} \times 2 / \text{RSET}$$

The tolerance of the reference current is given by the tolerance on the resistor (typically 1%) in combination with the tolerance on the LM334 which is 4% giving a worst case maximum error in IREF of 5%. This must be added to the tolerance of the CLUT itself which is 5% to give a total tolerance of 10%.

The temperature drift of the circuit in the 'temperature compensated' mode shown above is insignificant when compared to this overall tolerance, (typically less than 1% across a 0 – 100 °C temperature range).

The LM334 also has a high slew rate (around 5mV/ns at 10mA IREF), which means that it is able to track any high frequency noise on the board VDD supply and thus does not require external decoupling capacitors.

The cost of the LM334 is low. At the time of writing STC quote $1.69 for the National LM334Z in quantities of 100.

In summary, the LM334 has all the right attributes for an external reference, high precision, stability and slew rate, requires minimal additional components and is available at low cost.

A typical recommended voltage refererence circuit.

Some 'VGA compatible' devices offered by other vendors can use either a current reference or a voltage reference so that if a designer designs his board to use a current reference he will be able to use either the INMOS part or any of the other vendors parts.

A typical recommended circuit for the voltage reference is shown in figure 10.8.

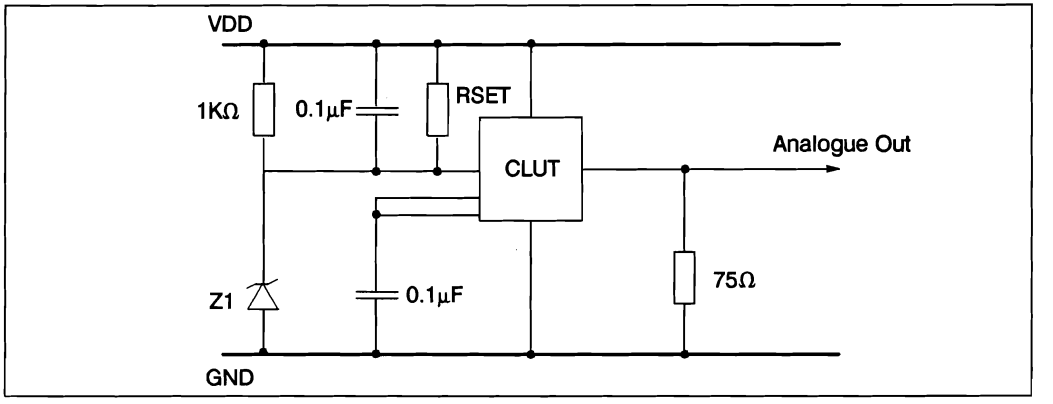


Figure 10.8 Voltage reference circuit

The circuit uses a National Semiconductor LM385BZ which is a precision 1.2 volt reference. The basic accuracy of this part is 1%, with a temperature tolerance approximately equal to the LM334 circuit.

This 1% tolerance compares well against the 4% for the LM334. However taking into account the other tolerances which all add up to the final DAC output accuracy, namely the 1% resistor tolerance and the 5% tolerance on the CLUT, the total tolerance is 7%. So in terms of **total** tolerance the difference is 7% for the voltage reference circuit against 10% for the current reference circuit. Further inaccuracies may be incurred through the use of a voltage reference circuit. This is because internal CMOS conversion is usually required by devices in the voltage reference mode.

The noise rejection of the system is determined by a combination of the external capacitors in conjunction with an operational amplifier internal to the colour palette. High frequency decoupling will depend on the performance of the on-chip op-amp and the low frequency noise rejection is largely provided by the additional external capacitors.

The main drawback of this circuit is cost. The required external noise decoupling costs two extra capacitors which are not needed on the current reference circuit. The LM385, whilst being more accurate is a much more expensive device, (the device is actually trimmed on chip, making it inherently more expensive) and the comparable quote for this device is $3.31 for the same 100 off quantities.

In summary the INMOS circuit :-

1 Requires two less components (and so uses less board area)

2 Has similar temperature stability

3 Is inherently noise rejecting

4 Provides slightly less overall DAC FSD accuracy

5 Is significantly cheaper ($1.60 less)

10.1.8 Radiated power from graphics systems

In order to comply with FCC regulations concerning computing devices, all computing systems, including their graphics components, must not emit Radio Frequency Interference beyond set limits. The following guidelines are intended to help designers minimise the RFI emitted from the video components of a graphics system, including the CLUT circuitry.

All conductors carrying time varying currents radiate electromagnetic radiation. This radiation in turn may induce currents in other conductors nearby. Radiated power from a conductor increases when it is physically large and is separated by a large distance from any ground plane. That is to say, good radiating ariels are large open systems. In a typical graphics board, the major radiating ariels are the tracks and wires surrounding the video components which carry the high frequency video signals.

To minimise the radiated power from a board a number of basic rules can be applied:

1 Keep tracks leading to and from the CLUT short, particularly the pixel address, pixel clock and DAC outputs.

2 Always use at least a four-layer board with VDD and GND planes.

3 Avoid flying leads carrying high frequency signals which are not screened.

4 Place load resistors as close as possible to the analogue outputs.

Major current transients occur when CLUT DACs are switched on and off, since this current is drawn from VDD it is important to ensure that VDD to GND coupling close to the CLUT is efficient both at low and high frequencies.

Radiated power increases with the frequency of the radiating signal (to the fourth power). It is therefore desirable to have as few signals as possible with very fast edge rates since these will have high frequency components. For example, do not use FTTL where LS will meet the timing requirements; as well as giving greater undershoot on PCB traces, the fast edges produced by the faster logic will radiate more power.

The DAC outputs themselves will in many systems be a significant radiating source. Here again any high frequency noise transients should be kept to a minimum. These may be coupled through from the pixel lines or VDD noise. Ferrite beads may be used on the analog outputs to remove these high frequency transients, though some experimentation will be required to achieve the maximum suppresion consistent with an acceptably fast risetime on the DAC output.

It should be noted that any risetime much faster than the bandwidth of the monitor it is feeding serves little purpose other than to generate more RFI and will not improve the sharpness of the displayed image.

Although not a significant contributor the bond wires of a package can behave like ariels for radiated power. In very critical high-speed applications it may be preferable to use a device in a PLCC package (IMS G176 or IMS G178) since the bond wires in such a package are shorter than in the 28-pin DIL package and overall RFI emissions may be reduced.

In summary, to minimise RFI emissions, keep all tracks carrying video and near-video rate signals as short as possible, keep edge rates as slow as possible and ensure good power supply coupling around all the video circuitry.

10.1.9 Minimising the power dissipation of a CLUT

In some cases, portable battery equipment in particular, it may be necessary to minimise the power dissipated by a CLUT by putting it into a power-down mode. An example would be a lap-top or a notebook computer which ordinarily used an LCD display but had the option to generate colour VGA displays on a standard colour monitor using a CLUT.

There are several measures which can be taken to drastically reduce the power consumption of all INMOS CLUTs. However, the IMS G176L is a specific power-down version of the IMS G176. It is guaranteed to have a standby power supply current of less than 10mA and is strongly recommended for all power down applications. The conditions to meet the standby mode are laid out in the IMS G176L datasheet, but the following explanation may be useful for 'power down' board designs containing any INMOS CLUT.

A substantial power saving can be achieved by reducing the DAC current to zero. The simplest method of doing this is to reduce the reference current, IREF, to zero. This will switch off the DACs completely, pulling the maximum d.c. current down below 100mA.

Stopping the pixel clock supplied to the CLUT will reduce the digital current drawn by the part to something less than 10mA; the remaining current is drawn by DC paths inside the device. One of these DC paths is in the input stage of each pixel input, and by taking the pixel inputs low this too can be turned off

In summary, by switching off the IREF current, stopping the pixel clock and holding the pixel inputs low, the DC current of any INMOS CLUT can be reduced to something around 10mA (guaranteed to less than 10mA with the IMS G176L), thus reducing the overall power consumption to 25–50mW.

10.2 Circuit techniques using the IMS G17X family

10.2.1 Adding composite sync to the G171/6

The major functional difference between the IMS G170 and the G171/6 devices is that the former provided the facility for adding composite sync, whereas the latter two devices offer the alternative facility of reading back the colour table contents. It quite possible however to add the composite sync function externally to the G171 or G176 and have both features. The component count to do this is small and it requires only minimal redesign around the CLUT socket.

The circuit shown below is used to superimpose a simple step waveform onto the DAC outputs of the G171/6. When this offset is momentarily removed a sync pulse is transmitted. The circuit basically has three sections:

1 A SYNC Shifter. All IMS g17X parts achieve high pixel rates by pipelining the memory accesses over a number of clock cycles. Thus there is a delay between the input of pixel data to the look-up table and the output of the appropriate analogue value. To ensure that the SYNC signal remains aligned to the picture it must be delayed by a similar number of clock cycles by using a shift register. For the IMS G171/6 the SYNC signal must be delayed by 3 clock cycles.

2 A Current Reference. Since the IMS G171/6 DACs are current sources a SYNC type waveform can be added simply by providing an additional sync reference current to the DAC output.

3 A Current Dump. This part of the circuit ensures that the current, and thus the voltage, appearing at the video outputs drops to zero when the delayed SYNC signal is applied. When the current dump is turned off the video signal generated is the normal output of the DACs plus the offset provided by the additional sync reference current. When the current dump turns on it steals all the output current, since it provides a much lower impedance path to GND, so no voltage will appear on the video outputs.

Stopping the pixel clock supplied to the CLUT will reduce the digital current drawn by the part to something less than 10mA; this remaining current is drawn by DC paths inside the g17X. One of these DC paths is in the input stage of each pixel input, and by taking the pixel inputs low this path too can be turned off.

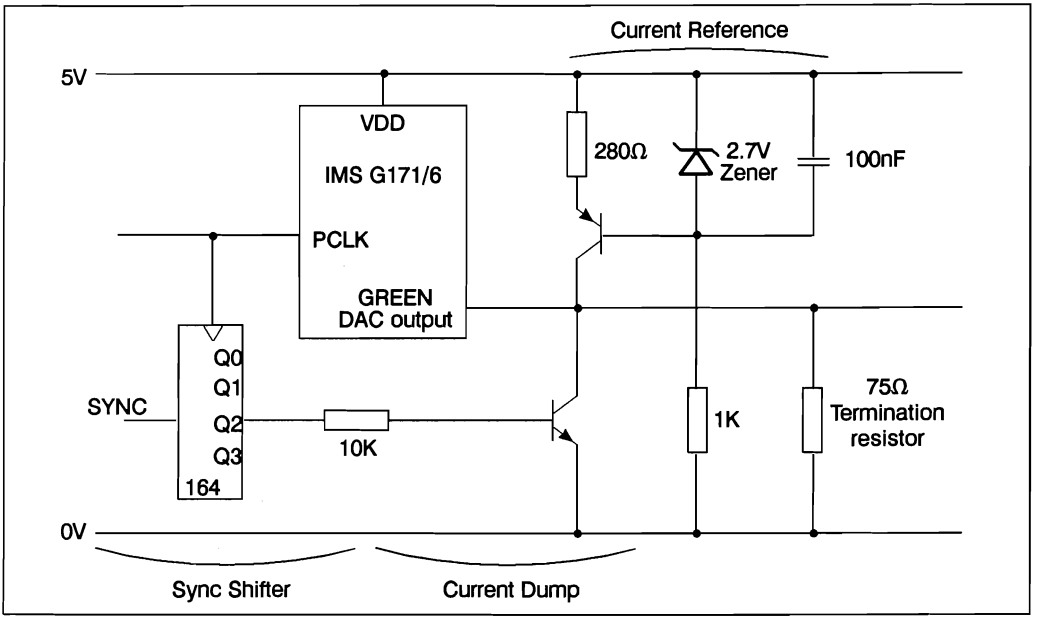


Figure 10.9 Adding an external sync pulse circuit to the G171/6.

Note that it is only necessary to build this circuit round the GREEN analogue output. Although all g17X parts with composite video provide sync signals on all 3 video outputs, most colour monitors only use the information provided on the GREEN channel.

The current reference circuit shown here should be perfectly adequate for most applications. Although the reference voltage established by the Zener diode may only be accurate to ±10% the absolute value of the sync offset should not be critical since most monitors are only A.C. coupled and are fairly tolerant to the magnitude of sync pulse provided. However, if a more accurate sync pedestal is required for a critical application, then the zener reference circuit should be replaced by one of the precision current reference circuits recommended for the IREF pin using either the LM-334 or the TL431.

10.3 Troubleshooting – common problems and their solutions

10.3.1 Unexplained colour changes on the screen

There are a number of possible causes for this effect which is due to corruption of the look-up table contents.

1 **Pixel setup and hold times not being met** – It is essential that the pixel inputs to the CLUT are stable within the window defined by the set-up and hold times on every sampling edge of the pixel clock, even during blanking periods. Any change of the pixel data applied to the device that occurs while the device is sampling its pixel input may result in an invalid address being applied to the look-up table. This asynchronous event may occur if for example the pixel data stream switches between banks of frame store RAM or a video RAM shift register is reloaded under the control of a system asynchronous to the pixel clock. Some mechanism must be put in place to re-synchronise this event to the pixel clock.

2 **Video data going tri-state** – In some systems the pixel data stream is made to go tri-state during blanking periods. If there is not a valid TTL level on the pixel inputs on the rising edge of pixel clock an invalid address may be applied to the RAM. The solution to this is either to leave the pixel data enabled, or to use pull-up resistors on the pixel inputs.

3 **Excessive undershoot on pixel inputs** – Due to the mismatch between the low impedence outputs of the TTL device driving the CLUT and the high impedence CLUT inputs, the pixel data port and pixel clock are the most common areas for signal undershoot. If this exceeds 1V this can cause device malfunction, or at worst latch-up. The section on 'Pixel Input' details termination methods and other recommendations to eliminate this problem.

4 **Asynchronous mask register updates** – On the IMS G170 and IMS G171 devices the pixel mask register must be updated synchronously with the data stream to avoid the possibility of the colour look-up table contents being corrupted. The timing and suggested hardware to achieve this are described in the appropriate datasheet. The pixel mask register synchronisation takes place internally on the IMS G176 and IMS G178 so all accesses to these devices can take place asynchronously without risk of look-up table corruption.

10.3.2 Grey streaks on light/dark boundaries

The possible causes for this effect are as follows:

1 **Noise on VCC and IREF pins of CLUT** – To get a constant full-scale DAC output the voltage between VCC and IREF must remain constant. If there is appreciable noise on VCC supply and the current reference cannot track the variations, this voltage difference will not be constant and incorrect DAC output will occur. In this case coupling capacitors should be used between IREF and VCC, typically a 100nF low-inductance chip capacitor in parallel with a 47μ tantalum should be used.

2 **Unneccessary decoupling on current reference** – Many current reference circuits in reality will have a high enough bandwidth to track any variations in VCC very well. In such cases it may well be that, particularly for high-speed applications, any decoupling between IREF and VCC will serve to slow down the current reference response so that it does not track VCC correctly. It is therefore worth trying both with and without current reference decoupling in applications where this streaking occurs.

3 **Poor quality monitor** – It should be noted that the above problem may not be due to the graphics system design at all. If the monitor used is of poor quality and has insufficient HT regulation then this effect will occur however good the system design is.

Designing with INMOS colour video controllers

11.1 Programming the IMS G300 colour video controller

11.1.1 Introduction

Programming the IMS G300 Colour Video Controller (CVC) is no more difficult than writing to any other memory mapped device. This text explains, from a programmers point of view, how to read, write, and program the IMS G300. It should be read in conjunction with other INMOS publications, namely the data sheets for the IMS G300A and IMS G300B, (and associated bug lists), the INMOS graphics data book, and INMOS technical notes 62 and 66. The technical notes explain the design and the use of the INMOS IMS B419 graphics TRAM, using the IMS G300. In particular, technical note 66 explains the use and control of the IMS G300A and the IMS B419 as well as using the feature enhancements on the IMS G300B.

11.1.2 The IMS G300 memory mapping

The IMS G300 is memory mapped as a 1/2 K word block into the host processor's address map, allowing fast and flexible configuration and updating of the IMS G300's parameters and palette contents. Registers are addressed on word boundaries. This can be easily achieved by placing a word array at the appropriate address (IMS G300 base address), and accessing elements within the array. The interface to the host processor can be either byte wide (8 bits) or word wide (24 bits). Clearly if the host interface is operating in byte mode, then this array would not be placed at the IMS G300 base address, and a procedure would be invoked to write the words as a sequence of 3 bytes.

11.1.3 Host access to the IMS G300 internal registers

The IMS G300 is read and written using words (24 bits) or bytes (8 bits) depending upon the word length of the host processor and the hardware system design. Bit 7 in the control register controls whether the host interface operates in byte or word mode. Note that byte mode on the A revision does not work when accessing the palette.

After reset, the host interface defaults to word mode. Setting bit 7 in the control register (by writing #80 in word mode) causes the host interface to operate in byte mode.

To write to the IMS G300 using byte mode, three successive bytes must be written to the same address consecutively, in byte little endian order (least significant byte first). When reading from the device, the data is read back in a similar manner. The use of byte mode with the IMS G300A (in mode 1) should be avoided, because byte accesses to the palette do not work. Mode 2 can be used in byte mode, however, as the palette is not used. In this case, care must be taken that bytes are always written correctly, 3 bytes at a time. The IMS G300A does not detect any address changes during these writes, or abort the write operation should there be one. Bytes are written individually, rather than after 3 bytes have been written.

Any address changes detected by the IMS G300B (caused by accessing another on-chip register, for example) before this sequence of three writes has been completed will abort the operation and *none* of the bytes of the destination register will be updated. The address change detection logic causes the byte counter to be reset. Similarly, if an address change is detected during a three byte read sequence, then the second and / or third bytes read will be incorrect, due to the byte counter being reset.

11.1.4 The internal sections of the IMS G300

The IMS G300 comprises the video timing (data path) registers, the boot location (phase locked loop multiplier), the top of screen and mask registers, and the control register. In addition to these there is a 256 by 24 bit look up table (LUT) that is used as the colour palette.

11.1.5 The control register

The control register is 24 bits wide, and controls the functionality, the operating mode, and the host interface of the device. It also controls the Video Timing Generator (VTG). The bit assignments and explanations can be found in the IMS G300 data sheet. This register can be accessed at any time.

11.1.6 The data path registers

The data path registers must always be read or written with the VTG disabled. This is achieved by writing 0 to bit 0 in the control register. Attempting to read or write the data path registers while the VTG is enabled will result in invalid data being transferred.

These registers must be set to their appropriate values depending upon the primary display parameters (required resolution, frame rate, video frequency etc.) and the monitor being used. A program is available from your local INMOS sales outlet, that can generate a test card and other test images, and automatically calculate (and program) the data path register values, interactively. This greatly eases their calculation for any particular parameters such as screen resolution and frame rate. Note that all these registers must be non-zero.

11.1.7 The mask register

The mask register is 8 bits wide, and is logically AND'ed with the pixel data in mode 1. The pixel data will be 8 bits wide with the IMS G300A, but could also be 4,2 or 1 bits wide if using the IMS G300B. The register is programmed by writing to the least significant byte at the appropriate word address. This register must only be accessed with the VTG disabled.

11.1.8 The boot location (phase locked loop multiplier)

This must be the first location written following reset, and can only be written once. If the device must be re-programmed, and this value needs to be changed, then reset must be asserted, and deasserted, then the new value can be written.

With the IMS G300B, bit 5 in the boot location controls the operation of the phase locked loop, 0 or 1 disabling or enabling respectively.

11.1.9 Colour palette

The colour palette must always be read or written when the VTG is not actually displaying pixel data, i.e. when the VTG is disabled, or during frame flyback time. Reading or writing while the VTG is displaying pixel data will result in invalid data being transferred, and probably streaking appearing on the screen.

It is often convenient to program the palette using a single block transfer (from another array). This will usually be more efficient, and should ensure that the palette access does not exceed the frame flyback time.

The colour palette (256 by 24 bits) is addressed by the pixel data values, and must contain the colour value that is to be displayed for each pixel value. The IMS G300A uses the palette only in mode 1, at 8 bits per pixel (accessing the 24 bit RGB colour value), but the IMS G300B uses it in both mode 1 and mode 2 (24 bits per pixel). In addition, the B revision also uses the palette in mode 1 when using 4,2 or 1 bits per pixel. In these cases, the first 2^n palette locations are used, where n is the number of bits per pixel. In mode 2 (with the B revision) the use of the colour palette allows full colour gamma correction, with individual transfer functions for each colour, to be performed with zero processor loading. In this case, each 8 bit pixel data field accesses one of the 256 8 bit R, G or B colour value fields.

11.1.10 Resetting and re-programming the IMS G300

11.1.11 The effect of reset

Reset causes the VTG control bit (bit 0) in the control register to be cleared, thus disabling the VTG. In addition, the host interface defaults to word mode following a reset.

Data in the palette and the data path registers is preserved following reset, with the exception of the boot location register, which must always be rewritten immediately following reset. Indeed this is the method by which the boot location value is altered, by resetting the device.

Clearly if the device is actually powered off and on again, then reset, the contents of all the registers and the colour palette will be undefined. Apart from this, the state of the device will be as above, following the reset.

11.1.12 Initialising the IMS G300

There are two different parts of the IMS G300 that must be programmed, the internal registers and the colour palette, (assuming that no data has been preserved from previous usage, as discussed above).

The IMS G300 must be initialised in the correct sequence. The boot location (phase locked loop multiplier) must be written first. The control register is then written, in order to put the device in a known operating mode, (with the VTG disabled by setting bit 0 to 0). The data path registers must then be written (in any order, although it is often convenient to write these using a block transfer, as with the palette). The palette can then be written, then finally the VTG can be enabled by setting control register bit 0 to a 1. These actions are summarised below:

1 Assert then deassert reset

2 Write phase locked loop multiplier (with bit 5 set if appropriate)

3 Write control register to set desired operating mode

4 Write data path registers

5 Write palette (if required)

6 Enable VTG by setting control register bit 0

11.1.13 Re-programming the IMS G300

The IMS G300 can be re-programmed at any time, to alter the operating mode or the screen display parameters. In order to do this, the VTG must first be disabled, by writing 0 to the control register bit 0. The data path registers may then be written (and the colour palette if required). Finally the VTG can be re-enabled, together with setting any new operating mode (if required). This is summarised below:

1 Disable VTG by writing 0 to control register bit 0

2 Write required data path registers (and colour palette)

3 Enable VTG and select new operating mode (if required)

11.2 Using the IMS G300B feature enhancements

11.2.1 Introduction

A number of features and enhancements have been incorporated in the IMS G300B, in addition to those already present on the IMS G300A.

These are listed below.

- New bits per pixel options, 4,2,1
- Use of the colour palette in mode 2
- Composite blank input / output
- Software control of phase locked loop
- VRAM transfer address step control
- Common screen data organisation for interlace and non-interlace modes
- Enhanced operation of host interface in byte mode

This text explains how to use the major feature, being the use of different bits per pixel (8,4,2, and 1) in mode 1. The use of the other features is covered elsewhere, in section 11.3, *Moving software from the IMS G300A to the IMS G300B*.

11.2.2 Different number of bits per pixel

The number of bits per pixel can be 1, 2, 4, or 8 in mode 1. The main use of this is to increase the speed of drawing shapes, PIXBLT operations, and moving (expanding) text to the screen, as well as reducing the VRAM memory requirements.

When using lower numbers of bits per pixel, the little endian convention is adhered to, in terms of bytes and bits. It may be noted that reducing the number of bits per pixel means that pixels cannot be manipulated using `BYTE` writes, as with 8 bits per pixel.

One technique that can be used is to write multiple pixels using a composed 8 bit colour byte value. This technique would only be used when the number of pixel bits to be written was a multiple of a byte. Clearly if a read modify write operation is to be performed, using less than 8 bits per pixel, then shift and mask operations will be necessary.

The colour palette will also need to be re-programmed, when using less than 8 bits per pixel, as this reduces the number of colours that can be displayed on screen at any one time. In 4 bits per pixel mode, palette locations 0 to 15 are used. In 2 bits per pixel mode, palette locations 0 to 3 are used, and in 1 bit per pixel mode only palette locations 0 and 1 are used. All other palette locations are not used in these modes.

To alter the number of bits per pixel, bits 18 and 17 are set appropriately in the IMS G300B Control Register, as shown in table 11.1:

Bits per pixel	Bits 18 and 17
8	11
4	10
2	01
1	00

Table 11.1

One important point must be noted when changing the number of bits per pixel, in order to keep the memory organisation continuous. Normally, in 8 bits per pixel, the **TransferDelay** and **MemInit** register values sum to the VRAM shift register length (512). With 4 bits per pixel, however, they must sum to twice this value, 1024, as the VRAM register length now corresponds to twice the number of pixels. **TransferDelay** remains constant, and **MemInit** is therefore calculated to be the difference. Similarly, when using 2 bits per pixel, these two parameters must sum to 2048, and 1 bit per pixel, to 4096. These values are summarised in table 11.2.

Bits per pixel	TransferDelay + MemInit
8	512
4	1024
2	2048
1	4096

Table 11.2

As an example, suppose that **TransferDelay** was set to 18, and **MemInit** set to 494. The values for different bits per pixel are therefore as shown in table 11.3:

Bits per pixel	TransferDelay	MemInit
8	18	494
4	18	1006
2	18	2030
1	18	4078

Table 11.3

If **MemInit** is not altered as shown above, then the displayed memory will not be continuous, and will have line gaps after each displayed line, due to the shorter length pixels. The screen display would also be totally wrong.

The major disadvantage that reducing the number of bits per pixel has is that the number of colours that can be displayed at one time is reduced, to 2^n, where n is the number of bits per pixel, as mentioned above. Another disadvantage is that the drawing of lines, figures and objects is different, and is not BYTE oriented anymore.

11.2.3 Address step control

Bits 20 and 19 together with the interlace bit, bit 2 in the IMS G300B Control Register allow the size of the VRAM transfer address increment to be specified. This was fixed with the IMS G300A, but can now be set

to be one of 8 different values. This facility allows greater flexibility when using interlace mode, allowing the framestore format to remain the same as for non-interlace mode. With the G300A, the screen bitmap has to be split into the relevant fields in interlace mode. This address step control also allows the correct field to be incremented when the IMS G300B addresses the VRAMs. Incrementing by 256, 512 or 1024 allows the use of different sized VRAMs (64Kbit, 1 Mbit and 4 Mbit devices respectively). This is dealt with in more detail in the IMS G300B data sheet.

11.2.4 Blank I/O

The IMS G300B has a Blank I/O pin that allows one IMS G300B to blank the output from another IMS G300B. Bit 16 in the Control Register configures this pin as either an input or an output.

11.3 Moving software from the IMS G300A to the IMS G300B

11.3.1 Introduction

The first engineering samples of the IMS G300 were designated revision 'A'. However, following much customer consultation, the device was enhanced with a number of additional and improved features. This device is currently in production and is designated revision 'B'. The following text provides an overview of the hardware and software changes required to upgrade an IMS G300A design to a G300B design. Reference should be made to other INMOS publications, namely the data sheets for the IMS G300A and IMS G300B, and INMOS technical notes 62 and 66. The technical notes explain the design and the use of the INMOS IMS B419 graphics TRAM, using the IMS G300. In particular, technical note 66 explains the use of the IMS G300 and the IMS B419 as well as using the feature enhancements on the IMS G300B.

11.3.2 Differences between the revisions A and B

There are several enhancements implemented on the IMS G300B. These are listed below.

- New bits per pixel options, 4,2,1
- Use of the colour palette in mode 2
- Composite blank input / output
- Software control of phase locked loop
- VRAM transfer address step control
- Common screen data organisation for interlace and non-interlace modes
- Enhanced operation of host interface in byte mode

11.3.3 Software changes required when upgrading from revision A to B

The IMS G300 revision B is upwardly software compatible with revision A except for the initialisation. A couple of minor but important changes must be made to this part of the software when upgrading from IMS G300 revision A to B. This section details the changes required, assuming that none of the IMS G300B feature enhancements are being used, so the device is thus functionally operating in exactly the same way as before.

11.3.4 Bits per pixel

Different bits per pixel can now be used with the IMS G300B, being 4,2 and 1 in addition to the 8 and 24 bits per pixel modes on the A revision. In order to use 8 bits per pixel, bits 18 and 17 in the control register must both be set high. This may be achieved by logically OR'ing the control register value with #60000 or 393216_{10}, or adding this value.

11.3.5 Use of the colour palette in mode 2

With the IMS G300A in mode 2 the 24 bit pixel values were used as the three 8 bit colour values for RGB directly, without using the colour palette. The IMS G300B uses the three 8 bit pixel value fields to address the colour palette, thus generating the three 8 bit colour values for RGB. This allows gamma correction and non-linear colour translations to be performed for each colour individually. This does mean, however, that the IMS G300B colour palette must be correctly programmed when operating in this mode. A simple one to one identity translation can be performed by programming the three colour values at each palette location with their address. Location *n*, for example, would be programmed with:

$$n\ OR\ ((n \ll 8)\ OR\ (n \gg 16))$$

Note that this does not perform any function between the input pixel value colour fields and the output RGB colour values.

11.3.6 Composite blank input / output

The IMS G300B allows a composite blank signal to be either an input or an output. Bit 16 in the control register controls the direction of this. This bit must be set high (CBlank set to output) in order for this function to be inactive. This may be achieved by logically OR'ing the control register value with #10000 or 65536_{10}, or adding this value.

11.3.7 Phase locked loop control bit

Bit 5 in the boot location controls the phase locked loop with the B revision. This must be set high to enable the phase locked loop, if desired. This may be achieved by OR'ing the multiplier value required with #20 or 32_{10}, or adding this value.

11.4 Hardware design upgrading from the IMS G300A to the IMS G300B

11.4.1 Introduction

This note describes the hardware changes required when upgrading from the IMS G300A to the IMS G300B. Reference should be made to section 11.3, 'Moving software from the IMS G300A to the IMS G300B' and data sheets for both the IMS G300A and IMS G300B in conjunction with this text.

11.4.2 Modifying a board designed originally with the IMS G300A to accept an IMS G300B

An existing board designed orginally for an IMS G300A can be upgraded to take advantage of the extended features of the IMS G300B. This would be done, for example, where use of the alternative pixel colour resolution modes (bits-per-pixel) of the IMS G300B were desired from a pseudo-colour system, or where use of the colour palette for gamma correction was desired for use with a full-colour system.

There are a number of differences between the two device revisions that need to be catered for. The IMS G300A employed two separate pins for the provision of device clocks, **PixClkIn** for use with a dot-rate clock and no on-chip frequency multiplication, and **PllClkIn** for use with the input clock for the on-chip phase-locked loop. Since these were alternatives, they have been combined on the IMS G300B to one pin, **ClkIn**, which is in the same physical position as **PllClkIn** was on the 'A' revision. The choice of whether the phase-locked loop (PLL) is enabled or disabled is then made by the logic state of a new bit allocation in the boot location, bit 5 of word address **#X1A0**, which must be written to during the device initialisation sequence. A '1' in this bit position enables the PLL, whilst a '0' disables it.

The **PixClkIn** pin freed by this re-design has been allocated a new function, and is called **CBlank**. Two bits in the control register, bits 16 and 23, configure the function performed by this pin, and a full description of its use can be found in the datasheet. Since the **CBlank** pin can be configured to be either an input or an output, it must be set as an output (control register bit 16 high) when used in a board where the device is replacing an 'A' revision part. In this situation the **CBlank** pin will be left disconnected and unused, and hence the value stored in bit 23 of the control register is irrelevant.

Hence for a pseudo-colour system designed around the 'A' revision part and making use of the PLL, a 'B' revision part can be used as pin-compatible replacement by ensuring that there is no connection to the **CBlank** pin. If the system has been designed not to use the PLL, and the device clock is therefore supplied to the 'A' revision **PixClkIn** pin, the board must be modified to move this to the 'B' revision **ClkIn** pin, and any connection removed from **PixClkIn** to allow **CBlank** to be driven out. In this case, bit 5 of the boot location would be set to a '0' on device initialisation to configure the **ClkIn** pin as a 'times one' input device clock.

Quality and reliability

A.1 Quality and reliability

The following information describes in a precise form the SGS-THOMSON approach to Quality and Reliability. The subject is comprehensively detailed in the SGS-THOMSON Microelectronics Quality and Reliability publication SURE 5. This program is also applied totally to INMOS products.

A.1.1 Introduction

The Quality and Reliability of a product depend on all the activities from the conception and design of a new product, through production and shipment, to the service given to the customers.

It is well known that Reliability must be designed into the product and the process. To manufacture consistently reliable high quality products, SGS-THOMSON believes that it is essential for everyone in the company to appreciate the importance of maintaining and improving the levels of Quality and Reliability.

SGS-THOMSON has adopted a Total Quality Control approach which means that everybody in the company must work to improve Quality.

With this approach problems can be solved at the stage where they arise, so that latent failures are not carried over to the next stage or to the finished product. Total Quality Control assures the conditions to avoid quality problems rather than simply eliminating defective finished products.

A.1.2 Quality culture

It is the precise choice of SGS-THOMSON to win its customers' trust via the establishment of a position of leadership for Service and Quality. The company must therefore have a quality based culture.

This culture can be seen in the individual behaviour of every person within the company and in the way each person interacts with his or her fellow worker to establish new and ever more demanding goals. It is sustained and nurtured through well defined policies, procedures, training and, of paramount importance, through examples from the very highest company management levels.

That quality is perceived as a company wide responsibility is no more obvious than in the field of training. An ongoing program, called Total Quality Control, was started in 1982 to involve all people and departments in the company, wherever the company operates throughout the world.

Total Quality Control takes the position that it is not enough to believe that things must be done, you must be able to do them. To this end it has as its primary objectives:

- Promotion of the Total Quality Control concept
- Training on statistical tools for people from all departments
- The creation of technical work groups for specific quality improvement programs
- The introduction of quality circles

Fundamental to this program is the conviction that quality is not an option, it is an obligation and that everyone in the company can, given suitable motivation and training, make a real contribution to overall improvements in quality levels.

From the very highest management levels and involving designers, engineers, production, supervisors and line operators in addition to Quality and Reliability people, the Total Quality Control program focused on:

- Personal motivation
- Quality in design
- Reliability in design
- Improved statistical process control
- Customer satisfaction

Recently SGS-THOMSON has begun a new company wide campaign *Quality and Service Culture for Excellence* based on the premise that basic quality ideas and methodology, if applied properly, will give:

- Complete Customer satisfaction
- Zero defect products
- Minimum product costs

These three basic ingredients for excellence will be complemented by a long term program to improve data processing networks and to reduce response times at all levels as well as the focusing of everyone's efforts on service, on quality and on process stability.

Our ultimate goal is to supply the products requested by our customers with zero delinquency, zero defects and of course 'just in time'.

A.1.3 Organisation and management

SGS-THOMSON is organised in product Divisions/Groups, Geographical sales areas (Regions) and Corporate departments.

Quality and Reliability control activities are managed, performed and promoted by the Corporate Service and Quality group (which reports to the top management) and Quality and Reliability departments at Division/Group and plant level.

Part of Corporate Service and Quality group is the Central Reliability and Quality Control department. This organisation makes it possible for SGS-THOMSON to handle Quality and Reliability for an extensive product range both effectively and efficiently.

Education and Training programs in the field of Excellence and Quality are managed by the Corporate Service and Quality organisation in cooperation with the Human Resources department.

At every production location there is an incoming inspection department with the job of assuring the quality of purchased materials.

Divisional Quality and Reliability departments evaluate the reliability of new processes and new products, before they go into volume production.

They require and coordinate corrective actions necessary to improve Quality and Reliability of products and processes; these improvements are planned in quality budgets.

They perform and collect reliability results and issue reliability reports for their products.

Division Quality and Reliability departments interface directly with customers from design phase to approval of customers' product specifications. In the past, successful in-house customer qualification, testing

and joint qualification programs with customers has been achieved. SGS-THOMSON remains committed to these joint customer/vendor programs.

Plant Quality and Reliability departments perform all the Quality and Reliability inspections and controls relevant to production done in their plants such as: incoming inspection, in process control, outgoing inspection, reliability testing and failure analysis.

A.1.4 Quality by design

Since the Quality and Reliability of semiconductor devices depend to a large extent on the basic structure, SGS-THOMSON pays careful attention to Quality and Reliability studies at the design stage, paying deep attention to the users' reliability requirements and operating conditions. Quality and Reliability checkpoints for materials, process and device structure are considered from the design phase on.

One of the key steps is the Design Review which consists of a study of design documents, the definition of reliability test methods to check on the compatibility of processes with design goals and conditions of use, and review of failure mechanism history in similar products.

In addition, qualification procedures are used mainly to ascertain the main characteristics of new processes/products (or to evaluate process/product changes) and to guarantee the availability of a characterisation and the complete set of specifications for introduction to SGS-THOMSON manufacturing. Qualification should demonstrate capability to meet customer requirements.

A.1.5 Quality auditing

SGS-THOMSON performs quality audits to verify that products, processes, programs and the Quality and Reliability organisations are all in accordance with the written procedures and specifications.

A quality audit does not replace the normal quality monitors or acceptance but helps to ensure that everything is being done as it should be and to anticipate quality problems.

SGS-THOMSON factories are familiar with internal and external audits.

A.1.6 Documentation control system

Quality and Reliability are measurable features. But, for measurements to have any meaning, they must be carried out in accordance with strict procedures and methods. Similarly, production processes must be managed in a repeatable way. This means that detailed instructions and descriptions of every process step must be prepared and kept updated.

This information is formalised in the company's specifications that cover all the procedures and process instructions. The Documentation Control System, therefore, documents all the various manufacturing processes and encompasses the SGS-THOMSON technical know-how.

The Documentation Control System consists of a series of documents properly organised by subject and content. The system is managed and administered by Document Control at Divisional Documentation Control Centres for efficiently issuing, updating and approving specifications. Special text processing software is used to issue specification documents, allowing access to the updated versions only, ensuring rapid updating and distribution of documentation. The Documentation Centres guarantee homogeneity in specifications, record changes histories and issue general specification procedures.

A very strict company procedure governs the engineering changes (issue, approval and modifications).

A.1.7 Reliability assurance

Reliability testing is an ongoing process adopted to identify and then improve reliability performance.

Accelerated tests, such as extended temperature operating life, THB and temperature cycling, are important tools for evaluating long-term reliability and stability of process and product parameters.

SGS-THOMSON performs rigorous tests throughout production to ensure that production devices have the properly designed reliability.

Reliability tests are conducted in two stages.

First we test our engineering samples during design and development stages to see if their Quality and Reliability corresponds to that called for in the design.

Reliability testing is usually performed on a small sample but for long periods or under very accelerated conditions to investigate wear-out failures and to determine tolerances and limits of design. For these tests it is also possible to use the step-stress procedure (for example, ESD resistance evaluation).

The second type of test is performed periodically during production to check, maintain and improve the assured Quality and Reliability levels.

The reliability tests involve both environmental and endurance examination and are performed under conditions more severe than those met in the field. These conditions, are chosen to accelerate, the occurrence of failures that would appear in actual operation, and care is taken to ensure that the failure modes and mechanisms are unchanged. The data from reliability tests provide an objective tool for product performance evaluation under a wide range of conditions.

When a failure occurs, the SGS-THOMSON engineers conduct an in-depth analysis of the failure mechanism/mode to apply immediate suitable corrective actions.

Reliability testing activity during recent years has been extended to all SGS-THOMSON factories with new and advanced equipment enabling all the plants to perform all the main tests.

Graphics glossary

B.1 Graphics glossary

Aspect ratio — The ratio of width to height. An emerging work station standard is 1280×1024 pixels (i.e. 5:4). For the picture transmitted by a television station, the aspect ratio is 4:3.

Back porch — The portion of a horizontal blanking pulse that follows the trailing edge of the horizontal synchronising pulse (ie at the start of the displayed line).

Bandwidth — The number of bits of information per second that can be transferred by a device.

Bit map — The digital representation of an image in terms of pixels, usually stored in the video memory (RAM). The pixels in the bit map are mapped directly to the appropriate location on-screen.

Black level — The amplitude of the composite signal at which the beam is 'off' (not visible).

Blanking — Part of the composite signal whose amplitude makes the vertical and horizontal scan retrace not visible on the monitor, i.e the display electron beam is cut off (blanked).

Blanking level — The amplitude of the front and back porches of the composite video signal.

Blanking period — The time when the composite video signal is reduced in amplitude to the blanking level, i.e. below which the display electron beam is cut off. This allows the beam to go from the right side of the display to the left at the end of each linescan without being visible (horizontal blanking) and from the bottom right of the screen to the top left of the screen (vertical blanking).

CLUT — Colour look-up table or colour palette.

Colour table — The memory inside the colour look-up table device containing the detailed colour values.

Colour value — A word stored in the colour table defining the colour of a pixel in terms of its red, green and blue intensity.

Composite sync — To provide a timing reference to the monitor indicating the point where a new frame or a new line starts, all monitors require two types of sync pulses – frame sync and line sync. Frame and line sync pulses are distinguished by their duration. Frame sync pulses are longer than line sync pulses. For a typical high resolution monitor, a frame sync pulse might be 50 to 100μs whereas line sync pulses would be in the region of 2 to 6μs.

Composite Video — The composite video signal is the whole video signal consisting of the pixel information, horizontal and vertical blanking, colour and line synchronisation. There are two different approaches to providing sync pulses. Composite video superimposes these timing pulses onto the analogue video signal (approximately a 0.3V pedestal on a 0.7V video signal using the RS170 standard). Most monitors strip the sync on information from just the green channel, even though INMOS devices provide sync on all three channels. A separate sync video system, as its name suggests, supplies the sync pulses on an extra signal line to the monitor; although it has the advantage of not requiring a circuit to strip the sync timing from the video inputs inside the monitor.

CRT — Cathode Ray Tube.

DAC — Digital to Analogue Converter.

Display Memory — The area of memory used to store the digital representation of the screen image output to the video monitor.

DRAM Refresh — The operation of maintaining data stored in dynamic RAMs. The data stored in a DRAM is represented by charges across a grid of capacitive cells. The charges leak over time so it must be refreshed periodically. This is in addition to screen refresh.

Frame Buffer — Often referred to as the 'bit-map' of the display, it is a portion of memory containing the logical pixels corresponding to the point on the monitor screen.

Fly-back The period when the blanked electron beam returns from the right side of the screen to the left, or from the bottom of the screen to the top. This period is often used to update the palette, or toggle the screen etc.

Frame Frequency See frame refresh rate.

Frame Refresh Rate Frame rate defines the frequency at which each new frame is drawn in the screen. Too low a frame rate can lead to a perception of the image flickering on the screen.

Frame Store The digital representation of the displayed image in the form of a 2-dimensional array of pixels.

Front Porch The portion of a horizontal blanking pulse that precedes the leading edge of the horizontal sync pulse ie. after the displayed line.

Full Colour As true colour, but specifically 24-bits per pixel. This is currently an industry standard for high performance displays and is used in many applications such as laser disks and video cameras.

Gamma Correction Due to the nature of the phosphors used on colour monitor screens, colour intensity displayed is a non-linear function of the applied electron beam. Gamma correction is the process of approximately eliminating these non-linearities by translating the pixels in a look-up table before they are converted into analogue signals.

Grey Scale A scale of light intensities incrementing from zero to full scale where RGB components are always equal.

Horizontal Blanking The blanking signal at the end of each line that prevents the retrace of the display electron beam from being visible.

Horizontal Retrace The rapid return of the scanning electron beam from the right of the screen to the left.

Horizontal Sync The synchronising signal that signifies horizontal retrace of the electron beam of a CRT display.

Interlaced Scanning A system of picture scanning. Odd numbered scanning lines, which make up an odd field, are interlaced with the even numbered lines of an even field. These two fields are refreshed alternatively. The two interlaced fields constitute one frame.

Interlaced Screen A technique used to lower the video dot rate whilst still maintaining a high screen resolution. Interlaced displays refresh just alternate lines of the image on every frame scan, swapping between odd and even lines on each successive sweep.

Look-Up Table The colour map or palette which is used to convert the colour pixel code into the detailed colour data for the three DACs.

Memory Map An area of memory space partitioned into addressable blocks.

Multiplexing The action of sending more than one set of signals at once over a single communication link.

NTSC National Television Standards Committee - a group instrumental in setting standards in North America and Japan - eg. RS-343A, EIA-343A and RS-170. The PAL (CCIR) and SECAM standards are used in Europe.

Overlays Overlays are extra planes in a graphics frame store which contain pixel information and is substituted for a normal pixel data on a pixel by pixel basis. Often used for cursor and grid information.

Palette See Look-Up Table.

Panning The ability to move part (or whole) of the display with respect to the boundary of a window or the edge of the screen.

Pixel Picture Element - the smallest unit of display memory which can be individually controlled.

Pixel Panning The ability to pan by one pixel at a time.

Pixel 'Address' The pixel value stored in the frame store and used to address colour values in the CLUT. This could also refer to the x-y address of a pixel on the display.

Psuedo-Colour A colour scheme where the pixels experience colour expansion when passed through a look-up table prior to being sent to the video DACs. In this scheme the pixels stored in the frame-store are used as an address to look-up the appropriate colour value containing a much larger number of bits, the colour value is then applied to the DACs. This greatly reduces the amount of frame store required to hold an image while still retaining the total colour resolution.

Raster A rectangular grid of pixels whose intensity levels are manipulated to represent images. In a bit-mapped display, the bits within a portion of the memory, referred to as the frame buffer, are mapped to the raster pattern of a CRT monitor.

Raster Display A CRT display generated by an electron beam that illuminates the CRT by sweeping the beam horizontally across the phosphor surface in a predetermined pattern, providing substantially uniform coverage of the display area.

Raster Scan The grid pattern traced by the electron beam on the face of the CRT in a TV or similar raster-scan display device.

Resolution The screen resolution refers to the number of individual pixels making up the screen. The colour resolution refers to the total possible number of colours available at once. The DAC resolution refers to the number n, where 2n is the number of discrete analogue levels which the DAC is capable of converting.

RGB Signal The Red Green and Blue analogue signals required to drive an analogue monitor.

Retrace The line traced by the scanning beam of a picture tube as it travels from the end of one horizontal line to the beginning of the next.

RGB Monitor Red-Green-Blue CRT Monitor.

Scan Line A horizontal line traced across a CRT by the electron beam in a TV or monitor.

Screen The portion of a graphics system upon which the image actually appears.

Screen Refresh The operation of dumping the contents of the frame buffer to a CRT monitor in sync with the movement of the electron beam.

True Colour A colour scheme where the pixels bypass the look-up table (except for gamma correction) and are sent straight to the DACs without colour expansion. This method allows access to be gained to all possible colours simultaneously.

Vertical Sync The synchronising signal that enables vertical retrace of the electron beam of a CRT.

VGA Video Graphics Array - the graphics standard introduced by I.B.M. in their PS/2 range of PCs. IBM use the INMOS G171 CLUT in this range to achieve the VGA standard.

Video Memory See bit-map/frame buffer.

Video RAM or Video DRAM Video Dynamic Access Memory. A dual ported memory device for computer graphics applications, containing two interfaces; one to allow a processor to read or write data from an internal memory array; a second interface to provide a serial stream of screen refresh data to a CRT display device.

Window A specified rectangular area of a virtual space shown on the display.

Zoom To scale a display or display item so it is 'magnified' or 'reduced' on the screen.