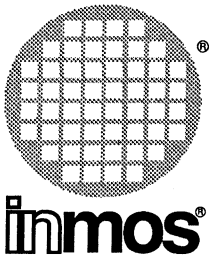

GRAPHICS DATABOOK

First Edition November 1988

INMOS Databook Series

Transputer Databook
Military Micro-products Databook
Transputer Development and *iq* Systems Databook
Memory Databook
Graphics Databook
Digital Signal Processing Databook
Transputer Applications Notebook: Architecture and Software
Transputer Applications Notebook: Systems and Performance

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Contents

Preface

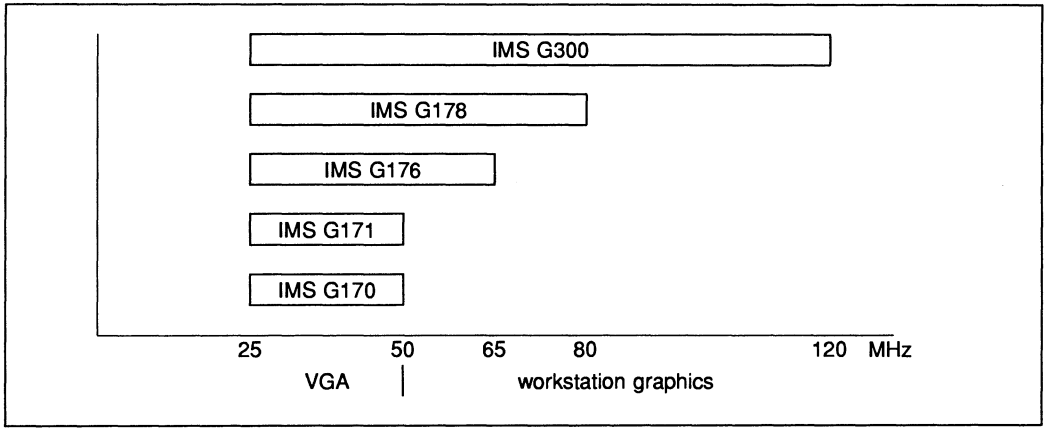
Graphics processing is a significant area of application for INMOS devices. The INMOS Graphics Databook has been published in response to the growing interest and requests for information concerning INMOS graphics devices.

The databook comprises an overview, engineering data and applications information for the INMOS IMS G171, G176 and G178 Colour Look-Up Tables (CLUTs), and the INMOS IMS G300 Colour Video Controller (CVC).

The INMOS family of colour look-up tables provide the analogue output stages for colour graphic systems. The device consists of a high-speed random access store or look-up table, three DACs, a pixel word mask and a microprocessor interface.

The INMOS G300 colour video controller provides all necessary functions for controlling real time operation of a raster scan video system, using dual ported DRAMs. The design enables the host processor to be isolated from the constraints of the real time system without interfering with the ability of the processor to specify and manipulate screen data. The device integrates all video timing and control circuitry, bit map to screen refresh management, colour expansion look-up table and data conversion/monitor drivers into a single chip.

In addition to graphics devices, the INMOS product range also includes transputer products, digital signal processing devices and fast SRAMs. For further information concerning INMOS products please contact your local INMOS sales outlet.



Applications of the INMOS graphics family

INMOS

1.1 Introduction

INMOS is a recognised leader in the development and design of high performance integrated circuits, and is regarded as a pioneer in the field of parallel processing. The company manufactures components that meet the processing needs of the most demanding applications today, and provides an upgrade path into applications of tomorrow. New designs under development will meet the requirements of systems in the next decade. Computing requires high performance, flexibility and simplicity of use, and these characteristics are central to the design of all INMOS products.

INMOS now has over 10 years experience in the memory and microprocessor industry and is looking forward to the future with confidence. The company has a solid record of innovation in a wide range of product areas for companies manufacturing systems in the United States, Europe, Japan and the Far East. As developers of the Transputer, a unique microprocessor concept with a revolutionary architecture, and the occam parallel processing language, INMOS has established the standards for the future exploitation of the power of parallel processing. Other INMOS products include a range of chips aimed at digital signal processing, to be used in areas such as radar, robot vision systems and high definition television. INMOS also has an established reputation as a manufacturer of high-speed static RAMs, a field in which it holds a greater than 10% market share.

This databook concentrates on another highly successful INMOS product line, that of high performance Colour Look-Up Tables and other components aimed at colour graphics systems. In 1985 the company launched the IMS G170, the first generation Colour Look Up Table (CLUT), and soon established a wide customer base. In 1986 minimal redesign of the IMS G170 resulted in the introduction of the IMS G171. This device rapidly became the industry standard and was adopted by IBM for incorporation into the IBM PS/2[1] range. A high speed version of the IMS G171, designated the IMS G176, was then released in 1987. This device is now available in PLCC at speeds up to 65MHz. These are being used to deliver an unprecedented cost-performance ratio in many display systems and have been chosen for use by most major international computer companies to improve the graphics capabilities of their latest range of personal computers.

In addition to extending and developing the CLUT range, INMOS has also diversified into the field of Colour Video Controllers (CVCs) with the IMS G300. This device integrates all video timing and control circuitry, bit map to screen refresh management, colour expansion look up table and data conversion/monitor drivers into a single chip.

The corporate headquarters, product design team and worldwide sales and marketing management are based at Bristol, UK.

INMOS is constantly upgrading, improving and developing its range of graphics products and is committed to maintaining its position as a world leader in this field.

1.2 Manufacturing

All products are manufactured at the INMOS Newport, Duffryn facility which began operations in 1983. This is an 8000 square metre building with a 3000 square metre cleanroom operating to Class 10 environment in the work areas.

To produce high performance products, where each microchip may consist of up to 300,000 transistors, INMOS uses advanced manufacturing equipment. Wafer steppers, plasma etchers and ion implanters form the basis of fabrication.

Assembly

Sub-contractors, primarily in Korea, Taiwan, Hong Kong and the UK, are used to assemble devices.

Test

The final testing of commercial products is carried out at the INMOS Newport, Coed Rhedyn facility. Military final testing takes place at Colorado Springs.

[1] IBM and PS/2 are registered trademarks of International Business Machines Corporation

1.3 Quality and Reliability

Stringent controls of quality and reliability provide the customer with early failure rates of less than 1000 ppm and long term reliability rates of better than 100 FITs (one FIT is one failure per 1000 million hours). Military requirements are even more stringent.

1.4 Future Developments

1.4.1 Research and Development

INMOS has achieved technical success based on its position of leadership in products and process technology in conjunction with substantial research and development investment. R and D investment has averaged 18 percent of revenues since inception and it is anticipated that the future investment levels will remain within this range.

1.4.2 Process Developments

One aspect of the work of the Technology Development Group at Newport is to scale the present 1.2 micron technology to 1.0 micron for products to be manufactured in 1988/89. In addition, work is in progress on the development of 0.8 micron CMOS technology.

graphics overview

2.1 The advancing graphics market

Recent years have seen graphics systems playing an increasingly important role in computer technology. The potential for future growth is expanding as the power of computer graphics hardware increases. Business systems, Graphics Design, Animation, Desktop publishing, CAD/CAM Workstations and Medical Imaging are just some of the application areas. The benefits offered to so many systems are likely to ensure continued and increasing demand for graphics and graphical interfaces for many years to come. Better communication of information, better user productivity and the introduction of computer systems to a wider non-technical audience are just some of the reasons behind the increasing importance of computer graphics. The growing volumes for graphics-based systems and the advances in silicon technology have both contributed to reducing costs of such systems and thus fuelling further increases in performance.

The trend towards higher resolutions, more colours and faster screen updates has spawned improved technology in computer graphics hardware. The need for high data rates in graphics systems was a major push in the development of fast DRAMs for example. Fast access modes such as page and nibble mode were the first steps in the quest to increase bandwidth, and now dual port video DRAM's with their on-chip serial shift registers are the most popular component for building high speed frame buffers.

One other significant component which has helped to enhance the performance of todays graphics systems is the colour palette or Colour Look-Up Table (CLUT). This is the device which converts the high-speed digital pixel data into the analogue signals required to drive an analogue colour monitor.

2.2 CLUTs and colour representation

With the developments in the performance of graphics systems has come the requirement to display many more colours on the screen. Increased resolutions demand a wider total range of colours, thus giving the subtle degrees of shading that the resolution makes possible. The bit-mapped method of storing a raster-scan image means that the more information about any pixel that has to be stored (e.g. its colour and intensity) the more memory it requires in the frame buffer. A single bit per pixel obviously gives a black and white display — each pixel is either on or off. Three bits per pixel (one for each colour gun) gives only eight crude colours, totally inadequate for serious graphics work. Increase this to say 8 bits per gun (24 bits per pixel) and you have a total colour range of over 16 million, which is more appropriate for the fine shading required by the solids modelling and CAD/CAE applications of today.

However, there is a price to pay. If a reasonable range of colours is provided, the overall memory requirement soon becomes prohibitively large, as does the processing power required to manipulate this data. For example, if each pixel in a 1K x 1K display used 8 bits to describe the intensity of each colour gun the overall memory requirement would be 3Mbytes. The main problem with this would be the cost, but it would also be difficult for a drawing processor to manipulate this amount of data quickly enough to avoid annoying delays whilst the screen is being updated.

The colour look-up table approach is to store a much smaller amount of data for each pixel, and to use this data to reference a location in a colour table. The table which contains the colour definitions then provides a larger amount of data to describe the particular colour required. The colour definitions stored in the table can be changed by the host processor according to the particular application. Typical CLUTs can accomadate up to 256 colours in a table or 'palette' at any one time, with each entry in the table being perhaps 18 or 24 bits wide. An 18 bit wide colour value (6 bits for each for red, green and blue) provides a choice from a total range of 264,144 colours, whilst a 24 bit colour value increases the choice to over 16 million shades.

The key factor in the colour look-up table solution is the availability of an enormous range of possible colours, but the acceptance that for a particular application, only a smaller sub-set of those colours will ever need to be displayed on the screen at any given time. Someone developing a flight simulator program may desire a large number of earth tones, predominantly greens and browns, with which to render his landscape; a solid modelling application may require various shades of one colour to give objects the illusion of depth, shape or illumination; a portrait library forming part of a security database may require only skin tones to portray human faces. The aesthetics and ergonomics of colour selection are also well catered for by the Colour Look-Up Table solution. Choosing a range of colours which are both pleasing and safe to look at for long periods can be important for, say, PCB layout where the designer may spend many hours looking at hundreds of fine lines packed closely together.

A great deal of effort has been put into developing dithering and histogramming techniques which make it possible to convert almost any full-colour picture into a 256 colour form which is very difficult to distinguish from the original.

2.3 The INMOS CLUT history

By drawing on its previous experience with high-speed memory devices, INMOS developed its first CLUT in 1985. The first example, the IMS G170, provided a palette of 256 colours, from a total range of over 256K colours. Additional features such as the implementation of composite sync on the outputs, a pixel mask register and compatibility with industry video signal standards made it an instant success, offering a cheaper yet better performance option to many of the existing hybrid solutions. The current INMOS family of CLUTs provides a range of speed, functionality and cost. Further members of the family are under development.

The success of these parts can be judged by their rapid uptake by many of the industry's biggest colour graphics users, the greatest testament being their use by IBM in the latest range of PS/2[1] machines for their VGA graphics systems.

2.4 Graphics controllers and drawing processors

Graphics controller chips started as devices which provided only the CRT control signals. More recent graphics engines also perform bitmap operations and take the more computationally intensive graphics drawing tasks away from the processor by having a set of hardwired primitives, allowing the processor to run certain types of application program much faster.

However there is a danger with casting drawing algorithims in silicon. With graphics algorithms continually changing, any drawing primitive that is hardwired into the silicon of a graphics engine becomes expensive and time-consuming to replace. The trend now therefore is for drawing algorithms to remain in software, running on a processor, or if performance dictates — several processors. In this way improved or new algorithms require only software upgrades and do not require the purchase of new and expensive hardware. The latest graphics component from INMOS, the IMS G300 Colour Video Controller (CVC), supports this system architecture, and leads the way into flexible any truly upgradeable graphics systems.

2.5 Computer displays

Monitors too are developing to keep pace with the other components in the system. The trends are set for finer dot pitches to improve detail, higher screen refresh rates to reduce flicker and improved brightness to enhance readability.

Multisync monitors available now address the problem of interfacing to a variety of systems with different CRT timing signal outputs, yet this could be seen as approaching the problem from the wrong direction. Multisync monitors are partly a solution to the limitations of the graphics controller devices which provide only fixed or limited programmability of their timing signals. The IMS G300 on the other hand, approaches the problem from the other direction by providing a fully programmable video timing generator, allowing it to interface to any monitor and avoid the need for more expensive multisync monitors.

2.6 INMOS and future directions for graphics products

It is clear from developments at the leading edge of graphics systems research that the graphics market will continue to demand higher resolutions, more functional integration, faster drawing speeds, better drawing algorithms, and yet all at suitably competitive prices.

This was the starting point for the design of INMOS' next device for the colour graphics marketplace, the IMS G300 Colour Video Controller mentioned earlier. This device integrates onto one chip not only the CLUT, but also a fully programmable video timing generator and intelligent memory interface to support video DRAMs. It offers a solution to the real-time problems of bit mapped graphics systems and interfaces to the

[1] IBM and PS/2 are registered trademarks of International Business Machines Corporation

host processor and frame buffer with the minimum of external circuitry.

As mentioned above, the IMS G300 encourages a graphics architecture where drawing algorithms are implemented in software, so allowing greater flexibility. With the IMS G300 one graphics board can be designed to drive a range of colour displays, with the change from one to another requiring just a re-programming of a maximum of nine registers in the G300.

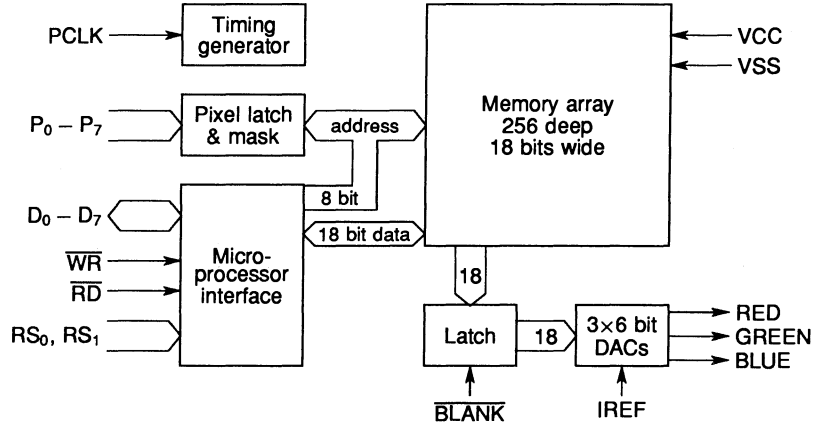
The support of dual-ported Video DRAMs is essential for high performance systems to allow maximum drawing bandwidth between processor and bitmap. The IMS G300 handles all bitmap to screen operations, including screen refresh, address generation (interlaced or non-interlaced) video synchronisation and data conversion. Whilst many video controllers have claimed to support VDRAMs effectively, the IMS G300 is the first to allow seamless mid-line updates of the screen, thus allowing the bitmap to be configured to any shape of display. Screen sizes are no longer restricted to multiples of the serial shift register length, so wastage of the bitmap is eliminated.

The IMS G300 also supports a number of other advanced features, including a look-up table bypass mode where the DACs can be addressed directly with 24-bit pixel data, providing a 'full-colour' mode of operation. It performs 4:1 pixel data multiplexing and on-chip clock multiplication by the use of a phase-locked loop, so that there are no video rate digital signals or clocks external to the chip. This minimises the need for high-speed digital design, all external components can be low cost CMOS or TTL; radiated emissions are kept low, giving easy compliance with Federal Communications Commission regulations, and design times and production costs are held to a minimum.

All these features make the IMS G300 an ideal component for the next generation of high performance colour graphics systems, and shows INMOS' ongoing commitment to this sector. With this and other devices under development INMOS intends to maintain its reputation as an innovative and quality supplier of VLSI devices and remain a dominant force in the growing graphics marketplace.

IMS G171
High performance CMOS colour look-up table

Designed to be compatible with IBM PS/2[1], VGA graphics systems



FEATURES

- Compatible with the RS170 video standard.
- Pixel rates up to 50MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun, composite blank.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V ±10% power supply.
- Low power dissipation, 880mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL package.

DESCRIPTION

The IMS G171 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters (designed to drive into a doubly terminated 75Ω line) and bi-directional microprocessor interface into a single 28 pin package.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G171 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

[1]IBM and PS/2 are registered trademarks of International Business Machines Corporation

3.1 Pin designations

3.1.1 Pixel interface

Signal	Pin	I/O	Signal name	Description
PCLK	13	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
$P_0 - P_7$	5–12	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the colour look-up table.
$\overline{BLANK}$	16	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.

3.1.2 Analogue interface

Signal	Pin	I/O	Signal name	Description
RED GREEN BLUE	1 2 3	O O O		These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. The number of current sources active is controlled by the 6 bit binary value applied to each DAC.
IREF	4	I	Reference current	The reference current drawn from VCC via the IREF pin determines the current sourced by each of the current sources in the DACs.

3.1.3 Microprocessor interface

Signal	Pin	I/O	Signal name	Description
$\overline{WR}$	25	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	15	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	26,27	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
$D_0 - D_7$	17–24	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G171 under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register selected and will go to a high impedance state.

3.1.4 Power supply

Signal	Pin	Signal name	Description
VCC	28	Power supply	Digital and analogue supply pads are bonded out to a single pin. The package contains a high-frequency decoupling capacitor between VCC and VSS to ensure a high quality analogue supply.
VSS	14	Ground	

3.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
				There is a single Address register within the IMS G171. This register can be accessed through either register select 0,0 or register select 1,1
0	0	8	Address (write mode)	Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to register 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the colour look-up table addressed and then increments the Address register. A read from register 0,0 is identical to a read from 1,1.
0	1	18	Colour Value	The Colour Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits ($D_0 - D_5$) are used. When a byte is read only the least significant six bits contain information — the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up table specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operation of the IMS G171 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs ($P_0 - P_7$). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed, via that interface.

3.2 Device description

The IMS G171 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 × 18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18 bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 50 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G171. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation and flashing objects. The pixel mask register is directly in the pixel stream, thus operations on the contents of the mask register should be synchronised to the pixel stream.

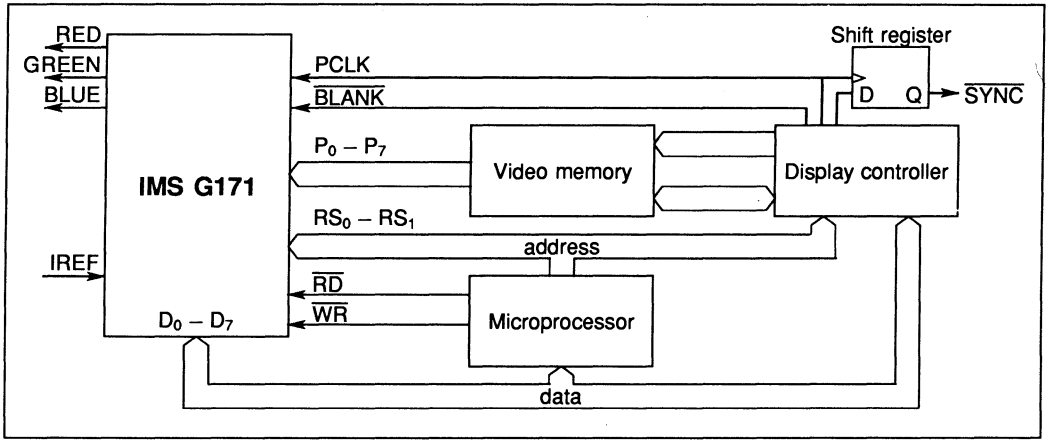


Figure 3.1 Typical iMS G171 application

3.2.1 Video path

Pixel address and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analogue outputs after three further rising edges of Pixel Clock (see figure 3.2).

3.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 8.88 mA when driving a doubly terminated 75Ω load . This corresponds to an effective DAC output loading ($R_{EFFECTIVE}$) of 37.5Ω.

The $\overline{\text{BLANK}}$ input to the IMS G171 acts on all three of the analogue outputs. When the $\overline{\text{BLANK}}$ input is low a binary zero is applied to the inputs of the DACs.

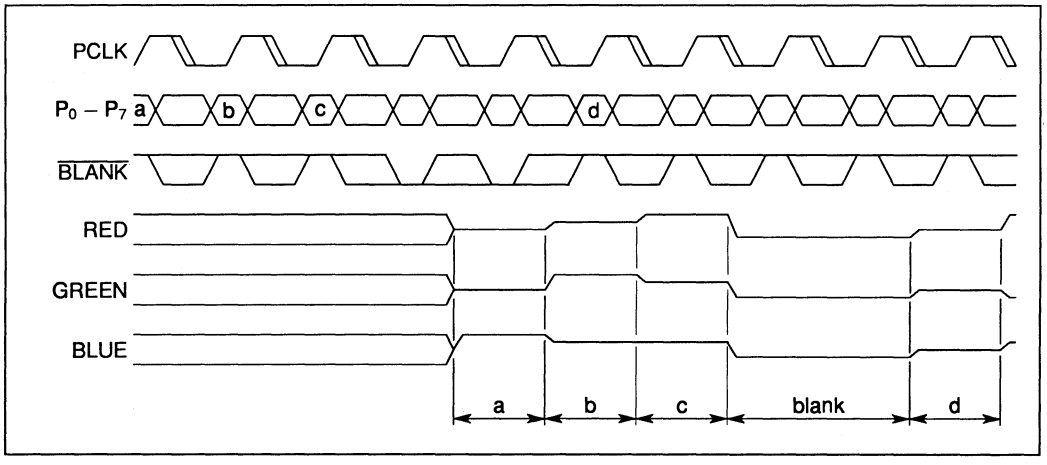


Figure 3.2

The expression for calculating IREF with various peak white voltage/output loading combinations is given below:

$$IREF = \frac{V_{PEAK\,WHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note that for all values of IREF and output loading:

$$V_{BLACKLEVEL} = 0$$

3.2.3 Microprocessor interface

Below are listed the three microprocessor interface registers within the IMS G171 and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address registers.

Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous look-up table access

Accesses to the Address and Colour Value registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G171. Internal logic synchronizes data transfers, between the look-up table and the Colour Value register, to the Pixel Clock in the period between the microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is independent of the Address and Colour Value registers. Operations on the Pixel Mask register are required to be synchronous to the pixel stream. The requirements for Pixel Mask register synchronisation are described in section 3.4.8.

3.3 Electrical specifications

3.3.1 Absolute maximum ratings *

Symbol	Parameter	Min.	Max.	Units	Notes
VCC	DC supply voltage		7.0	volts	
	Voltage on input and output pins	−1.0	VCC+0.5	volts	
TS	Storage temperature	−65	150	°C	
TA	Ambient temperature under bias	−40	85	°C	
PDmax	Power dissipation		1	W	
	Reference current	−15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

* Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VCC	Positive supply voltage	4.5	5.0	5.5	volts	2
VSS	Ground		0		volts	
VIH	Input logic '1' voltage	2.0		VCC+0.5	volts	
VIL	Input logic '0' voltage	−0.5		0.8	volts	3
TA	Ambient operating temperature	0		70	°C	4
IREF	Reference current	−7.0		−10	mA	5

Notes

1 All voltages are with respect to VSS unless otherwise specified.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

4 With a 400 linear ft/min transverse air flow.

5 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
ICC	Average power supply current		160	mA	4, IMS G171-50
ICC	Average power supply current		150	mA	4, IMS G171-35
VREF	Voltage at IREF input (pin 4)	VCC−3	VCC	volts	
IIN	Digital input current (any input)		±10	μA	5,6
IOZ	Off state digital output current		±50	μA	5,7
VOH	Output logic '1'	2.4		volts	IO = −5mA
VOL	Output logic '0'		0.4	volts	IO = 5mA

1 All voltages are with respect to VSS unless otherwise specified.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). ICC is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 VCC = max, VSS ≤ VIN ≤ VCC.

6 On digital inputs, pins 5–13, 15, 16, 25–27.

7 On digital input/output, pins 17–24.

3.3.3 DAC characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
	Resolution	6		bits	
VO(max)	Output voltage		1.5	volts	IO≤10mA
IO(max)	Output current		−21	mA	VO≤1V
	Full scale error		±5	%	4
	DAC to DAC correlation error		±2	%	5
	Integral linearity error		±0.5	LSB	6
	Rise time (10% to 90%)		8	ns	7
	Full scale settling time		20	ns	7,8,9, IMS G171-50
	Full scale settling time		28	ns	7,8,9, IMS G171-35
	Glitch energy		200	pVsec	7,9

Notes

1 All voltages are with respect to VSS unless otherwise specified.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

4 Full scale error from the value predicted by the design equations.

5 About the mid point of the distribution of the three DACs measured at full scale deflection.

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

7 Load = 37.5Ω + 30pF with IREF = −8.88mA.

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

3.3.4 AC test conditions

Input pulse levels	VSS to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure 3.3

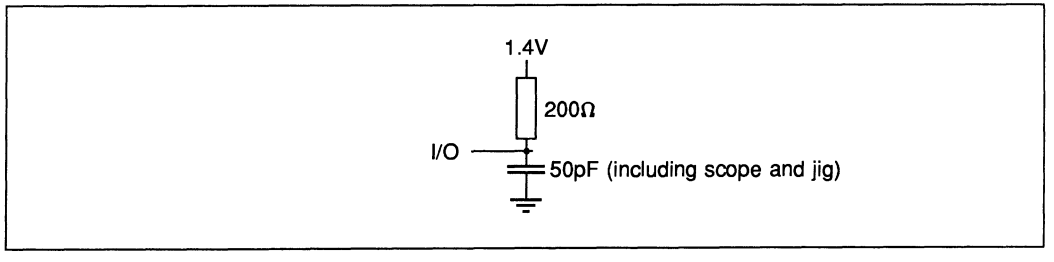


Figure 3.3 Digital output load

3.3.5 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable $D_0 - D_7$.

4 $\overline{BLANK} \leq$ VIL(max) to disable RED, GREEN and BLUE.

3.3.6 Video operation (figure 3.4)

Symbol	Parameter	All Max	35 MHz Min	50 MHz Min	Units	Notes
t_{CHCH}	PCLK period	10000	28	20	ns	
Δt_{CHCH}	PCLK jitter	±2.5			%	1
t_{CLCH}	PCLK width low	10000	9	6	ns	
t_{CHCL}	PCLK width high	10000	7	6	ns	
t_{PVCH}	Pixel address set-up time		5	4	ns	2
t_{CHPX}	Pixel address hold time		5	4	ns	2
t_{BVCH}	$\overline{BLANK}$ setup time		5	4	ns	
t_{CHBX}	$\overline{BLANK}$ hold time		5	4	ns	
t_{CHAV}	PCLK to valid DAC output	30	5	5	ns	3
Δt_{CHAV}	Differential output delay	2			ns	4
	Pixel clock transition time	50			ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (t_{CHCH}) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

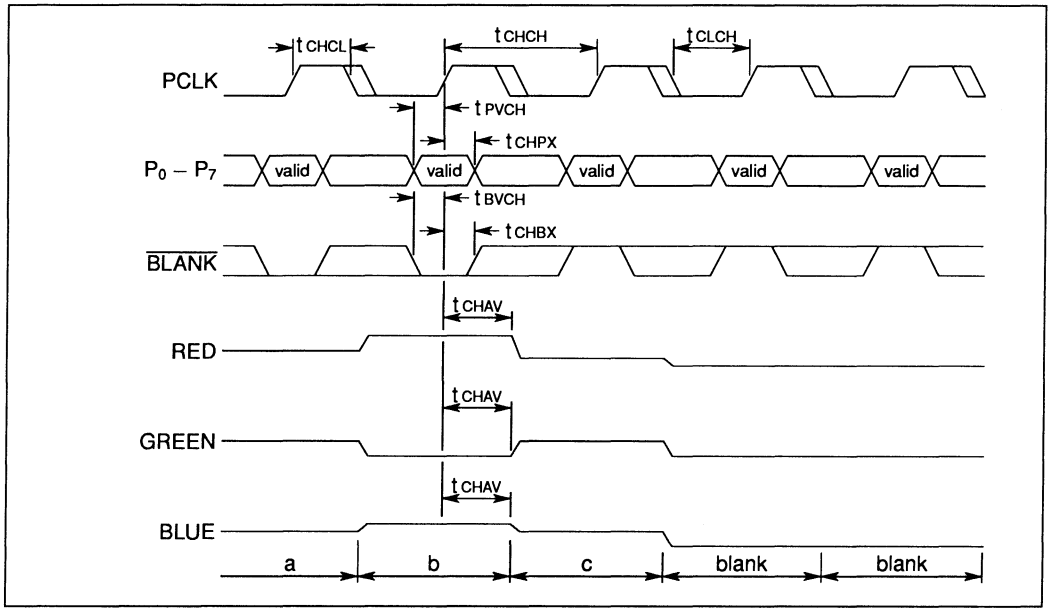


Figure 3.4 Video operation

3.3.7 Microprocessor interface operation (figures 3.5–3.13)

Symbol	Parameter	All Max	35 MHz Min	50 MHz Min	Units	Notes
t_{WLWH}	$\overline{WR}$ pulse width low		50	50	ns	
t_{RLRH}	$\overline{RD}$ pulse width low		50	50	ns	
t_{SVWL}	Register select setup time		15	10	ns	
t_{SVRL}	Register select setup time		15	10	ns	
t_{WLSX}	Register select hold time		15	10	ns	
t_{RLSX}	Register select hold time		15	10	ns	
t_{DVWH}	Write data setup time		15	10	ns	
t_{WHDX}	Write data hold time		15	10	ns	
t_{RLQX}	Output turn-on delay		5	5	ns	
t_{RLQV}	Read enable access time	40			ns	
t_{RHQX}	Output hold time		5	5	ns	
t_{RHQZ}	Output turn-off delay	20			ns	1
t_{WHWL1}	Successive write interval		$\mathcal{T}1$	$\mathcal{T}1$	ns	3
t_{WHRL1}	Write followed by read interval		$\mathcal{T}1$	$\mathcal{T}1$	ns	3
t_{RHRL1}	Successive read interval		$\mathcal{T}1$	$\mathcal{T}1$	ns	3
t_{RHWL1}	Read followed by write interval		$\mathcal{T}1$	$\mathcal{T}1$	ns	3
t_{WHWL2}	Write after colour write		$\mathcal{T}1$	$\mathcal{T}1$	ns	2,3
t_{WHRL2}	Read after colour write		$\mathcal{T}1$	$\mathcal{T}1$	ns	2,3
t_{RHRL2}	Read after colour read		$\mathcal{T}2$	$\mathcal{T}2$	ns	2,3
t_{RHWL2}	Write after colour read		$\mathcal{T}2$	$\mathcal{T}2$	ns	2,3
t_{WHRL3}	Read after read access write		$\mathcal{T}2$	$\mathcal{T}2$	ns	2,3
	Write/Read enable transition time	50			ns	

Notes

1 Measured ±200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 $\mathcal{T}1 = (3 \times t_{CHCH})$, $\mathcal{T}2 = (6 \times t_{CHCH})$.

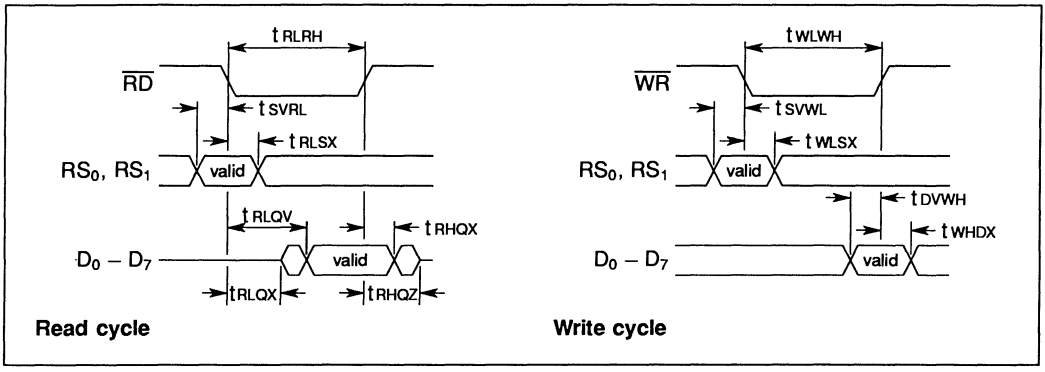


Figure 3.5 Basic read/write cycles

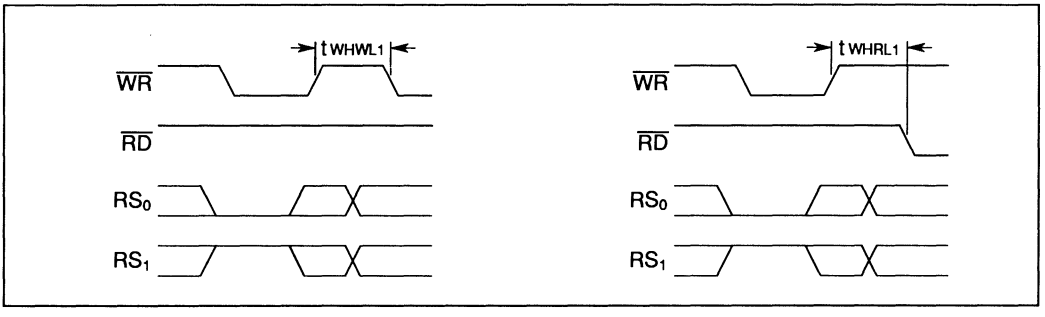


Figure 3.6 Write to pixel mask register followed by any access

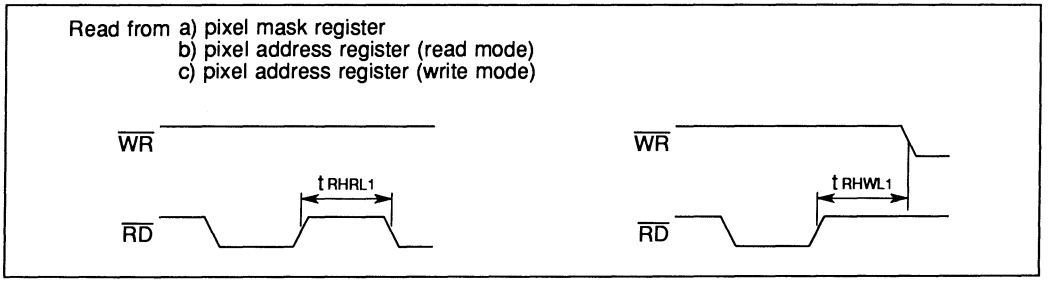


Figure 3.7 Read from register followed by any access

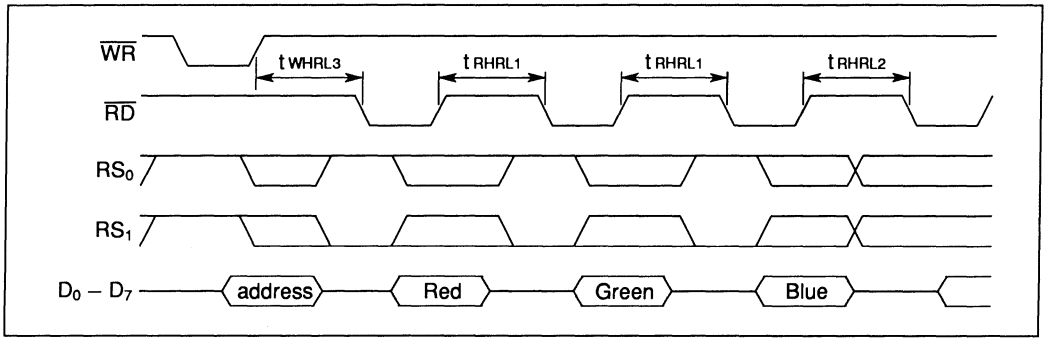


Figure 3.8 Colour value read followed by any read

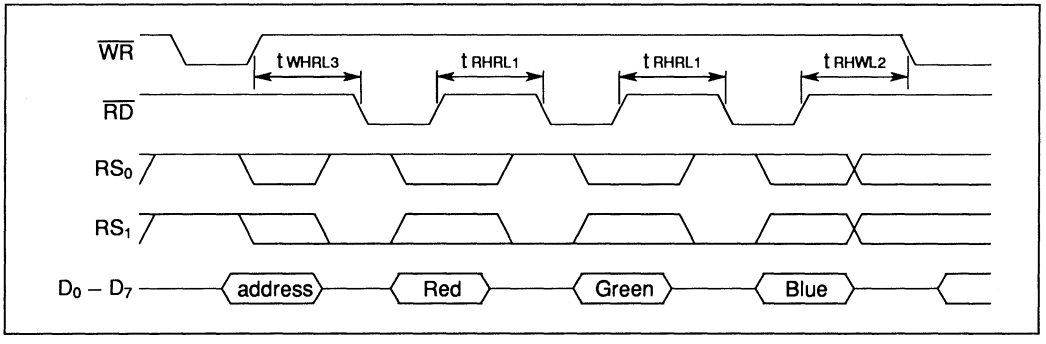


Figure 3.9 Colour value read followed by any write

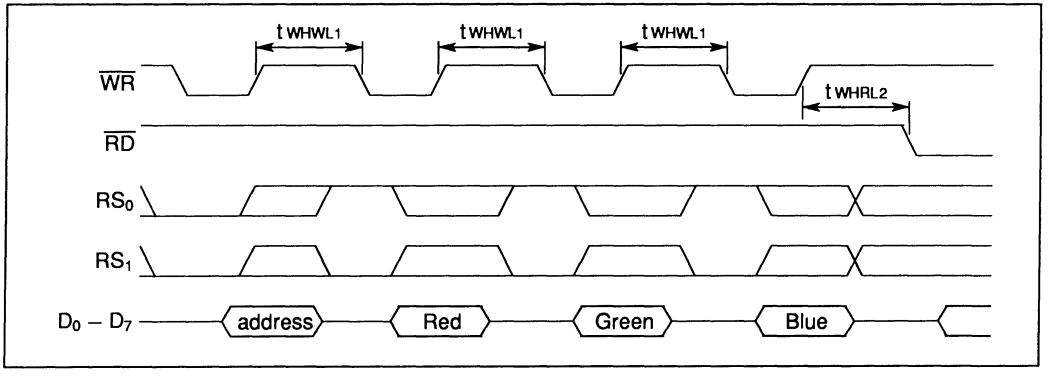


Figure 3.10 Colour value write followed by any read

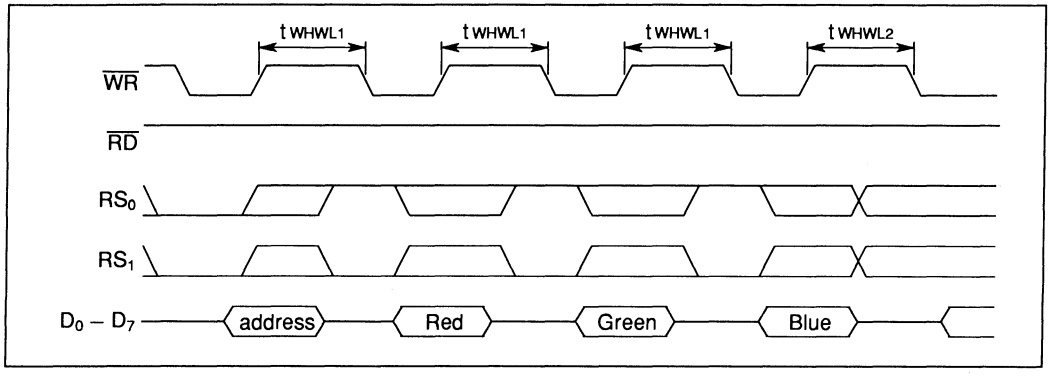


Figure 3.11 Colour value write followed by any write

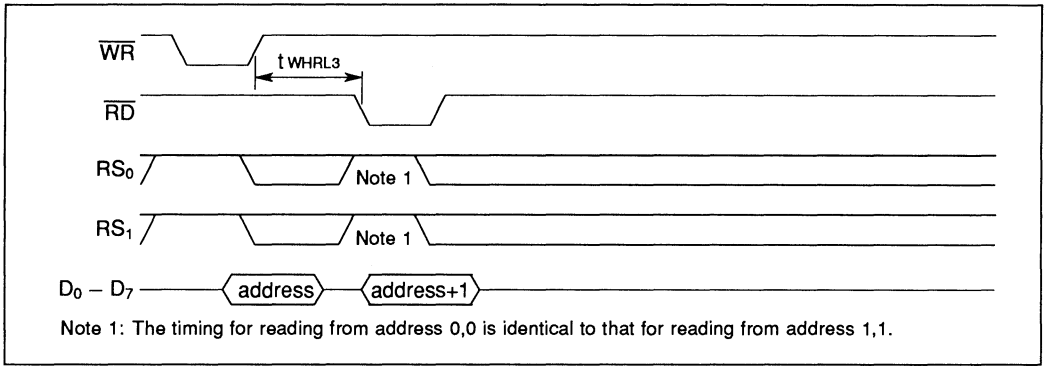


Figure 3.12 Write and read back address register (read mode)

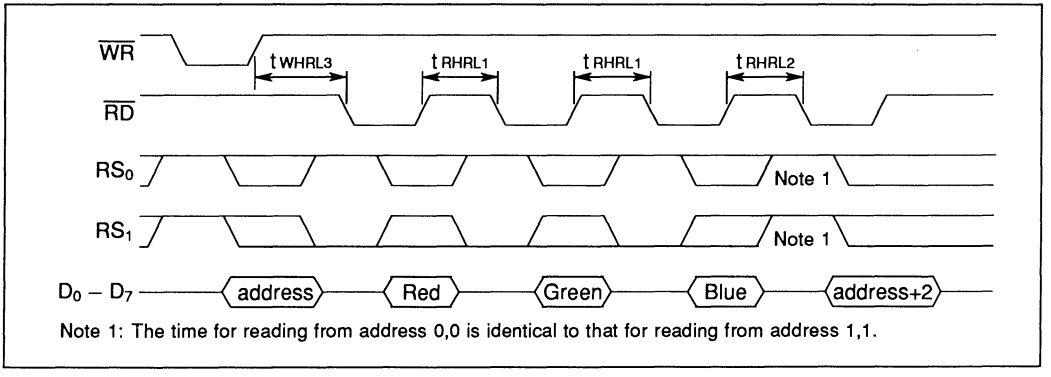


Figure 3.13 Read colour value then the address register (read mode)

3.4 Designing with the IMS G171

3.4.1 Board layout — general

The IMS G171 is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G171. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

3.4.2 Power supply decoupling

To supply the transient currents required by the IMS G171 the impedance in the decoupling path between VCC and VSS should be a 0.1 μF high frequency capacitor in parallel with a larger tantalum capacitor with a value between 22 μF and 47 μF. An inductance may be added in series with the positive supply to form a low pass filter and so further improve the power supply local to the IMS G171.

The combination of series impedance in the ground supply to the IMS G171 and transients in the current drawn by the IMS G171 will appear as differences in the VSS voltages to the IMS G171 and to the digital devices driving it. To minimise this differential ground noise the impedance in the ground supply between the IMS G171 and the digital devices driving it should be minimised.

3.4.3 Analogue output — line driving

The DACs in the IMS G171 are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G171 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good signal fidelity, RF techniques should be observed. The PCB trace connecting the IMS G171 to the offboard connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect from the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus, a double terminated DAC output will rise faster than any singly terminated output.

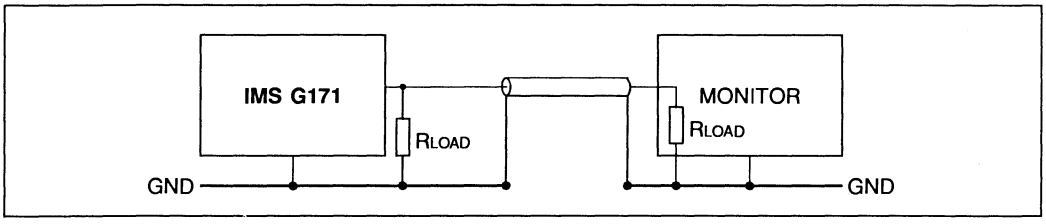


Figure 3.14 Double termination

Buffered signal

If the IMS G171 is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

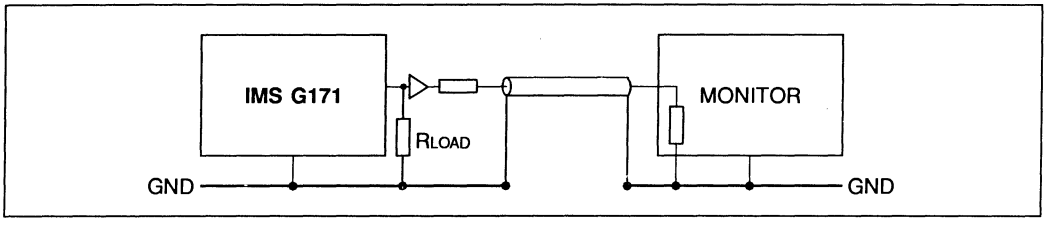


Figure 3.15 Buffered signal

3.4.4 Analogue output — protection

CMOS devices are susceptible to damage from from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G171 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G171 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection devices (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figure 3.17).

3.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G171 behave like low impedance transmission lines driven from a low impedance source and terminated with a high impedance. In accordance with transmission line principles signal transitions will be reflected from the high impedance input to the IMS G171. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a value around 100Ω will be required. Because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

3.4.6 Current reference — design

To ensure that the output current of the DACs is predictable and stable with temperature variations an active current reference is recommended. Figure 3.16 shows four designs of current reference.

Figure 3.16d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of VCC.

Figures 3.16a–c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuit 3.16b and 3.16c the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 3.16c).

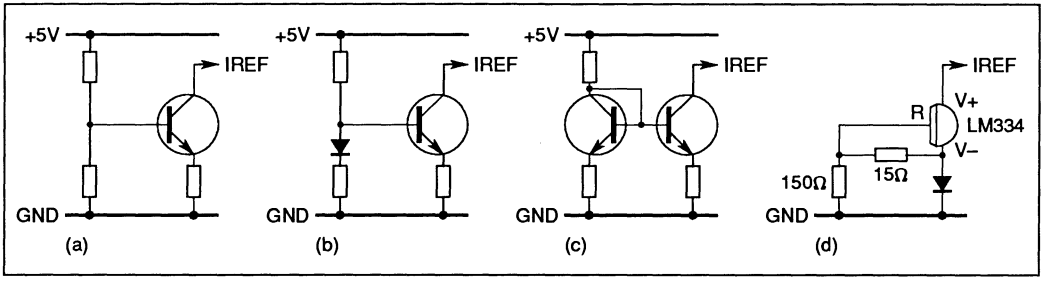


Figure 3.16

3.4.7 Current reference — decoupling

The DACs in the IMS G171 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capacitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VCC. This will enable the current reference to track both low and high frequency variations in the supply.

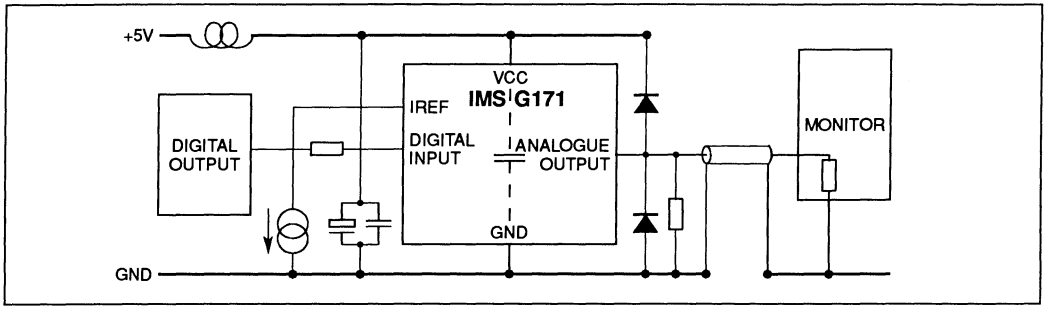


Figure 3.17 Circuit incorporating suggested design features

3.4.8 Pixel Mask register synchronisation

Each pixel address used as an address into the colour look-up table is masked by the Pixel Mask register.If the contents of the Pixel Mask register are modified asynchronously to PCLK there is a possibilty that the data held within the Pixel Mask register will change at such an instant as to corrupt the address applied to the look-up table as it is being latched.

If the Pixel Mask register is only initialised once on power up the synchronisation precautions described below need not be taken, it is sufficient simply to ensure that the colour look-up table is initialised after the Pixel Mask register. The synchronous properties of the Pixel Mask register in no way affect the ability to update the look-up table asynchronously,

If the Pixel Mask register is to be updated on a regular basis, asynchronously to PCLK, corruption of the look-up table contents will inevitably occur. To prevent such corruption the update of the mask register should occur at a time which ensures that the internal pixel mask value is not changing between values as it is being sampled. This requires that certain timing constraints synchronising $\overline{WR}$ to PCLK are met (see table 3.1).

The circuit given in figure 3.18 should be suitable for systems with pixel rates up to 35 MHz. The synchronisation circuity required for systems working above 35 MHz may be more complex.

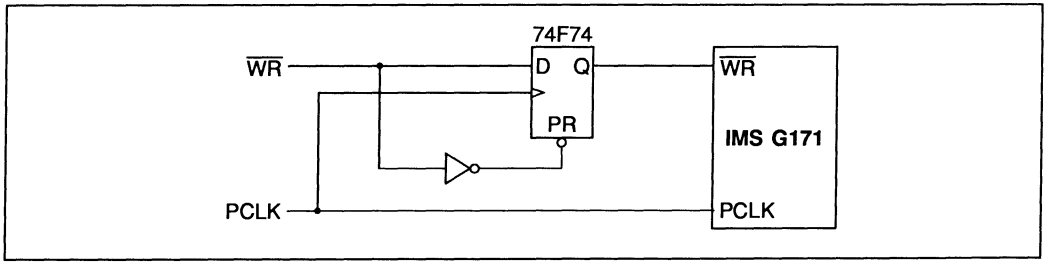


Figure 3.18

Symbol	Parameter	All	35 MHz	50 MHz	Units	Notes
		Max	Min	Min		
t_{WLCH}	$\overline{WR}$ illegal transition window	12	1	1	ns	1,2
t_{DVWL}	Data setup time		15	15	ns	2
t_{WHDX}	Data hold time		15	10	ns	

Table 3.1 Pixel mask register synchronisation.

Notes

1 $\overline{WR}$ should not change from high to low within the window delimited by the minimum and maximum times specified.

2 This parameter need only be observed if modifications of the value held in the Pixel Mask register are required to occur synchronously to the pixel stream.

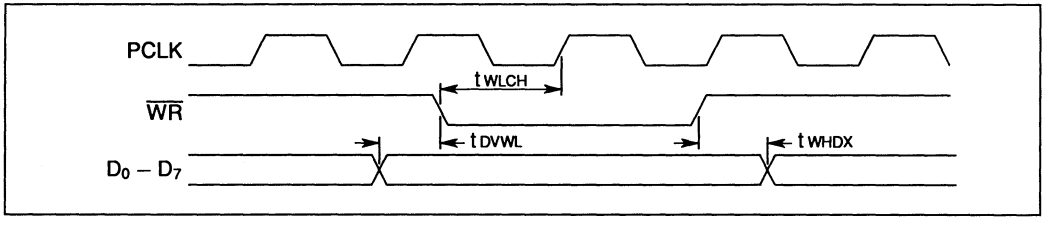


Figure 3.19 Pixel mask register synchronisation.

3.5 Package specifications

3.5.1 28 pin dual-in-line package

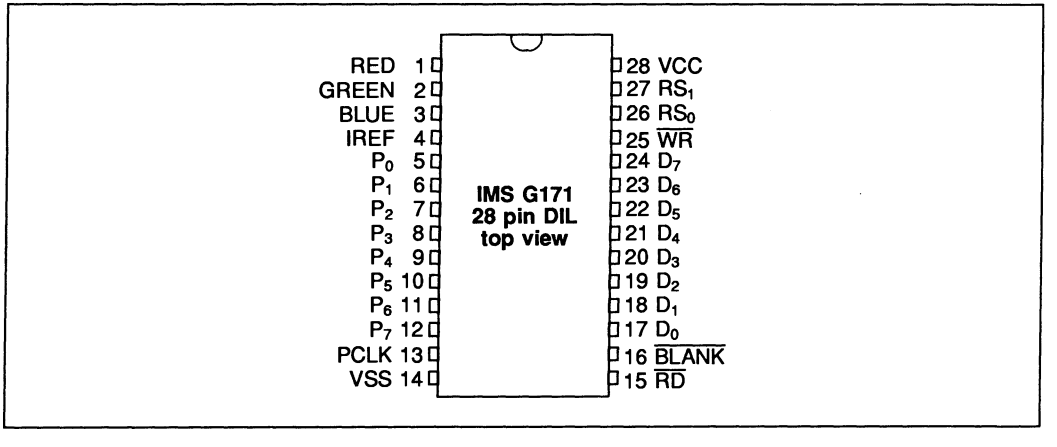


Figure 3.20 IMS G171 28 pin dual-in-line package pinout

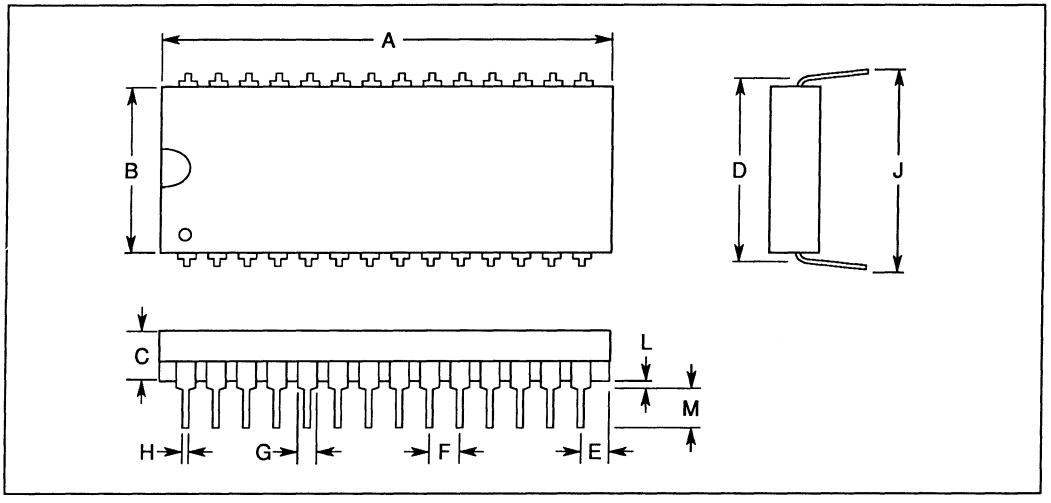


Figure 3.21 28 pin plastic dual-in-line package dimensions

	Millimetres		Inches		
DIM	NOM	TOL	NOM	TOL	Notes
A	36.830	±0.254	1.450	±0.010	
B	13.970	±0.254	0.550	±0.010	
C	4.445	±0.635	0.175	±0.025	
D	15.240	±0.076	0.600	±0.003	
E	1.905		0.075		
F	2.540		0.100		
G	1.397	±0.254	0.055	±0.010	
H	0.457		0.018		
J	16.256	±0.508	0.640	±0.020	
L	0.508		0.020		Minimum
M	3.429		0.135		Maximum

Table 3.2 28 pin plastic dual-in-line package dimensions

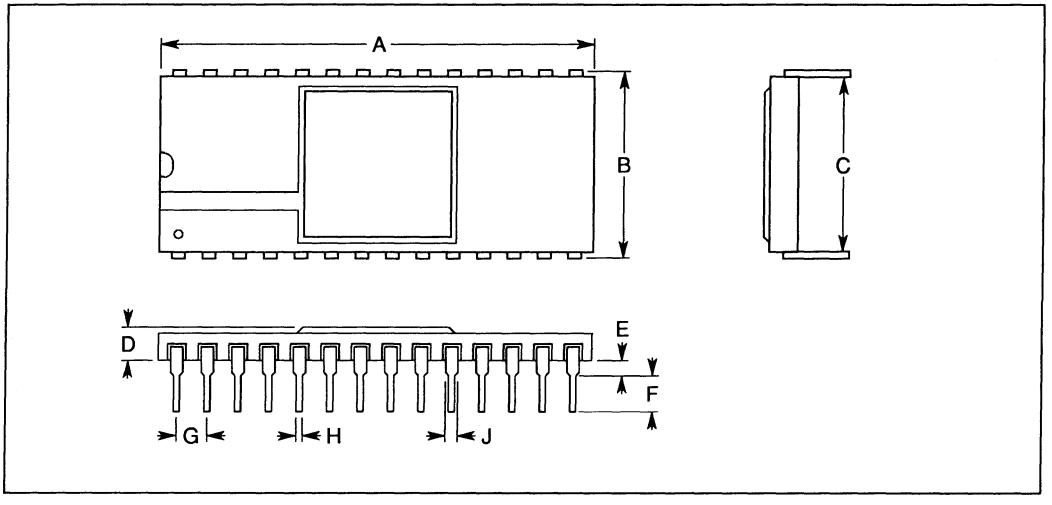


Figure 3.22 28 pin ceramic dual-in-line package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	35.560	±0.356	1.400	±0.014	
B	15.494	±0.254	0.610	±0.010	
C	14.681	+0.813	0.578	+0.032	
D	2.466	±0.229	0.097	±0.009	
E	1.270	±0.254	0.051	±0.010	
F	3.048		0.120		Minimum
G	2.540		0.100		
H	0.457	±0.051	0.018	±0.002	
J	1.016	+0.508	0.040	+0.020	

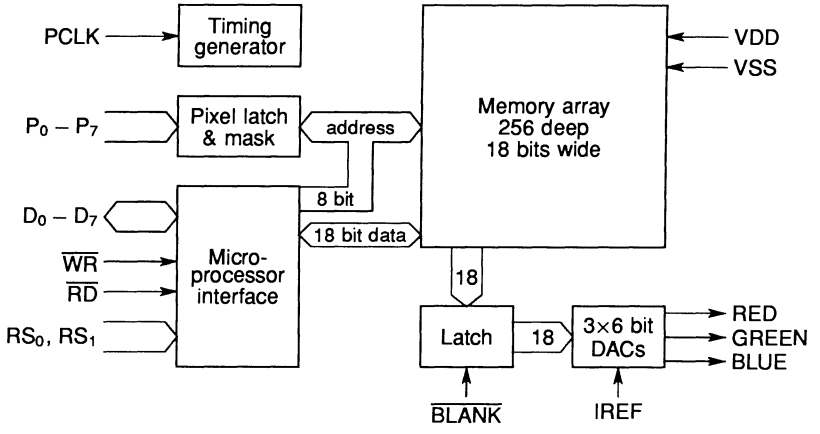
Table 3.3 28 pin ceramic dual-in-line package dimensions

3.5.2 Ordering information

Device	Clock rate	Package	Part number
IMS G171	35 MHz	Plastic DIP	IMSG171P-35
IMS G171	35 MHz	Ceramic DIP	IMSG171S-35
IMS G171	50 MHz	Plastic DIP	IMSG171P-50
IMS G171	50 MHz	Ceramic DIP	IMSG171S-50

IMS G176
High performance CMOS colour look-up table

Designed to be compatible with IBM PS/2[1], VGA graphics systems



FEATURES

- Compatible with the RS170 video standard.
- Pixel rates up to 65MHz.
- 256K possible colours.
- Single monolithic, high performance CMOS.
- Pixel word mask.
- RGB analogue output, 6 bit DAC per gun.
- Composite blank on all three channels.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- Up to 8 bits per pixel.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Single +5V ±10% power supply.
- Low power dissipation, 950mW max. at maximum pixel rate.
- Standard 600 mil 28 pin DIL or 32 pin Plastic LCC.
- Pin compatible with IMS G171.

DESCRIPTION

The IMS G176 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 28 pin DIL or 32 pin PLCC package.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite blank signals can be generated on all three outputs.

Capable of displaying 256 colours from a total of 262,144 colours, the IMS G176 replaces TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

[1]IBM and PS/2 are registered trademarks of International Business Machines Corporation

4.1 Pin designations

4.1.1 Pixel interface

Signal	Pin number		I/O	Signal name	Description
	DIL	PLCC			
PCLK	13	14	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address and Blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
$P_0 - P_7$	5–12	6–13	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel mask register and then used as the address into the colour look-up table.
$\overline{\text{BLANK}}$	16	20	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.

4.1.2 Analogue interface

Signal	Pin number		I/O	Signal name	Description
	DIL	PLCC			
RED GREEN BLUE	1 2 3	2 3 4	O O O		These signals are the outputs of the 6 bit DACs. Each DAC is composed of 63 current sources whose outputs are summed. The number of current sources active is controlled by the 6 bit binary value applied.
IREF	4	5	I	Reference current	The reference current drawn from VDD (or AVDD) via the IREF pin determines the current sourced by each of the current sources in the DACs.

4.1.3 Microprocessor interface

Signal	Pin number DIL	Pin number PLCC	I/O	Signal name	Description
$\overline{WR}$	25	29	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	15	19	I	Read enable	Most of the operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	26,27	30,31	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$); they specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
$D_0 - D_7$	17–24	21–28	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G176 under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register addressed and will go to a high impedance state.

4.1.4 Power supply

Signal	Pin number DIL	Pin number PLCC	Signal name	Description
VDD	28		Power supply	Digital and analogue supply pads are bonded out to a single pin on the DIL package. The package contains a high-frequency decoupling capacitor between VDD and VSS to ensure a high quality analogue supply.
VDD		17	Digital supply	Digital and analogue supply pads are bonded out separately on the PLCC package to give highest possible noise immunity. Due to package size limitations the decoupling capacitor capacitor must be provided externally (see section on 'Power supply decoupling')
AVDD		32	Analogue supply	
VSS	14	16	Ground	

4.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
				There is a single Address register within the IMS G176. This register can be accessed through either register select 0,0 or 1,1
0	0	8	Address (write mode)	Writing a value to register 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to register 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the look-up table addressed and then increments the Address register. A read from register 0,0 is functionally equivalent to a read from 1,1.
0	1	18	Colour Value	The Colour Value register is internally an 18 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this register address. When a byte is written only the least significant six bits ($D_0 - D_5$) are used. When a byte is read only the least significant six bits contain information — the most significant two bits being set to zero. The sequence of data transfer is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operations of the IMS G176 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs ($P_0 - P_7$). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, while a zero sets that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed via that interface.

4.2 Device description

The IMS G176 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 × 18 bit words, three 6 bit high speed DACs, a microprocessor interface and a pixel word mask.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18 bit data word being output from the table. This data is partitioned as three fields of 6 bits, each field being applied to the inputs of a 6 bit DAC.

Pixel rates of up to 65 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G176. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation, overlays and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

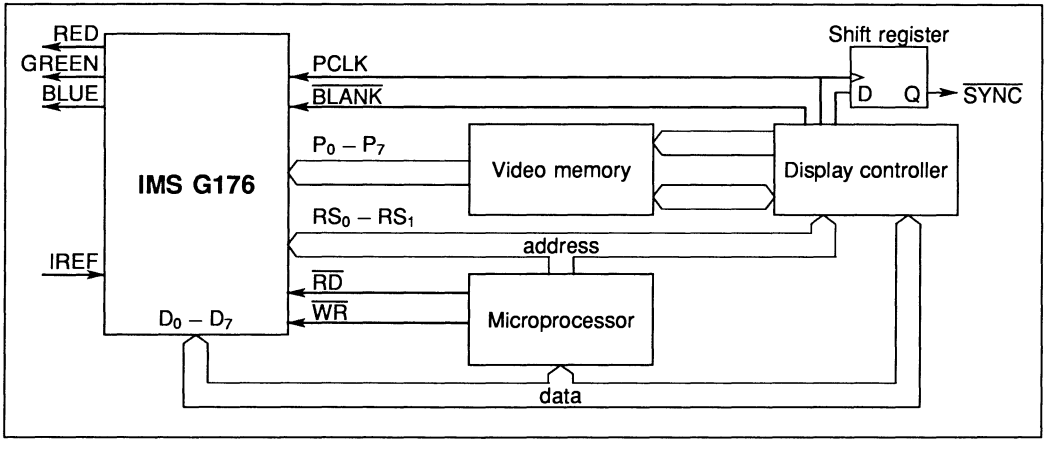


Figure 4.1 Typical IMS G176 application

4.2.1 Video path

$P_0 - P_7$ and $\overline{\text{BLANK}}$ inputs are sampled on the rising edge of Pixel Clock, their effect appears at the analogue outputs after three further rising edges of Pixel Clock (see figure 4.2).

4.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 0.7 volt peak white amplitude with an IREF of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The $\overline{\text{BLANK}}$ input to the IMS G176 acts on all three of the analogue outputs. When the $\overline{\text{BLANK}}$ input is low a binary zero is applied to the inputs of the DACs.

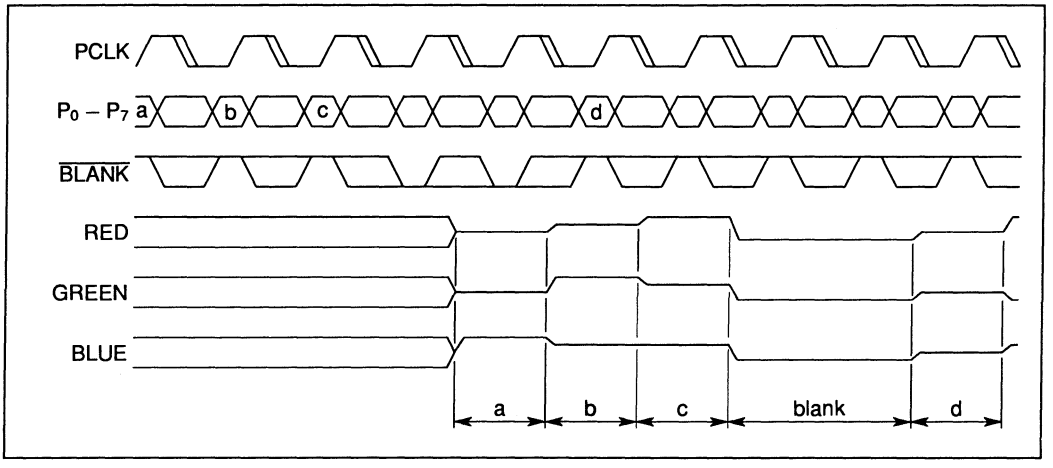


Figure 4.2

The expression for calculating IREF with various peak white voltage/output loading combinations is given below:

$$IREF = \frac{V_{PEAK\,WHITE}}{2.058 \times R_{EFFECTIVE}}$$

Note that for all values of IREF and output loading:

$$V_{BLACKLEVEL} = 0$$

4.2.3 Microprocessor interface

Below are listed the three microprocessor interface registers within the IMS G176 and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address register.

Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous microprocessor interface access

Accesses to all registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G176. Data transfers between the look-up table and the Colour Value register and modifications to the Pixel Mask register are synchronised to the Pixel Clock by internal logic. This is done in the period between microprocessor accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers or modifications to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is completely independent of the Address and Colour Value registers.

4.3 Electrical specifications

4.3.1 Absolute maximum ratings *

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	VSS−1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	−65	150	°C	
TA	Temperature under bias	−40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	−15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

Notes

* Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

4.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VDD	Positive supply voltage	4.5	5.0	5.5	V	2,3
VSS	Ground		0		V	
VIH	Input logic '1' voltage	2.0		VDD+0.5	V	3
VIL	Input logic '0' voltage	−0.5		0.8	V	4
TA	Ambient operating temperature	0		70	°C	5
IREF	Reference current	−7.0		−10	mA	6

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 These voltage ranges apply equally for AVDD and VDD when using the PLCC packaged device.

4 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (t_{CHCH}) or 10ns, whichever is the smaller value.

5 With a 400 linear ft/min transverse air flow.

6 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
IDD	Average power supply current		190	mA	4, IMS G176-65
IDD	Average power supply current		160	mA	4, IMS G176-50
IDD	Average power supply current		155	mA	4, IMS G176-40
VREF	Voltage at IREF input (pin 4)	VDD−3	VDD	V	5
IIN	Digital input current (any input)		±10	μA	6,7
IOZ	Off state digital output current		±50	μA	6,8
VOH	Output logic '1'	2.4		V	IO = −5mA
VOL	Output logic '0'		0.4	V	IO = 5mA

1 All voltages are with respect to VSS unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). IDD is dependent on digital loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 These voltages apply equally for AVDD and VDD when using the PLCC packaged device.

6 VDD = max, VSS ≤ VIN ≤ VDD.

7 On digital inputs, pins 5–13, 15, 16, 25–27 (pins 6–14, 19, 20, 29–31 on PLCC package).

8 On digital input/output, pins 17–24 (pins 21–28 on PLCC package).

4.3.3 DAC characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes (1,2,3)
	Resolution	6			bits	
VO(max)	Output voltage			1.5	V	IO≤10mA
IO(max)	Output current			−21	mA	VO≤1V
	Full scale error			±5	%	4
	DAC to DAC correlation error			±2	%	5
	Integral linearity error			±0.5	LSB	6
	Rise time (10% to 90%)			6	ns	7, IMS G176-65
	Rise time (10% to 90%)			8	ns	7, IMS G176-40/50
	Full scale settling time			15.3	ns	7,8,9, IMS G176-65
	Full scale settling time			20	ns	7,8,9, IMS G176-50
	Full scale settling time			25	ns	7,8,9, IMS G176-40
	Glitch energy		120		pVsec	7,9

Notes

1 All voltages are with respect to VSS unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

4 Full scale error from the value predicted by the design equations.

5 About the mid point of the distribution of the three DACs measured at full scale deflection.

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

7 Load = 37.5Ω + 30pF with IREF = −8.88mA.

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

4.3.4 AC test conditions

Input pulse levels	VSS to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure 4.3

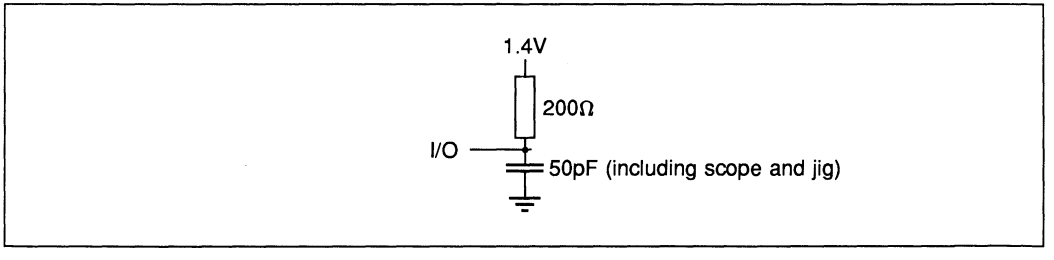


Figure 4.3 Digital output load

4.3.5 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable $D_0 - D_7$.

4 $\overline{BLANK} \leq$ VIL(max) to disable RED, GREEN and BLUE.

4.3.6 Video operation (figure 4.4)

Symbol	Parameter	All Max	40 MHz Min	50 MHz Min	65 MHz Min	Units	Notes
t_{CHCH}	PCLK period	10000	25	20	15.3	ns	
Δt_{CHCH}	PCLK jitter	±2.5				%	1
t_{CLCH}	PCLK width low	10000	9	6	5	ns	
t_{CHCL}	PCLK width high	10000	7	6	5	ns	
t_{PVCH}	Pixel address set-up time		5	4	3	ns	2
t_{CHPX}	Pixel address hold time		5	4	3	ns	2
t_{BVCH}	$\overline{BLANK}$ setup time		5	4	3	ns	
t_{CHBX}	$\overline{BLANK}$ hold time		5	4	3	ns	
t_{CHAV}	PCLK to valid DAC output	30	5	5	5	ns	3
Δt_{CHAV}	Differential output delay	2				ns	4
	Pixel clock transition time	50				ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (t_{CHCH}) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

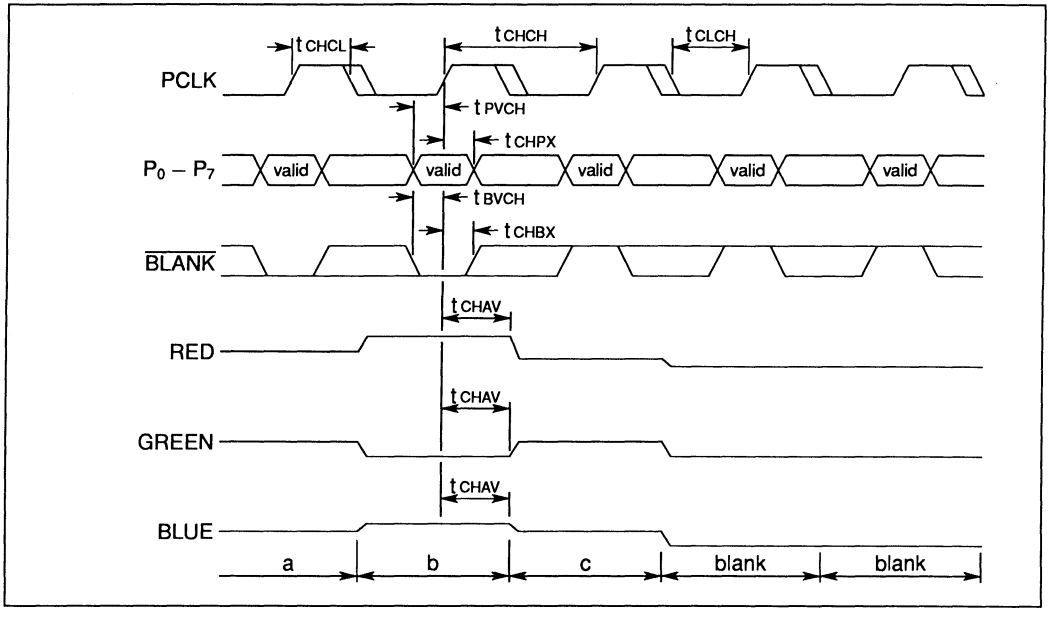


Figure 4.4 Video operation

4.3.7 Microprocessor interface operation

Symbol	Parameter	All Max	40 MHz Min	50 MHz Min	65 MHz Min	Units	Notes
t_{WLWH}	$\overline{WR}$ pulse width low		50	50	50	ns	
t_{RLRH}	$\overline{RD}$ pulse width low		50	50	50	ns	
t_{SVWL}	Register select setup time		15	10	10	ns	
t_{SVRL}	Register select setup time		15	10	10	ns	
t_{WLSX}	Register select hold time		15	10	10	ns	
t_{RLSX}	Register select hold time		15	10	10	ns	
t_{DVWH}	Write data setup time		15	10	10	ns	
t_{WHDX}	Write data hold time		15	10	10	ns	
t_{RLQX}	Output turn-on delay		5	5	5	ns	
t_{RLQV}	Read enable access time	40				ns	
t_{RHQX}	Output hold time		5	5	5	ns	
t_{RHQZ}	Output turn-off delay	20				ns	1
t_{WHWL1}	Successive write interval						
t_{WHRL1}	Write followed by read interval						
t_{RHRL1}	Successive read interval						
t_{RHWL1}	Read followed by write interval		$4 \times t_{CHCH} + 30ns$			ns	2
t_{WHWL2}	Write after colour write						
t_{WHRL2}	Read after colour write						
t_{RHWL2}	Write after colour read						
t_{RHRL2}	Read after colour read		$6 \times t_{CHCH} + 40ns$			ns	2
t_{WHRL3}	Read after read address write						
t_{CYC}	Write/Read cycle time		$6 \times t_{CHCH} + 40ns$			ns	2,3
	Write/Read enable transition time	50				ns	

Notes

1 Measured ±200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the microprocessor port are internally synchronised to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the microprocessor port being specified in terms of pixel clock periods.

In the case of the IMS G176 the minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is $6 \times t_{CHCH} + 40ns$.

For example, in the case of a 25MHz system the pixel clock period (t_{CHCH}) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

$$6 \times 40ns + 40ns = 280ns$$

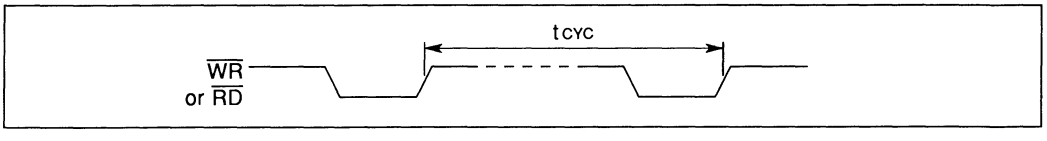


Figure 4.5 Write/Read cycle time

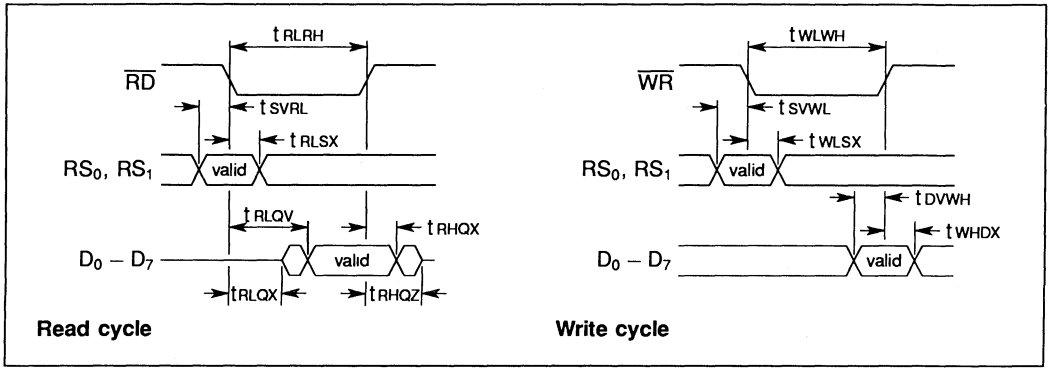


Figure 4.6 Basic read/write cycles

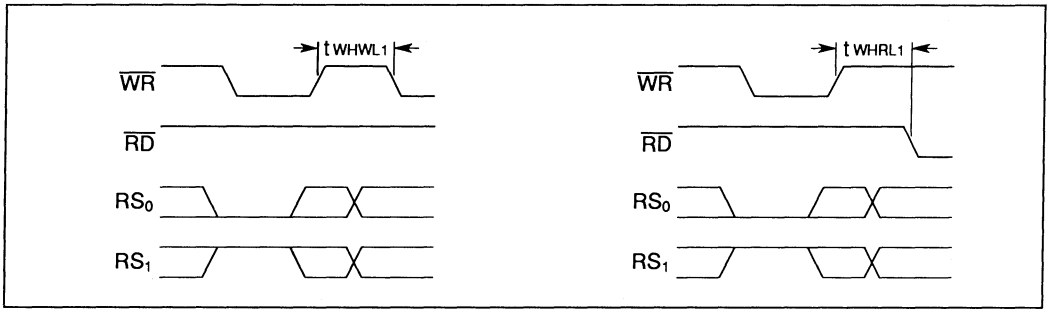


Figure 4.7 Write to pixel mask register followed by any access

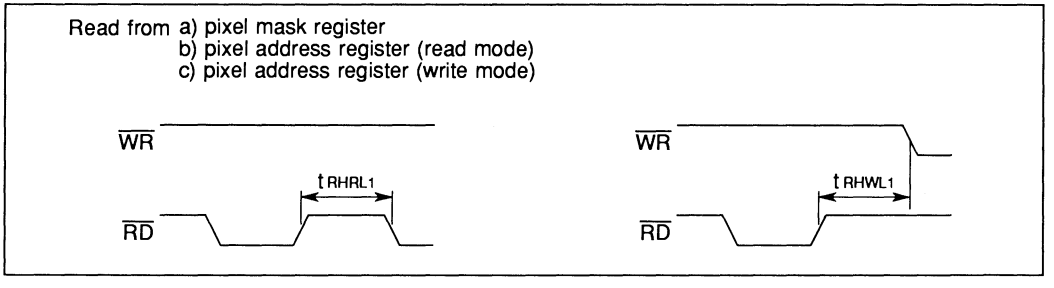


Figure 4.8 Read from register followed by any access

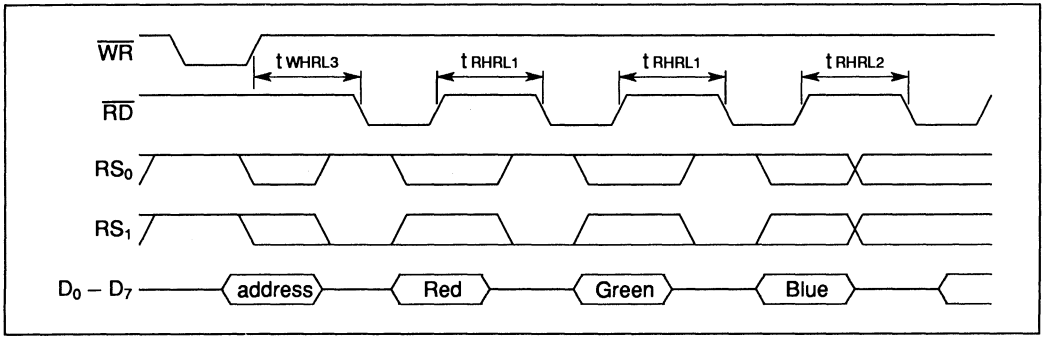


Figure 4.9 Colour value read followed by any read

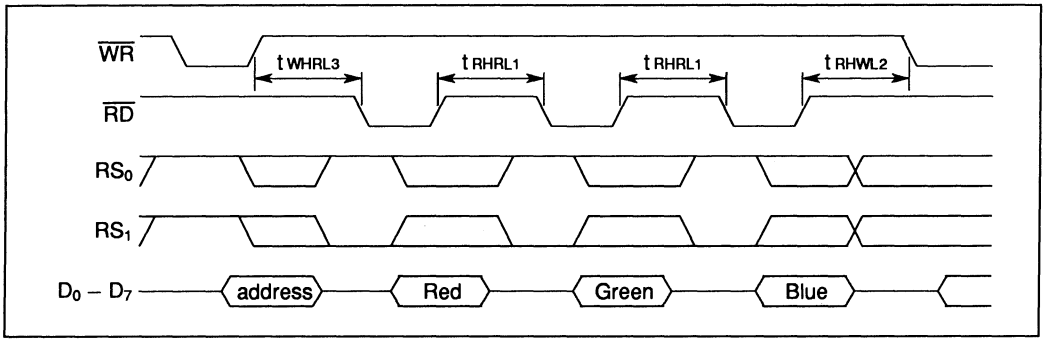


Figure 4.10 Colour value read followed by any write

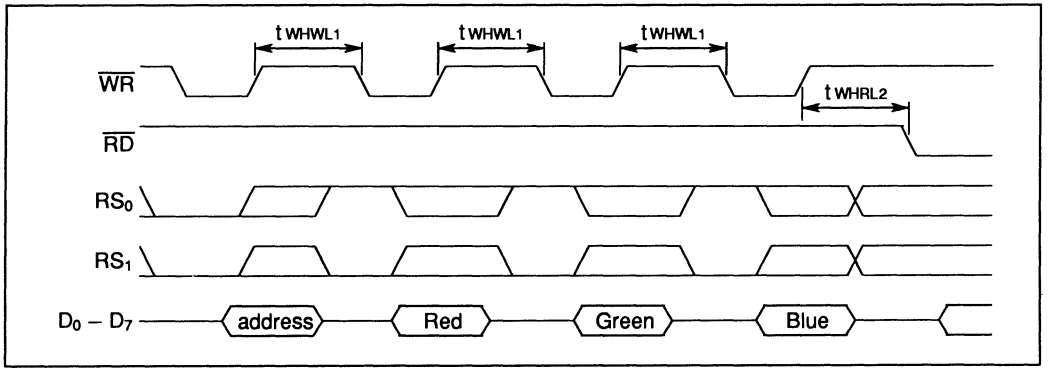


Figure 4.11 Colour value write followed by any read

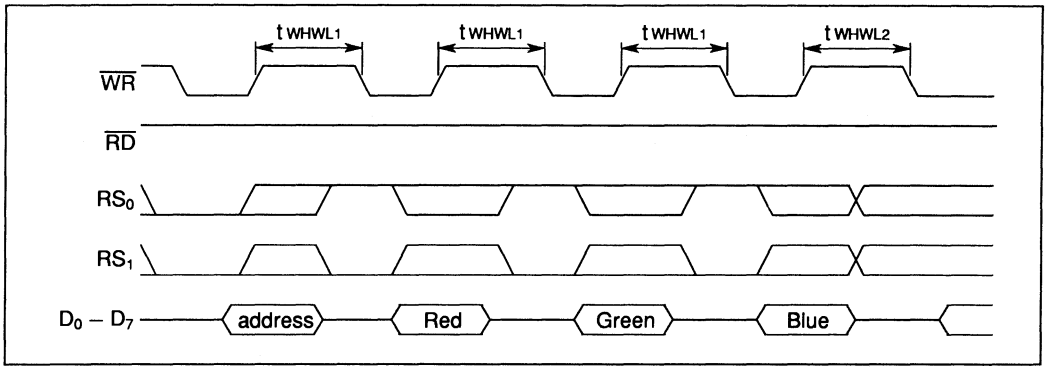


Figure 4.12 Colour value write followed by any write

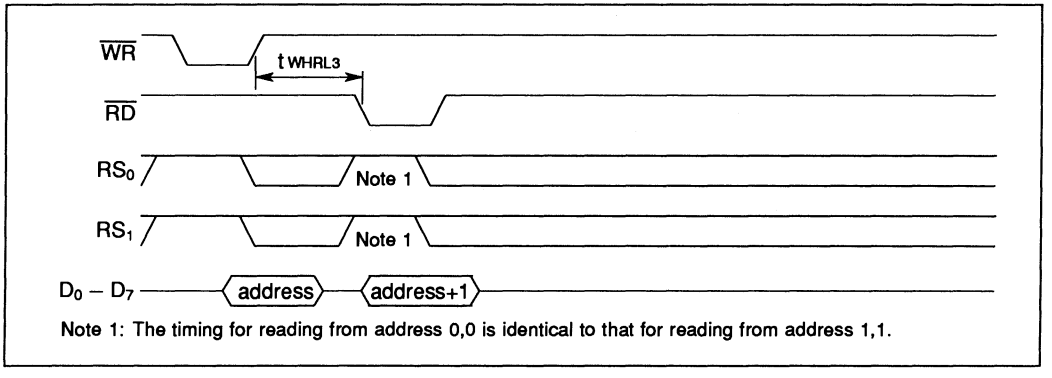


Figure 4.13 Write and read back address register (read mode)

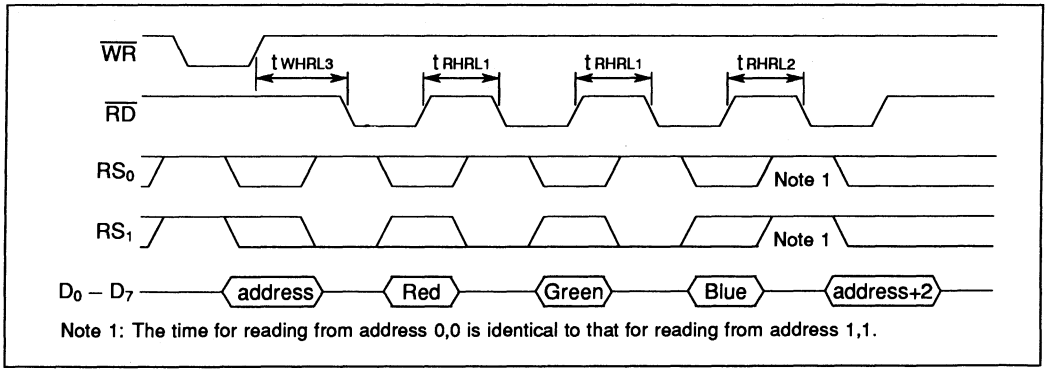


Figure 4.14 Read colour value then the address register (read mode)

4.4 Designing with the IMS G176

4.4.1 Board layout — general

The IMS G176 is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G176. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

4.4.2 Power supply decoupling

The DACs in the IMS G176 are referenced to the positive power supply, so are fairly insensitive to ground supply noise. To ensure that switching noise generated by the digital sections of the IMS G176 is not transmitted to the DAC circuitry, independent analogue and digital +5V supplies are provided on-chip.

When packaged in a PLCC, the analogue and digital supplies are bonded out to separate pins. It is recommended that a high frequency capacitor of around 100nF (preferably a chip capacitor) should be placed as close as possible to the package between VDD and VSS. A large tantalum capacitor (between 22μF and 47μF) should also be placed in parallel with this high-frequency capacitor. AVDD should be connected to the positive power plane by the smallest impedance path possible, e.g. a via right next to a pin (see figure 4.18).

In the DIL package both the analogue and digital supplies are bonded out to a single pin (VDD). Again it is recommended that a high-frequency 100nF capacitor in parallel with a large tantalum capacitor are provided externally to ensure a high quality analogue supply (see figure 4.19).

An inductor may also be added in series with the positive supply to form a low-pass filter and so further improve the power supply local to the IMS G176.

4.4.3 Analogue output — line driving

The DACs in the IMS G176 are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G176 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good signal fidelity, RF techniques should be observed. The PCB trace connecting the IMS G176 to the offboard connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus, a double terminated DAC output will rise faster than any singly terminated output.

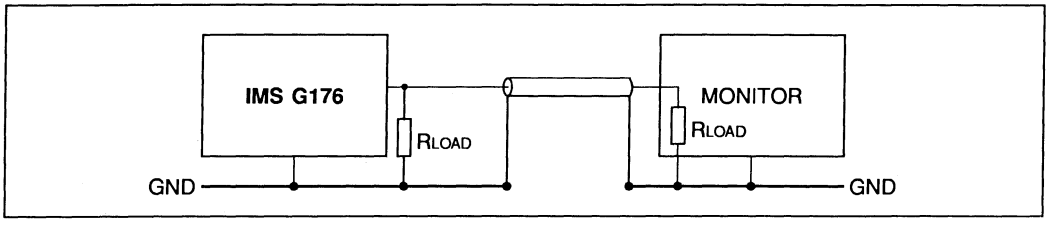


Figure 4.15 Double termination

Buffered signal

If the IMS G176 is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

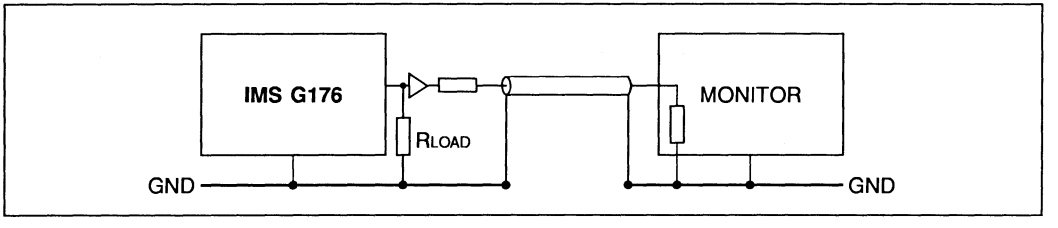


Figure 4.16 Buffered signal

4.4.4 Analogue output — protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G176 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G176 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection devices (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figures 4.18 and 4.19).

4.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G176 and the input to the IMS G176 have a low impedance source and are terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of the IMS G176. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing, and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimise reflections, but generally a value around 100Ω will be required. because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

4.4.6 Current reference — design

To ensure that the output current of the DACs is predictable and stable with temperature variations, an active current reference is recommended. Figure 4.17 shows four designs of current reference.

Figure 4.17d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 4.17a–c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuits 4.17b and 4.17c the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 4.17c).

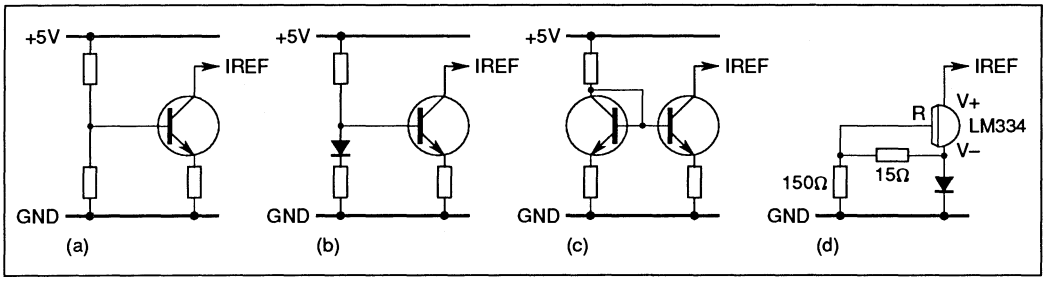


Figure 4.17

4.4.7 Current reference — decoupling

The DACs in the IMS G176 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

So long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capicitors need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high frequency capacitor of 100nF should be used to couple the IREF input to VDD (or to AVDD if the PLCC package is used). This will enable the current reference to track both low and high frequency variations in the supply.

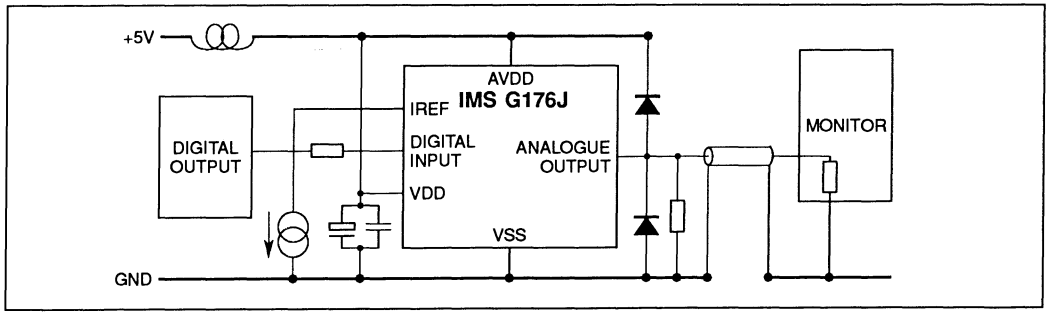


Figure 4.18 Suggested circuit using PLCC package

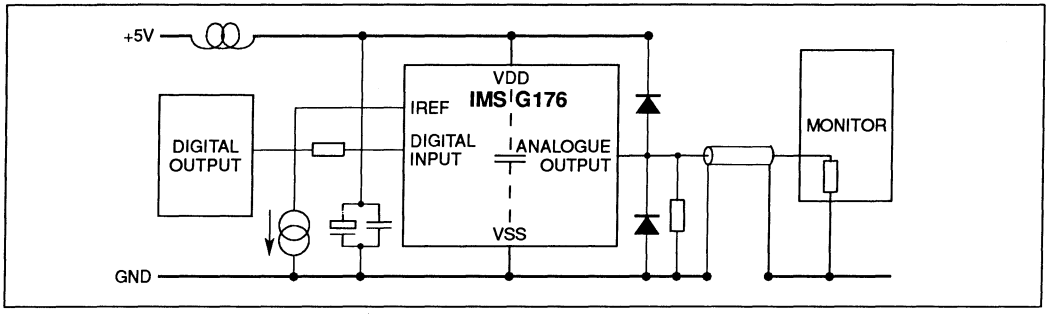


Figure 4.19 Suggested circuit using DIL package

4.5 Package specifications

4.5.1 28 pin dual-in-line package

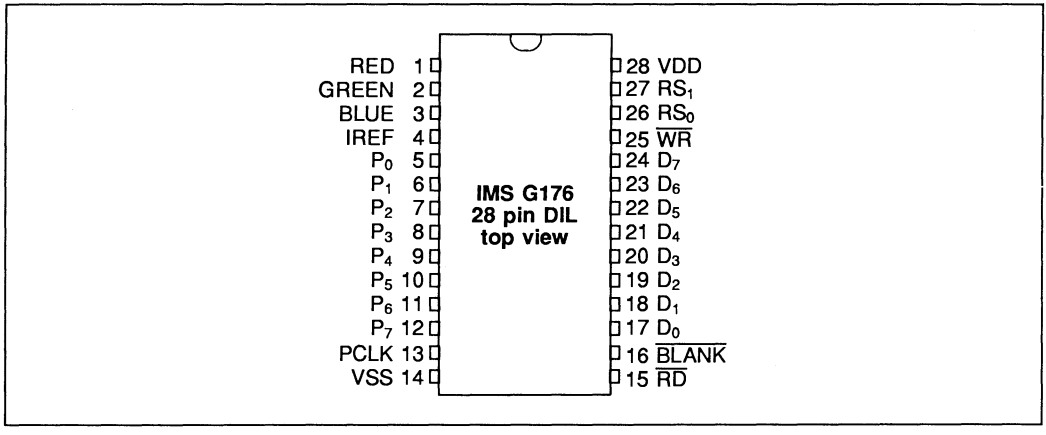


Figure 4.20 IMS G176 28 pin dual-in-line package pinout

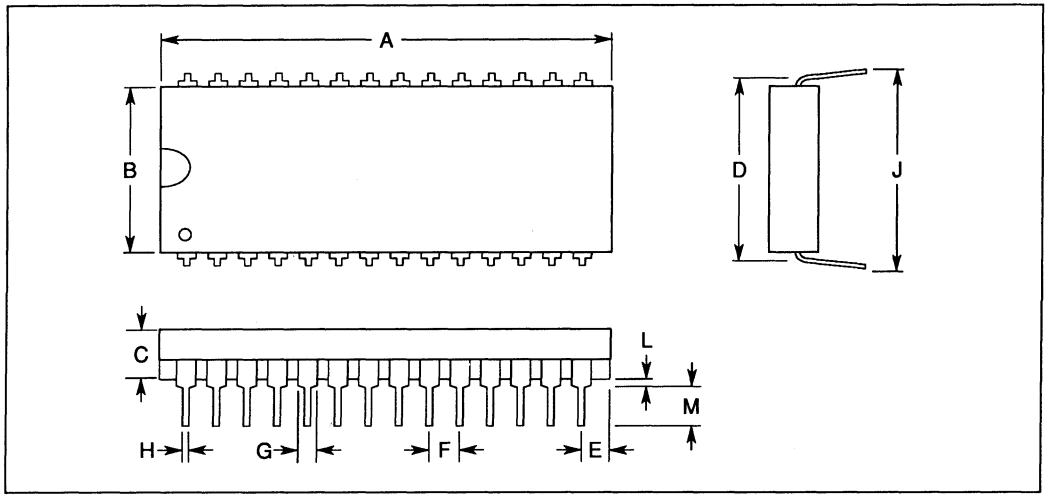


Figure 4.21 28 pin plastic dual-in-line package dimensions

	Millimetres		Inches		
DIM	NOM	TOL	NOM	TOL	Notes
A	36.830	±0.254	1.450	±0.010	
B	13.970	±0.254	0.550	±0.010	
C	4.445	±0.635	0.175	±0.025	
D	15.240	±0.076	0.600	±0.003	
E	1.905		0.075		
F	2.540		0.100		
G	1.397	±0.254	0.055	±0.010	
H	0.457		0.018		
J	16.256	±0.508	0.640	±0.020	
L	0.508		0.020		Minimum
M	3.429		0.135		Maximum

Table 4.1 28 pin plastic dual-in-line package dimensions

4.5.2 32 pin plastic leaded-chip-carrier package

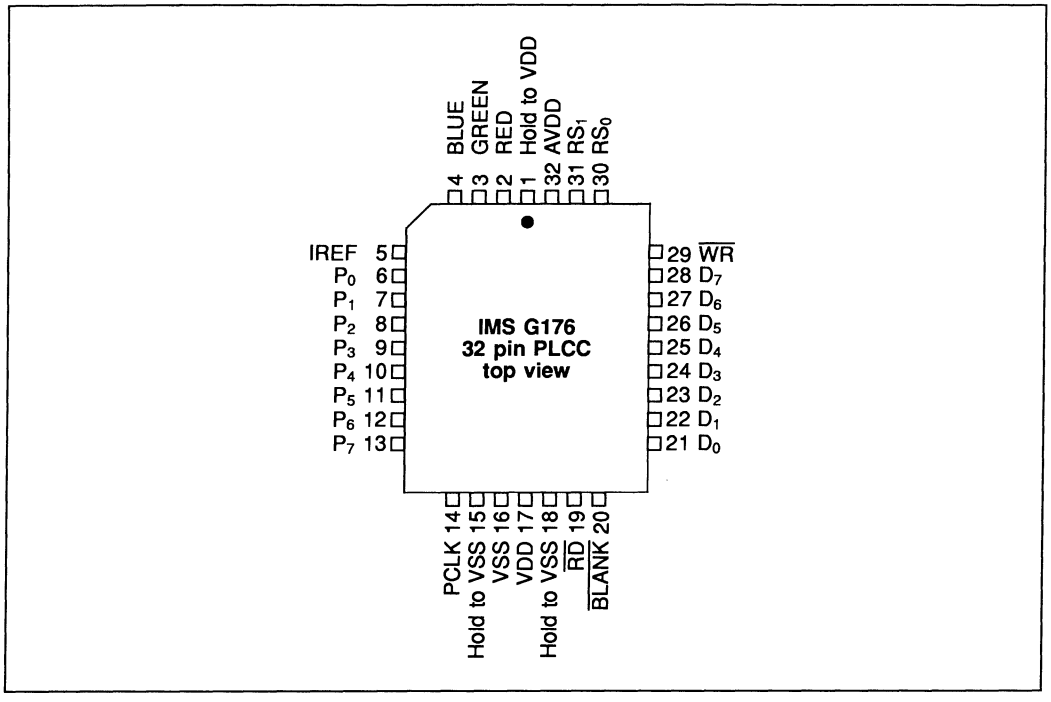


Figure 4.22 IMS G176 32 pin PLCC J-bend package pinout

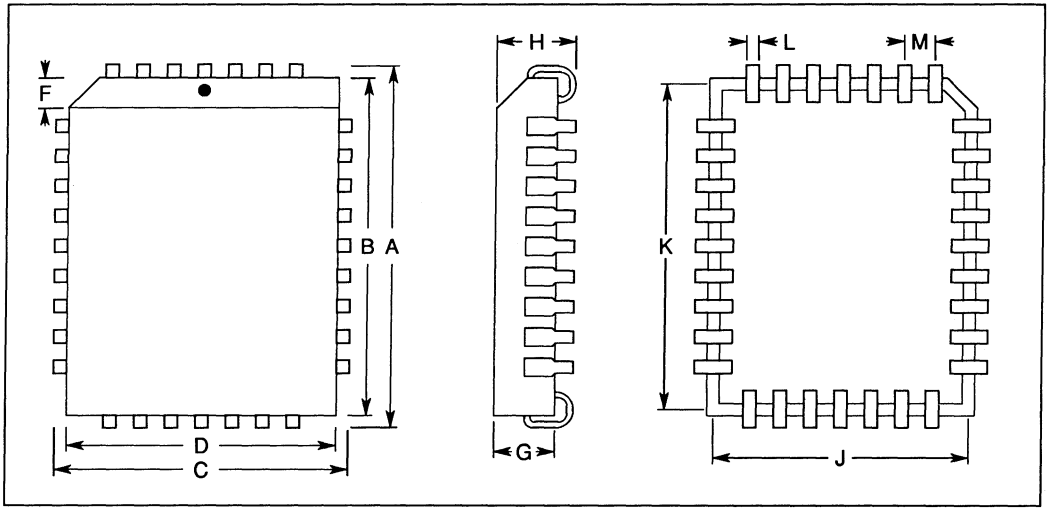


Figure 4.1 32 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	14.986	±0.127	0.590	±0.005	
B	13.970	±0.076	0.550	±0.003	
C	12.450	±0.127	0.490	±0.005	
D	11.430	±0.076	0.450	±0.003	
F	1.143		0.045		
G	2.794		0.110		
H	3.454	±0.127	0.136	±0.005	
J	10.541	±0.254	0.415	±0.010	
K	13.081	±0.254	0.515	±0.010	
L	0.432		0.017		
M	1.270		0.050		

Table 4.1 32 pin PLCC J-bend package dimensions

4.5.3 Ordering information

Device	Clock rate	Package	Part number
IMS G176	40 MHz	Plastic DIP	IMS G176P-40
IMS G176	50 MHz	Plastic DIP	IMS G176P-50
IMS G176	65 MHz	Plastic DIP	IMS G176P-65
IMS G176	40 MHz	Plastic LCC	IMS G176J-40
IMS G176	50 MHz	Plastic LCC	IMS G176J-50
IMS G176	65 MHz	Plastic LCC	IMS G176J-65

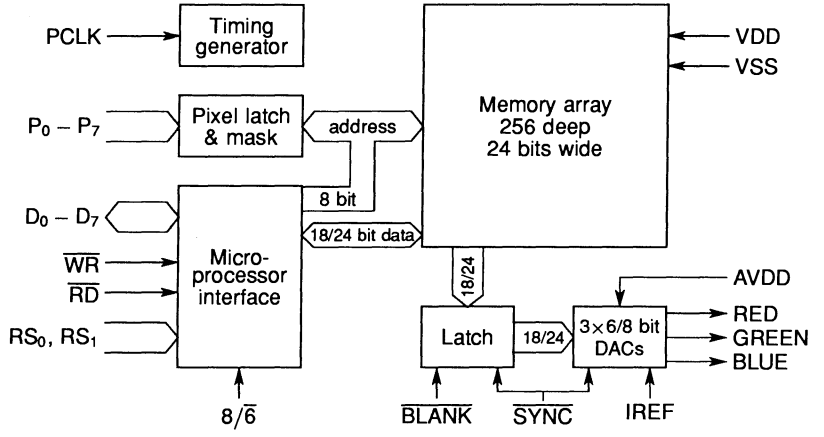
Note: IMS G176J units can be supplied mounted on tape and reel.

IMS G178

High performance CMOS colour look-up table

Designed to be compatible with IBM PS/2[1], VGA graphics systems

Preliminary Data



FEATURES

- Compatible with the RS170 video standard.
- RGB analogue output, configurable to 6 or 8 bit DAC operation
- 256K or 16M possible colours.
- Composite sync and blank on all three channels
- Pixel rates up to 80MHz.
- Low DAC glitch energy.
- Video signal output into 37.5Ω.
- TTL compatible inputs.
- Microprocessor compatible interface.
- Asynchronous access to all internal registers.
- Single monolithic, high performance CMOS.
- Up to 8 bits per pixel.
- Pixel word mask.
- Single +5V ±10% power supply.
- Low power dissipation, typically 1W at maximum pixel rate.
- 32 pin Plastic LCC package.
- Backward compatible with other members of IMS G17x look-up table family.

DESCRIPTION

The IMS G178 integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and bi-directional microprocessor interface into a single 32 pin PLCC package.

The device is switchable between 6 or 8 bit DAC operation, so is capable of displaying 256 colours from a total of 262,144 colours in 6 bit mode, or from over 16 million colours in 8 bit mode.

The device is capable of driving a doubly-terminated 75Ω line with no external buffering, and composite sync and blank signals can be generated on all three outputs.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than by modifying the look-up table.

The IMS G178 is software-compatible with the IMS G171 and both software and pin-compatible with the IMS G176 products in 6 bit mode. It replaces TTL/ECL systems and thus gives reduced component cost, board area and power consumption.

[1]IBM and PS/2 are registered trademarks of International Business Machines Corporation

5.1 Pin designations

5.1.1 Pixel interface

Signal	Pin	I/O	Signal name	Description
PCLK	14	I	Pixel Clock	The rising edge of the Pixel Clock signal controls the sampling of values on the Pixel Address, sync and blank inputs. The Pixel Clock also controls the progress of these values through the three stage pipeline of the colour look-up table to the analogue outputs.
$P_0 - P_7$	6–13	I	Pixel Address	The byte wide value sampled on these inputs is masked by the Pixel Mask register and then used as the address into the colour look-up table.
$\overline{BLANK}$	20	I	Blank	A low value on this input, when sampled, will cause a colour value of zero to be applied to the inputs of the DACs regardless of the colour value of the current pixel.
$\overline{SYNC}$	18	I	Sync	A low value on this input, when sampled, will cause an offset corresponding to 30% of the full-scale value to be removed from the DAC output. A high value, if sampled, will add the offset.

5.1.2 Analogue interface

Signal	Pin	I/O	Signal name	Description
RED GREEN BLUE	2 3 4	O O O		These signals are the outputs of the 6/8 bit DACs. Each DAC is composed of a number of current sources whose outputs are summed. The number of current sources active is controlled by the 6/8 bit binary value generated by the look-up table.
IREF	5	I	Reference current	The reference current drawn from AVDD via the IREF pin determines the current sourced by each of the current sources in the DACs.

5.1.3 Microprocessor interface

Signal	Pin	I/O	Signal name	Description
$\overline{WR}$	29	I	Write enable	The Read Enable and Write Enable signals control the timing of read and write operations on the microprocessor interface.
$\overline{RD}$	19	I	Read enable	All operations on the microprocessor interface can take place asynchronously to the pixel stream being processed by the colour look-up table. Various minimum periods between operations are specified (in terms of Pixel Clock) to allow this asynchronous behaviour. The Read and Write Enable signals should not be asserted at the same time.
RS_0, RS_1	30,31	I	Register select	The values on these inputs are sampled on the falling edge of the active enable signal ($\overline{RD}$ or $\overline{WR}$). They specify which one of the internal registers is to be accessed. See Internal Register description for the function of these registers.
$D_0 - D_7$	21–28	I/O	Program Data	Data is transferred between the 8 bit wide Program Data bus and the registers within the IMS G178 under control of the active enable signal ($\overline{RD}$ or $\overline{WR}$). In a write cycle the rising edge of $\overline{WR}$ validates the data on the program data bus and causes it to be written to the register selected. The rising edge of the $\overline{RD}$ signal signifies the end of a read cycle, after which the program data bus will cease to carry the contents of the register selected and will go to a high impedance state.
$8/\overline{6}$	15	I	8/6 mode select	When this pin is held high the part operates in 8 bit mode and when held low the part operates in 6 bit mode.

5.1.4 Power supply

Signal	Pin	Signal name	Description
			Digital and analogue power to the G178 is supplied on separate pins to provide maximum noise immunity.
VDD	17	Digital supply	Digital logic is supplied via VDD.
AVDD	32	Analogue supply	Analogue circuitry, including DACs and reference circuits, is supplied through the AVDD pin
VSS	16	Ground	

5.1.5 Internal registers

RS_1	RS_0	Size (bits)	Register name	Description
0	0	8	Address (write mode)	There is a single Address register within the IMS G178. This register can be accessed through either register select 0,0 or register select 1,1 Writing a value to address 0,0 performs the following operations which would normally precede writing one or more new colour definitions to the colour look-up table: a) Specifies an address within the colour look-up table. b) Initialises the Colour Value register.
1	1	8	Address (read mode)	Writing a value to address 1,1 performs the following operations which would normally precede reading one or more colour definitions from the colour look-up table: a) Specifies an address within the the colour look-up table. b) Loads the Colour Value register with the contents of the location in the colour look-up table addressed and then increments the Address register. A read from address 0,0 is identical to a read from 1,1.
0	1	24	Colour Value	The Colour Value register is internally a 24 bit wide register used as a buffer between the microprocessor interface and the colour look-up table. A value can be read from or written to this register by a sequence of three byte transfers at this address. When writing in 6 bit mode, only the least significant six bits ($D_0 - D_5$) are used. When operating in 8 bit mode the full 8 bit word is used for reading and writing, with D_7 being the most significant bit. The sequence of data transfer in both modes is red first, green second and blue last. After writing three values to this register its contents are written to the location in the colour look-up specified by the Address register. The Address register then increments. After reading three values from this register the contents of the location in the colour look-up table specified by the Address register are copied into the Colour Value register. The Address register then increments. Each transfer between the Colour Value register and the colour look-up table replaces the normal pixel mapping operations of the IMS G178 for a single pixel.
1	0	8	Pixel Mask	The Pixel Mask register can be used to mask selected bits of the Pixel Address value applied to the Pixel Address inputs ($P_0 - P_7$). A one in a position in the mask register leaves the corresponding bit in the Pixel Address unaltered, a zero setting that bit to zero. The Pixel Mask register does not affect the Address generated by the Microprocessor Interface when the look-up table is being accessed via that interface.

5.2 Device description

The IMS G178 is intended for use as the output stage of raster scan video systems. It contains a high speed random access store (or look-up table) of 256 × 24 bit words, three 8 bit high speed DACs, a microprocessor interface and a pixel word mask. In addition, the part can be configured, through the use of the 8/$\overline{6}$ pin to operate in a restricted 6 bit mode and emulate the function of the IMS G171 and IMS G176. In this mode only 18 bits of the 24 bit colour table are used and the DACs are restricted to 6 bit resolution.

An 8 bit value read in on the Pixel Address inputs is used as a read address for the look-up table and results in an 18/24 bit data word being output from the table. This data is partitioned as three fields of 6/8 bits, each field being applied to the inputs of one DAC.

Pixel rates of up to 80 MHz are achieved by pipelining the memory access over three clock periods.

An externally generated blank signal can be input to the IMS G178. This signal acts on all three of the analogue outputs. The $\overline{\text{BLANK}}$ signal is delayed internally so that it appears at the analogue outputs with the correct relationship to the pixel stream.

An externally generated sync signal may also be supplied to the IMS G178 on the $\overline{\text{SYNC}}$ pin. This can be used to generate composite video sync on all three of the DAC outputs.

The contents of the look-up table can be accessed via an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows colour value accesses to be totally asynchronous to the video path.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes to the effective contents of the colour look-up table to facilitate such operations as animation, overlays and flashing objects. Operations on the contents of the mask register can also be totally asynchronous to the pixel stream.

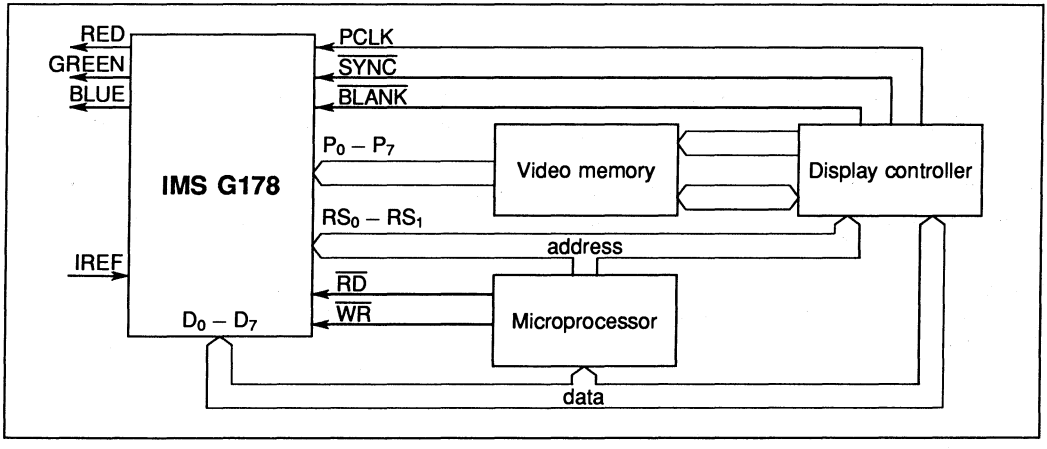


Figure 5.1 Typical IMS G178 application

5.2.1 Video path

$P_0 - P_7$, $\overline{BLANK}$ and $\overline{SYNC}$ inputs are sampled on the rising edge of PCLK, their effect appears at the analogue outputs after three further rising edges of PCLK.

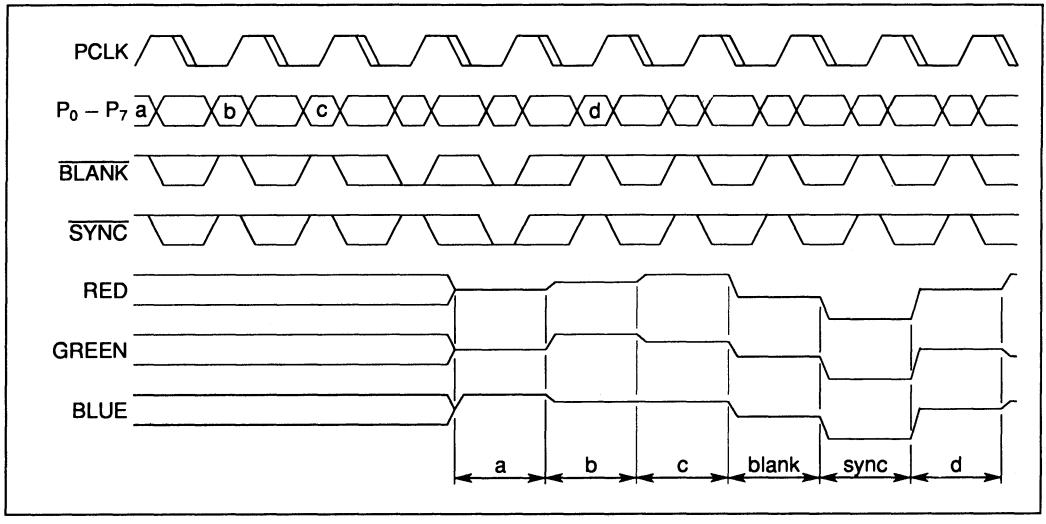


Figure 5.2

5.2.2 Analogue outputs

The outputs of the DACs are designed to be capable of producing 1.0 volt peak white amplitude (conforming to the RS170 standard) with an IREF of 8.88 mA when driving a doubly terminated 75Ω load. This corresponds to an effective DAC output load ($R_{EFFECTIVE}$) of 37.5Ω.

The $\overline{BLANK}$ and $\overline{SYNC}$ inputs to the IMS G178 act on all three of the analogue outputs. When the $\overline{BLANK}$ input is low a binary zero is applied to the inputs of the DACs. When $\overline{SYNC}$ is low the sync pedestal is removed from the DAC output.

The IMS G178 internally compensates for the switch between 6 and 8 bit operation; therfore the expressions for calculating the full white component and the sync component (if used) of the video signal in both modes are as follows:

$$V_{WHITE} = 2.058 \times IREF \times R_{EFFECTIVE} \qquad V_{WHITE}$$

$$V_{SYNC} = 0.878 \times IREF \times R_{EFFECTIVE} \qquad V_{SYNC}$$

5.2.3 Microprocessor interface

Below are listed the three microprocessor interface registers within the IMS G178 and the four locations through which they can be accessed:

RS_1	RS_0	Register name
0	0	Address (write mode)
1	1	Address (read mode)
0	1	Colour Value
1	0	Pixel Mask

The contents of the colour look-up table can be accessed via the Colour Value register and the Address register.

Writing to the look-up table

To set a new colour definition a value specifying a location in the colour look-up table is first written to the write mode Address register. The values for the red, green and blue intensities are then written in succession to the Colour Value register. After the blue data is written to the Colour Value register the new colour definition is transferred to the colour look-up table and the Address register is automatically incremented.

As the Address register increments after each new colour definition has been transfered from the Colour Value register to the colour look-up table, it is simple to write a set of consecutive locations with new colour definitions. First the start address of the set of locations is written to the write mode Address register; then the colour definitions for each location are written sequentially to the Colour Value register.

Reading from the look-up table

To read a colour definition a value specifying the location in the look-up table to be read is written to the read mode Address register. After this value has been written, the contents of the location specified are copied to the Colour Value register and the Address register is then automatically incremented.

The red, green and blue intensity values can be read by a sequence of three reads from the Colour Value register. After the blue value has been read the location in the look-up table currently specified by the Address register is copied to the Colour Value register and the Address register is again incremented automatically.

Thus a set of colour definitions in consecutive locations can be read simply by writing the start address of the set to the read mode Address register and then sequentially reading the colour definitions for each location in the set.

Whenever the Address register is updated any unfinished colour definition read or write is aborted and a new one may begin.

Asynchronous microprocessor interface access

Accesses to all registers may occur without reference to the high speed timing of the pixel stream being processed by the IMS G178. Data transfers between the look-up table and the Colour Value register and modifications to the Pixel Mask register are synchronized to PCLK by internal logic. This is done in the period between the microprocessor interface accesses. Thus, various minimum periods are specified between microprocessor interface accesses to allow for the appropriate transfers to take place.

The Pixel Mask register

The pixel address used to access the colour look-up table through the pixel interface is the result of the bitwise ANDing of the incoming pixel address and the contents of the Pixel Mask register. This pixel masking process can be used to alter the displayed colours without altering the video memory or the look-up table contents. Thus, by partitioning the colour definitions by one or more bits in the pixel address such effects as rapid animation, overlays and flashing objects can be produced.

The Pixel Mask register is completely independent of the Address and Colour Value registers.

5.3 Electrical specifications

5.3.1 Absolute maximum ratings *

Symbol	Parameter	Min.	Max.	Units	Notes
VDD/AVDD	DC supply voltage		7.0	V	
	Voltage on input and output pins	−1.0	VDD+0.5	V	
TS	Storage temperature (ambient)	−65	150	°C	
TA	Ambient temperature under bias	−40	85	°C	
PDmax	Power dissipation		1.5	W	
	Reference current	−15		mA	
	Analogue output current (per output)		45	mA	
	DC digital output current		25	mA	

* Stresses greater than those listed under 'Absolute maximum ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5.3.2 DC operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1)
VDD/AVDD	Positive supply voltage	4.5	5.0	5.5	V	2,3
GND	VSS		0		V	
VIH	Input logic '1' voltage	2.0		VDD+0.5	V	3
VIL	Input logic '0' voltage	−0.5		0.8	V	4
TA	Ambient operating temperature	0		70	°C	5
IREF	Reference current	−7.0		−10	mA	6

Notes

1 All voltages are with respect to GND unless specified otherwise.

2 This parameter allows for a range of fixed power supply voltages to be used; it does not imply that the supply voltage should be allowed to vary dynamically within these limits.

3 These voltage ranges apply equally for AVDD and VDD. (N.B. VDD must = AVDD)

4 VIL(min) = −1.0V for a pulse width not exceeding 25% of the duty cycle (tCHCH) or 10ns, whichever is the smaller value.

5 With a 400 linear ft/min transverse air flow.

6 Reference currents below the minimum specified may cause the analogue outputs to become invalid.

DC electrical characteristics

Symbol	Parameter	Min.	Max.	Units	Notes (1,2,3)
IDD	Average power supply current		265	mA	4, IMS G178-80
IDD	Average power supply current		230	mA	4, IMS G178-65
IDD	Average power supply current		215	mA	4, IMS G178-50
IDD	Average power supply current		205	mA	4, IMS G178-40
VREF	Voltage at IREF input	VDD−3	VDD	V	5
IIN	Digital input current (any input)		±10	μA	6,7
IOZ	Off state digital output current		±50	μA	6,8
VOH	Output logic '1'	2.4		V	IO = −5mA
VOL	Output logic '0'		0.4	V	IO = 5mA

1 All voltages are with respect to GND unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Over the range of the DC operating conditions unless specified otherwise.

4 IO = IO(max). IDD is dependent on digital output loading and cycle rate, the specified values are obtained with the outputs unloaded and at the maximum rated Pixel Clock frequency.

5 These voltage ranges apply equally for AVDD and VDD. (N.B. VDD must = AVDD)

6 VDD = max, GND $\leq$ VIN $\leq$ VDD.

7 On digital inputs, pins 6–14, 19, 20, 29–31.

8 On digital input/output, pins 21–28.

5.3.3 DAC characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes (1,2,3)
	Resolution	6		8	bits	depending on mode
VO(max)	Output voltage			1.5	V	IO$\leq$10mA
IO(max)	Output current			−29.5	mA	VO$\leq$1V
	Full scale error			±5	%	4
	SYNC pedestal error			±10	%	
	DAC to DAC correlation error			±2.5	%	5
	Integral linearity error			±0.5	LSB	6, 6 bit mode
	Integral linearity error			±1	LSB	6, 8 bit mode
	Rise time (10% to 90%)			6	ns	7, IMS G178-65/80
	Rise time (10% to 90%)			8	ns	7, IMS G178-40/50
	Full scale settling time			12.5	ns	7,8,9, IMS G178-80
	Full scale settling time			15.3	ns	7,8,9, IMS G178-65
	Full scale settling time			20	ns	7,8,9, IMS G178-50
	Full scale settling time			25	ns	7,8,9, IMS G178-40
	Glitch energy		75		pVsec	7,9

Notes

1 All voltages are with respect to GND unless specified otherwise.

2 The Pixel Clock frequency must be stable for a period of at least 20μs after power-up (or after change in a Pixel Clock frequency) before proper device operation is guaranteed.

3 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

4 Full scale error from the value predicted by the design equations (Sync off).

5 About the mid point of the distribution of the three DACs measured at full scale deflection (Sync off).

6 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed (Sync off).

7 Load = 37.5Ω + 30pF with IREF = −8.88mA

8 From a 2% change in the output voltage until settling to within 2% of the final value.

9 This parameter is sampled, not 100% tested.

5.3.4 AC test conditions

Input pulse levels	GND to 3V
Typical input rise and fall times (10% to 90%)	3ns
Digital input timing reference level	1.5V
Digital output timing reference level	0.8V and 2.4V
Digital output load	see figure 5.3

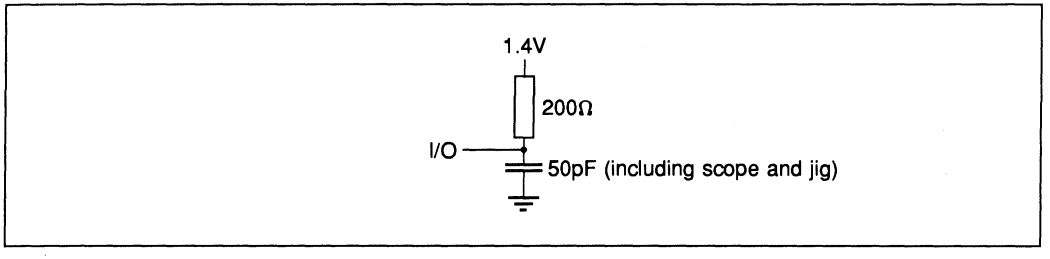


Figure 5.3 Digital output load

5.3.5 Capacitance

Symbol	Parameter	Min.	Max.	Units	Notes (1,2)
CI	Digital input		7	pF	
CO	Digital output		7	pF	3
COA	Analogue output		10	pF	4

Notes

1 These parameters are sampled, not 100% tested.

2 Measured on a BOONTON METER.

3 $\overline{RD} \geq$ VIH(min) to disable $D_0 - D_7$.

4 $\overline{BLANK} \leq$ VIL(max) to disable RED, GREEN and BLUE.

5.3.6 Video operation (Figure 5.4)

Symbol	Parameter	40MHz Min	50MHz Min	65MHz Min	80MHz Min	All Max	Units	Notes
t_{CHCH}	PCLK period	25	20	15.3	12.5	10000	ns	
Δt_{CHCH}	PCLK jitter					±2.5	%	1
t_{CLCH}	PCLK width low	9	6	5	5	10000	ns	
t_{CHCL}	PCLK width high	7	6	5	5	10000	ns	
t_{PVCH}	Pixel address set-up time	5	4	3	3		ns	2
t_{CHPX}	Pixel address hold time	5	4	3	3		ns	2
t_{BVCH}	$\overline{BLANK}$ setup time	5	4	3	3		ns	
t_{CHBX}	$\overline{BLANK}$ hold time	5	4	3	3		ns	
t_{SVCH}	$\overline{SYNC}$ setup time	5	4	3	3		ns	
t_{CHSX}	$\overline{SYNC}$ hold time	5	4	3	3		ns	
t_{CHAV}	PCLK to valid DAC output	5	5	5	5	30	ns	3
Δt_{CHAV}	Differential output delay					2	ns	4
	Pixel clock transition time					50	ns	

Notes

1 This parameter allows for variation in the Pixel Clock frequency, but does not permit the Pixel Clock period to vary outside the minimum and maximum values for Pixel Clock (t_{CHCH}) period specified above.

2 It is required that the Pixel Address input to the colour look-up table be set up as a valid logic level with the appropriate setup and hold times to each rising edge of PCLK (this requirement must be met during the blanking period).

3 A valid analogue output is defined as when the changing analogue signal is half way between its successive values. This parameter is stable with time but can vary between different devices and may vary with different DC operating conditions.

4 Between different analogue outputs on the same device.

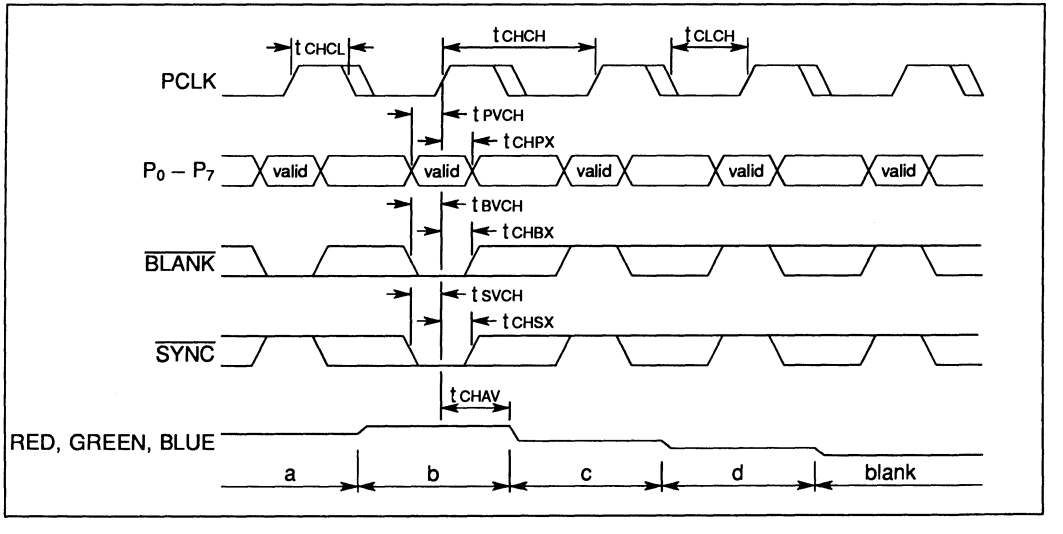


Figure 5.4 Video operation

5.3.7 Microprocessor interface operation

Symbol	Parameter	All Max	40 MHz Min	50 MHz Min	65 MHz Min	80 MHz Min	Units	Notes
t_{WLWH}	$\overline{WR}$ pulse width low		50	50	50	50	ns	
t_{RLRH}	$\overline{RD}$ pulse width low		50	50	50	50	ns	
t_{SVWL}	Register select setup time		15	10	10	10	ns	
t_{SVRL}	Register select setup time		15	10	10	10	ns	
t_{WLSX}	Register select hold time		15	10	10	10	ns	
t_{RLSX}	Register select hold time		15	10	10	10	ns	
t_{DVWH}	Write data setup time		15	10	10	10	ns	
t_{WHDX}	Write data hold time		15	10	10	10	ns	
t_{RLQX}	Output turn-on delay		5	5	5	5	ns	
t_{RLQV}	Read enable access time	40					ns	
t_{RHQX}	Output hold time		5	5	5	5	ns	
t_{RHQZ}	Output turn-off delay	20					ns	1
t_{WHWL1}	Successive write interval							
t_{WHRL1}	Write followed by read interval							
t_{RHRL1}	Successive read interval							
t_{RHWL1}	Read followed by write interval		$4 \times t_{CHCH} + 30ns$				ns	2
t_{WHWL2}	Write after colour write							
t_{WHRL2}	Read after colour write							
t_{RHWL2}	Write after colour read							
t_{RHRL2}	Read after colour read		$6 \times t_{CHCH} + 40ns$				ns	2
t_{WHRL3}	Read after read address write							
t_{CYC}	Write/Read cycle time		$6 \times t_{CHCH} + 40ns$				ns	2,3
	Write/Read enable transition time	50					ns	

Notes

1 Measured ±200mV from steady output voltage.

2 This parameter allows for synchronisation between operations on the microprocessor interface and the pixel stream being processed by the colour look-up table.

3 From the rising edge of Read or Write pulse to the rising edge of the next Read or Write pulse.

Operations on the microprocessor port are internally synchronised to the pixel clock in the periods between cycles. This is the reason for the time between cycles on the microprocessor port being specified in terms of pixel clock periods.

In the case of the IMS G178 the minimum cycle time for all accesses (defined as the period between successive rising edges of the read or write strobe) is $6 \times t_{CHCH} + 40ns$.

For example, in the case of a 25MHz system the pixel clock period (t_{CHCH}) would be 40ns and the minimum cycle time for accesses on the microprocessor port is:

$$6 \times 40ns + 40ns = 280ns$$

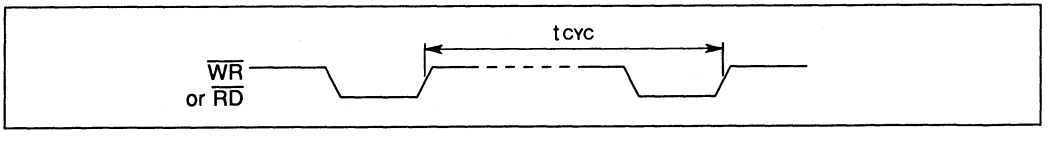


Figure 5.5 Write/Read cycle time

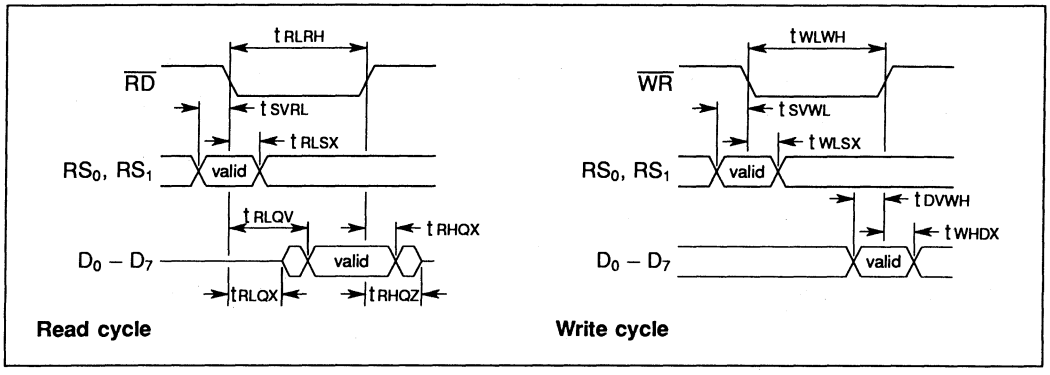


Figure 5.6 Basic read/write cycles

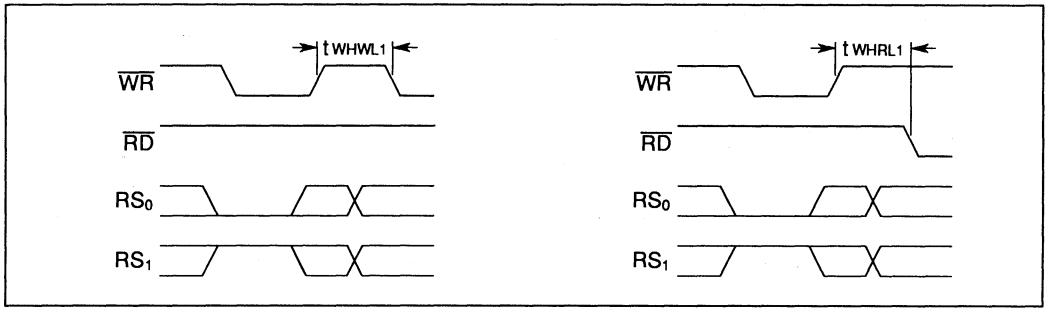


Figure 5.7 Write to pixel mask register followed by any access

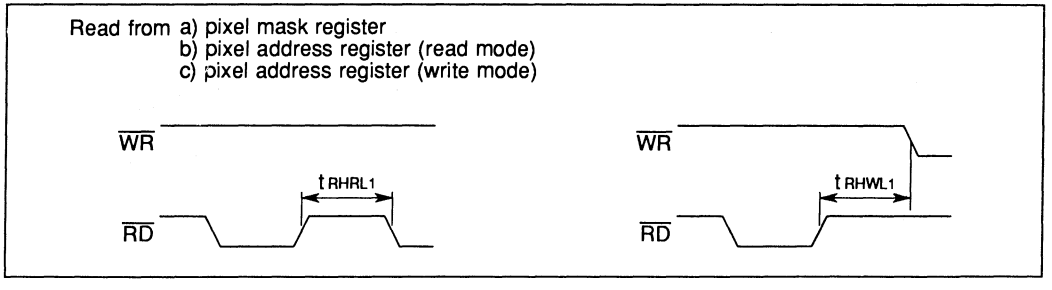


Figure 5.8 Read from register followed by any access

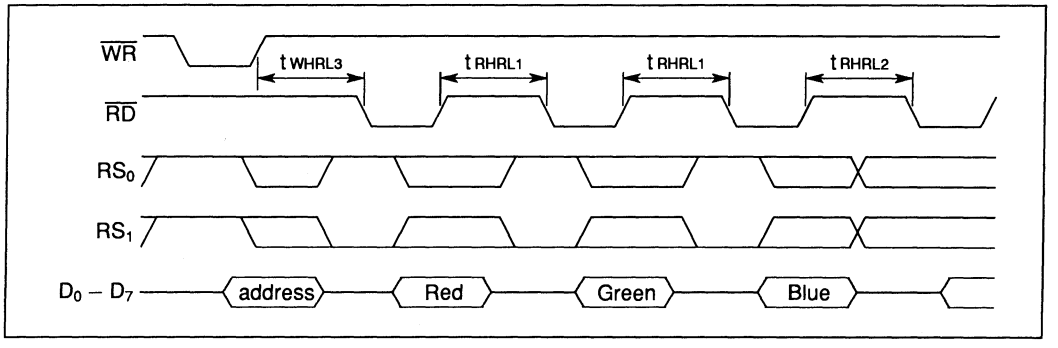


Figure 5.9 Colour value read followed by any read

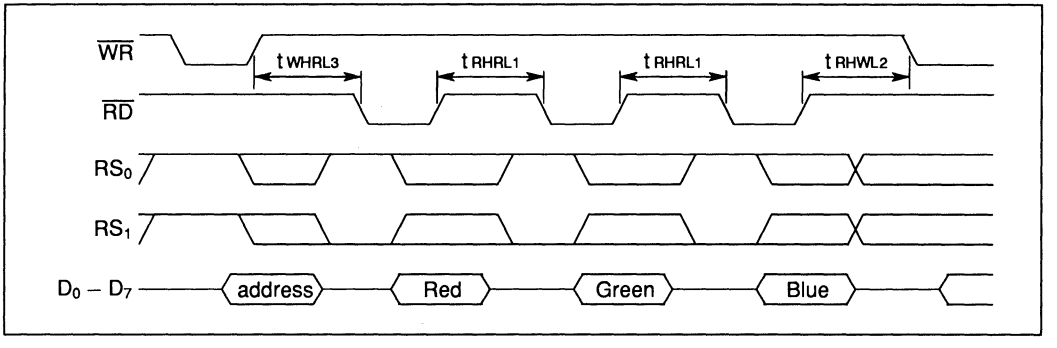


Figure 5.10 Colour value read followed by any write

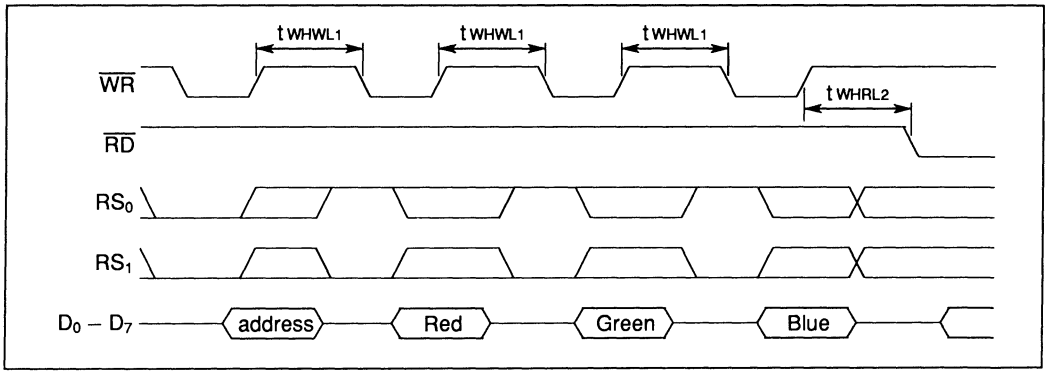


Figure 5.11 Colour value write followed by any read

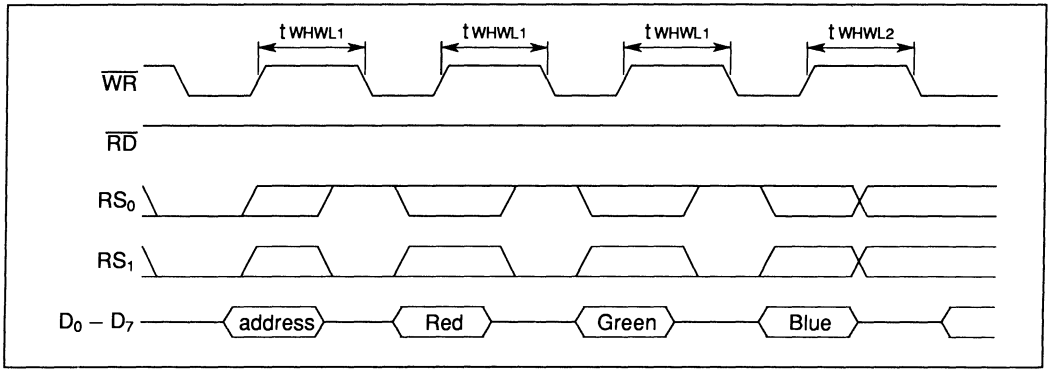


Figure 5.12 Colour value write followed by any write

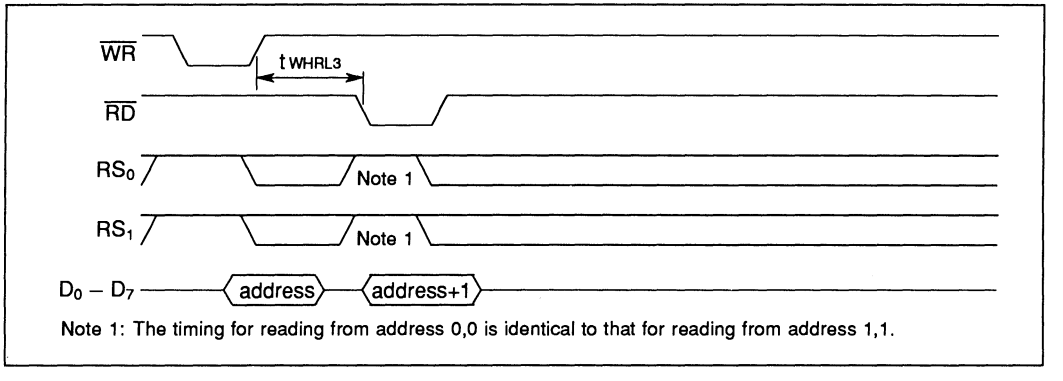


Figure 5.13 Write and read back address register (read mode)

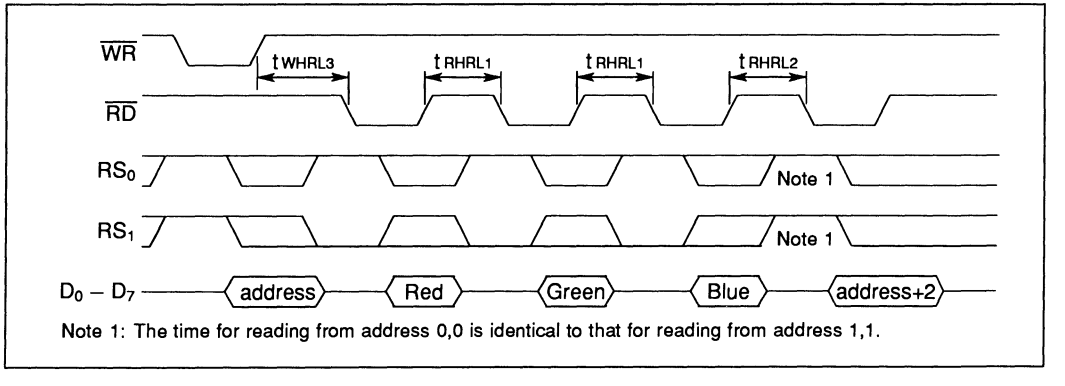


Figure 5.14 Read colour value then read the address register (read mode)

5.4 Designing with the IMS G178

5.4.1 Board layout — general

The IMS G178 is a high speed CMOS device. As such it has relatively low DC power requirements. However, CMOS devices may draw large transient currents from the power supply. To supply the transient currents present in high speed video circuitry it is essential that proper consideration is given to board layout and decoupling circuitry when using the IMS G178. A four layer board with separate power and ground planes is strongly recommended, since this will minimise differential noise and impedance in the supply.

5.4.2 Power supply decoupling

The DACs in the IMS G178 are referenced to the positive power supply, so are fairly insensitive to ground supply noise. To minimise the coupling of digital noise from the digital sections of the IMS G178, independent analogue and digital +5V supplies (AVDD and VDD respectively) are provided.

It is further recommended that a high-frequency capacitor of around 100nF (preferably a chip capacitor) should be placed as close as possible to the package between these supplies and VSS. A large tantalum capacitor (between 22μF and 47μF) should also be placed in parallel with this high-frequency capacitor.

In cases where the main digital supply on the graphics board is too noisy to achieve a satisfactory analogue output from the G178 DACs, a separate decoupled supply may be created just for the G178. An inductor may be used to decouple this supply to the main board supply. This forms a low pass filter rejecting high frequency noise components present on the main board supply.

5.4.3 Analogue output — line driving

The DACs in the IMS G178 are made from summed, switched current sources. IREF sets the current sourced by each current source, the digital input to each DAC determines how many current sources are active. The load resistance between the DAC output and VSS determines the voltage produced by each DAC.

The connection between the DAC outputs of the IMS G178 and the RGB inputs of the monitor it is driving should be regarded as a transmission line. Impedance changes along the transmission line will result in the reflection of part of the video signal back along the transmission line. These reflections may result in a degradation of the picture displayed by the monitor. To ensure good fidelity, RF techniques should be observed. The PCB trace connecting the IMS G178 to the off-board connector should be sized so as to form a transmission line of the correct impedance. Correctly matched RF connectors should be used to connect the PCB to the coaxial cable, and from the cable to the monitor being driven.

Two methods of DAC termination and their relative merits are described here.

Double termination

A load resistor is placed at both the DAC output and the monitor input. The resistor values should be equal to the characteristic impedance of the line.

Double termination of the DAC output allows both ends of the transmission line between the DAC outputs and the monitor inputs to be correctly matched, and thus should result in an ideal reflection free system.

This arrangement is relatively tolerant to variations in transmission line impedance (e.g. a mismatched connector) since no reflections occur from either end of the line.

Also the rise time of the DAC outputs is dependent on the RC time constant of the load it is driving. Thus a double terminated DAC output will rise faster than any singly terminated output.

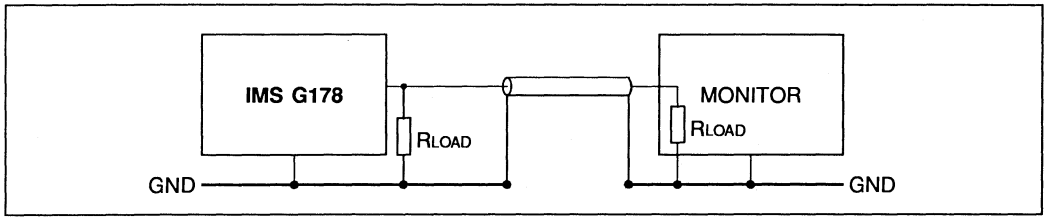


Figure 5.15 Double termination

Buffered signal

If the IMS G178 is required to drive large capacitative loads (for instance long lossy cable runs) it may be necessary to buffer the DAC outputs. The buffer will have a relatively high input impedance. The connection between the DAC outputs and the buffer inputs should be considered as a transmission line. The buffer output will have a relatively low impedance so should be matched to the transmission line between it and the monitor with a series terminating resistor. The transmission line should be terminated at the monitor.

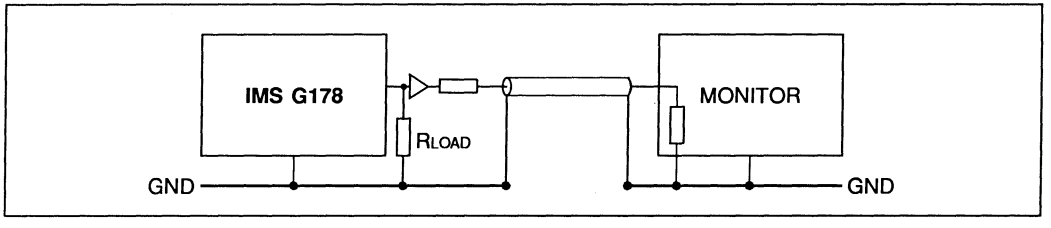


Figure 5.16 Buffered signal

5.4.4 Analogue output — protection

CMOS devices are susceptible to damage from from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G178 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However, if the analogue outputs of the IMS G178 are made available at connectors outside the graphic system they are still exposed to static damage and other hazardous voltages. Protection diodes (e.g. IN4148 or any low cost silicon diode) should be considered at this exposed interface (see figure 5.18).

5.4.5 Digital input termination

The PCB trace lines between the outputs of the TTL devices driving the IMS G178 and the input to the IMS G178 have a low impedance source and are terminated with a high impedance. They behave like low impedance transmission lines, so signal transitions will be reflected from the high impedance input of the IMS G178. Similarly signal transitions will be inverted and reflected from the low impedance TTL output. To reduce or eliminate the ringing and in particular the undershoot that reflections cause, line termination is recommended. The termination may either be series or parallel.

The recommended technique is to use series termination. Series termination has the advantage of drawing no DC current and using fewer components. Series termination is accomplished by placing a resistor in series with the signal line at the output of the TTL driver. This matches the TTL output impedance to that of the transmission line and so ensures that any signal incident on the TTL output is not reflected.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a value around 100Ω will be required. Because each design will result in a different signal impedance, a resistor of a predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be found empirically.

5.4.6 Current reference — design

To ensure that the output current of the DACs is predictable and stable with temperature variations an active current reference is recommended. Figure 5.17 shows four designs of current reference.

Figure 5.17d shows the use of the LM334 precision current source as a current reference. It is shown in its temperature compensated configuration. The reference current is set by a single resistor (15Ω in this case) and is independent of the value of power supply voltage.

Figures 5.17a–c are similar circuits. Each circuit uses three resistors and the power supply voltage to set the reference current IREF through a transistor. In circuit 5.17b and c the thermal variations in the base emitter voltage of the transistor are compensated by the use of a forward biased diode (a transistor acting as a diode in the case of circuit 5.17c).

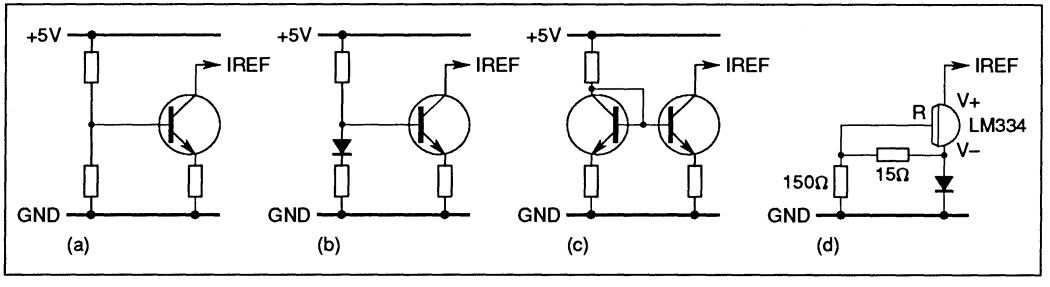


Figure 5.17

5.4.7 Current reference — decoupling

The DACs in the IMS G178 are made from switched current sources which are based around a current mirror. The total current output by each DAC is determined by the number of active current sources and the reference current IREF.

As long as any supply variations are minor, or a suitably high quality current reference is used which tracks the variations, then no coupling capacitor need be used.

However, voltage variations on the supply not managed by the current reference circuit will result in variations in the DAC output current. If the bandwidth of the current reference circuit is not sufficient to track these supply variations it is recommended that a coupling capacitor (47μF to 100μF) in parallel with a high-frequency capacitor of 100nF should be used to couple the IREF input to AVDD. This will enable the current reference to track both low and high frequency variations in the supply.

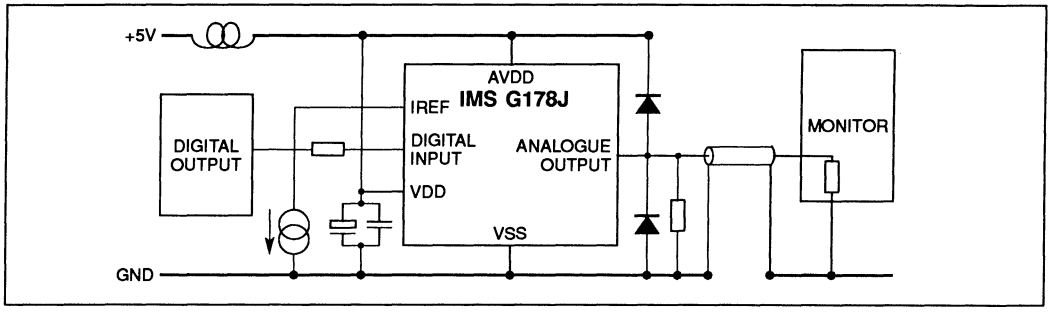


Figure 5.18 Suggested circuit

5.5 Package specifications

5.5.1 32 pin plastic leaded-chip-carrier package

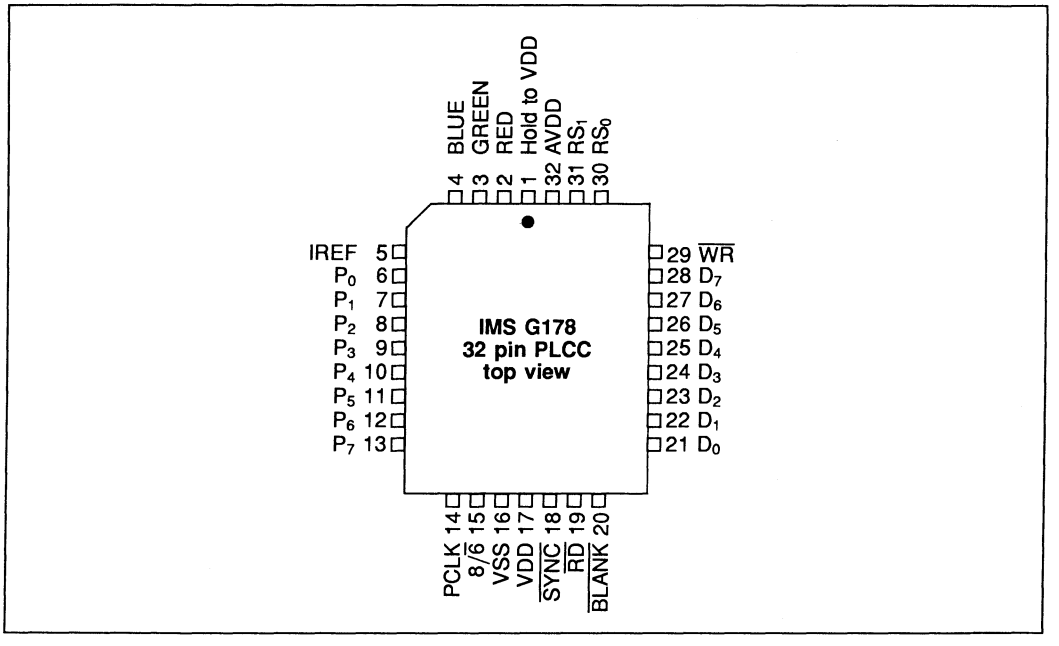


Figure 5.19 IMS G178 32 pin PLCC J-bend package pinout

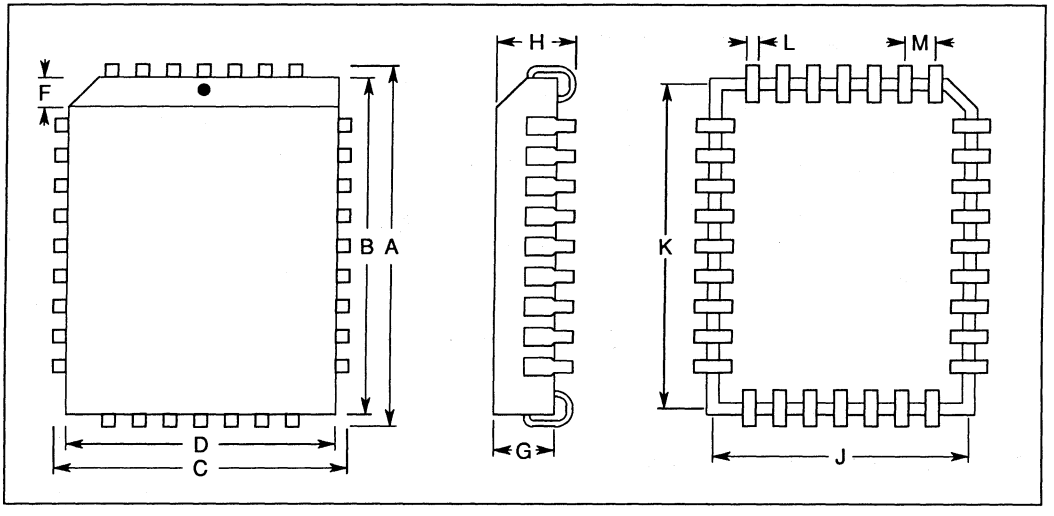


Figure 5.20 32 pin PLCC J-bend package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	14.986	±0.127	0.590	±0.005	
B	13.970	±0.076	0.550	±0.003	
C	12.450	±0.127	0.490	±0.005	
D	11.430	±0.076	0.450	±0.003	
F	1.143		0.045		
G	2.794		0.110		
H	3.454	±0.127	0.136	±0.005	
J	10.541	±0.254	0.415	±0.010	
K	13.081	±0.254	0.515	±0.010	
L	0.432		0.017		
M	1.270		0.050		

Table 5.1 32 pin PLCC J-bend package dimensions

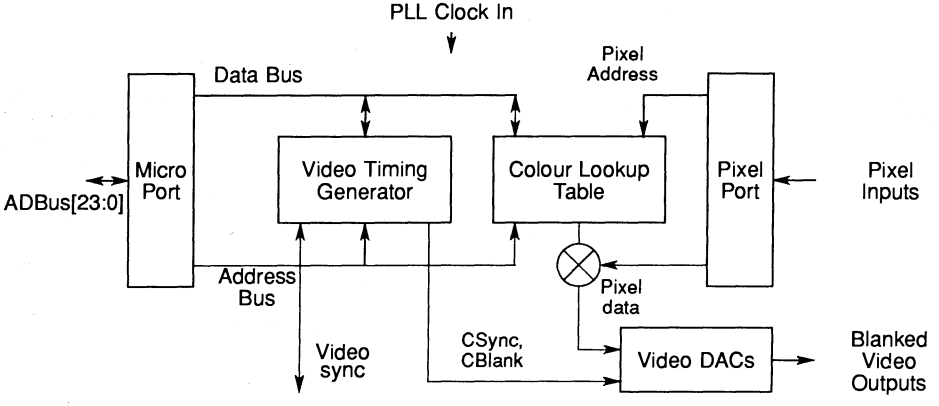
5.5.2 Ordering information

Device	Clock rate	Package	Part number
IMS G178	40 MHz	Plastic LCC	IMS G178J-40
IMS G178	50 MHz	Plastic LCC	IMS G178J-50
IMS G178	65 MHz	Plastic LCC	IMS G178J-65
IMS G178	80 MHz	Plastic LCC	IMS G178J-80

Note: IMS G178J units can be supplied mounted on tape and reel.

IMS G300
colour video controller

Preliminary Data



FEATURES

Video rates up to 120MHz
Software configurable video timing generator
Interlaced or non-interlaced video
Generates Studio broadcast standard Sync signals
Supplies blanked analogue video outputs
Internal or external Sync options
Single or synchronous multiple operation

---

4 into 1 multiplexed Pixel input
On chip 256 location x 24 bits colour palette
Triple high speed 8 bit video DACs
RS 170a and EIA 343-A compatible
Indirect 8 planes per pixel mode via palette, or:
24 planes per pixel mode direct to DACs

General purpose Video RAM support
Synchronous VRAM DataTransfer strobing
Video RAM Row address auto-increment
Screen line length independent of VRAM architecture
On-chip phase-locked loop (PLL)
All external signals and clocks at 1/4 video rate

APPLICATIONS

General purpose raster scan control
CRT Screen control
Colour plotters and printers
Plane-based workstations
Portable personal computers

Three dimensional modelling
Real time animation systems
Computer visualisation
Multiple processor systems
Frame swapping systems
Scene insertion into live camera data

Distributed computing environments

6.1 Introduction

The IMS G300 is a dedicated support chip which provides all necessary functions for controlling real time operation of a raster scan video system, using dual ported video DRAMs. The facilities provided are designed to isolate the host processor from the constraints of the real time system without in any way interfering with the ability of the processor to specify and manipulate screen data.

The device consists of a programmable video timing generator with screen refresh and auto line increment capability, a 256 location by 24 bit colour lookup table (LUT), a triple 8 bit video DAC and an on chip phase-locked loop (PLL); see figure 6.1.

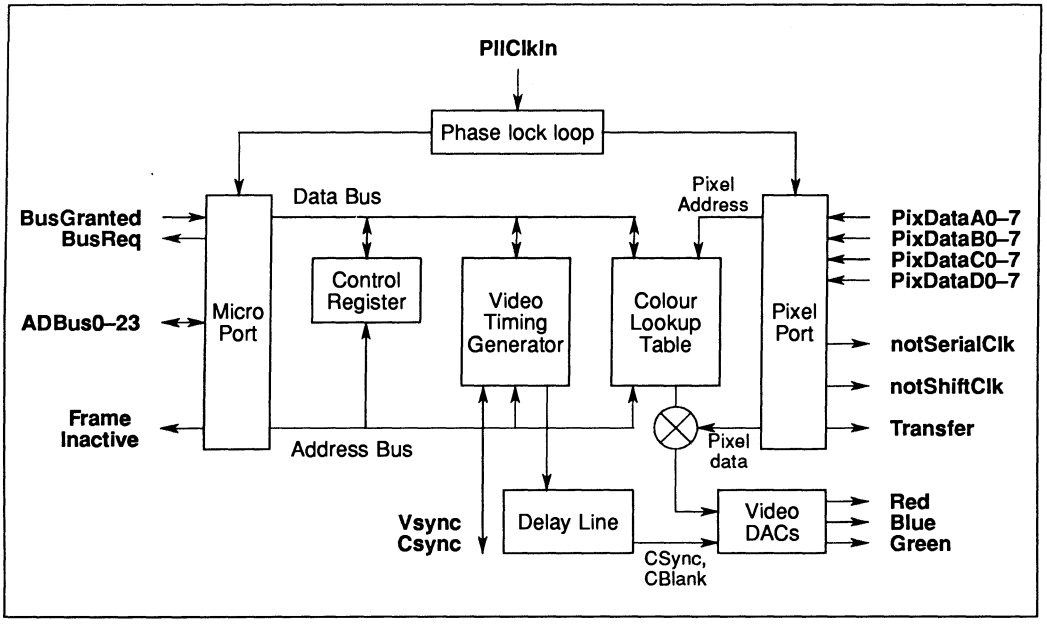


Figure 6.1 IMS G300 Block Diagram

6.1.1 Clocks

Use of the phase-locked loop allows the part to be driven from a low speed clock in the 5MHz to 9MHz range, which is internally multiplied by a user-specified factor to achieve video data rates. The controller can be clocked by a full rate system clock if desired, although at a reduced frequency compared to that achievable with the PLL. This option is selected by making a PCB link.

6.1.2 Video timing

The video timing generator is a programmable finite state machine which is programmed by loading a number of screen description parameters. It can be configured to free run, providing composite or separate sync, or to lock onto an external synchronising source which may be another IMS G300, giving the potential for multiple, synchronous video systems. In either mode, it supplies composite blank to the video DACs and is capable of supplying them with tesselated or plain composite sync when in internal (master) mode. The timing generator runs at one quarter of the video dot rate and the screen parameters are defined in terms of its resolution. Thus the screen is defined in multiples of four pixels.

6.1.3 Screen management

Video RAM support is provided by a screen refresh mechanism which performs a DMA to the video RAM and which allows seamless mid-line update of the screen. The video RAM shift register can be made to behave as though it is infinitely long and the flow of pixels onto the screen is controlled by starting and stopping the pixel shift clock at the appropriate times (a true serial clock output is also provided for system synchronisation). This method of control divorces the screen line length from dependence on the video RAM shift register length, allowing for very long display lines without extra multiplexing and for efficient use of memory irrespective of screen dimensions.

6.1.4 Pixel port

The pixel port is 32 bits wide and has two modes of operation, which are selectable in software.

In mode 1, the port interprets each 32-bit word as four byte-wide pixel addresses and accelerates them to full dot rate before addressing the LUT. The 24 bits of pixel data thus accessed are then sent to the video DACs for display.

In mode 2, the top byte of the input word is ignored and the remaining 24 bits are interpreted as pixel data. No acceleration takes place and the data is sent directly to the DACs.

Mode 2 is usable only when an external dot-rate clock is supplied, mode 1 can also be used with the phase-locked loop.

6.1.5 Video DACs

The triple video DAC has 8 bit resolution at the full video rate and produces blanked video signals. It is possible to select various styles of analogue output to conform with generally approved monitor and broadcast television output levels and timings, including RS170a and EIA-343.

6.1.6 Programming port

The IMS G300 has a memory mapped architecture which enables fast configuration and colour cycling through the use of block move or some other simple memory write cycle. Its micro-port appears as a block of memory (occupying 1/2Kword of address space) with the additional capability of operating in byte-wide or word-wide (24-bit) modes.

6.1.7 System Operation

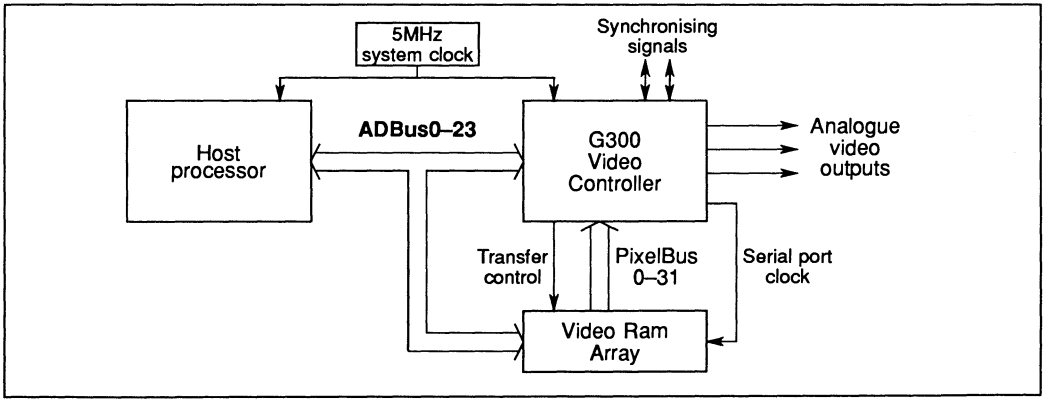


Figure 6.2 IMS G300 operating in a simple graphics system

Figure 6.2 shows how the IMS G300 would fit into a typical single-bitmap display system. The clock is sourced from a 5MHz crystal and the video data is being streamed to the screen at the full video rate of up to 120MHz. The video RAM array is directly accessed by the host and screen management is performed by the G300 on a DMA basis. All external digital signals and clocks are running at one quarter of the video rate.

6.2 Pin function reference guide

6.2.1 Micro port

Pin name	I/O	Page No.	Comments
FrameInactive	O	92	Timing signal which is high whenever the VTG is in Frame Flyback.
BusReq **BusGranted**	O I	88	DMA signals which, along with **Transfer**, supply the timing information to synchronously refresh the video ram shift registers.
ReadnotWrite **notCS**	I I	87	These signals provide all the timing information for accesses as well as defining access type.
ADBus0–23	I/O	87	Multiplexed address and data bus. All 24 bits are used for data; addresses are supplied to **ADBus2-11**. A byte-wide mode is available; the port is also used to drive out the 24-bit VRAM transfer address

6.2.2 Pixel port

Pin name	I/O	Page No.	Comments
notSerialClk **notShiftClk**	O O	93	**notSerialClk** runs at one quarter the video frequency, **notShiftClk** is similar but controls the pixel flow by starting and stopping under the control of the timing generator. Both of these clocks must be buffered.
Transfer	O	88	**Transfer** refreshes the video ram shift register synchronised to **notShiftClk**
PixClkIn	I	95	**PixClkIn** is the Dot-rate clock source when not using the Phase locked loop.
PixDataA0–7 **PixDataB0–7** **PixDataC0–7** **PixDataD0–7**	I I I I	93	The four pixel address bytes are used in the order A, B, C, D. In mode 2 **PixDataD0–7** is not used and RGB maps to ABC.

6.2.3 Miscellaneous

Pin name	I/O	Page No.	Comments
Reset	I	84	Active high, must be held active with clocks running for at least six cycles of **notSerialClk**.

6.2.4 Phase locked loop

Pin name	I/O	Page No.	Comments
CapPlus **CapMinus**	N/A	101	Phase locked loop decoupling pins, also used to select external dot rate clock source by connecting **CapPlus** to **CapMinus**.
PllClkIn	I	101	Low speed clock in the range 5MHz to 9MHz, for multiplication by the Phase locked loop to video dot rate.

6.2.5 Video signals

Pin name	I/O	Page No.	Comments
Red **Green** **Blue**	O O O	95	Blanked video outputs. Drive into doubly terminated 75Ω load.
Iref	I	96	Video DAC reference current.
VSync **CorHSync**	I/O I/O	86	These pins can be used as outputs to supply various software-selectable sync signals or as inputs to lock the device to a system. They are both active high

6.2.6 Supplies

Pin name	I/O	Page No.	Comments
AVdd	N/A	97	**AVdd** supplies analogue portions of chip
Vdd	N/A	97	**Vdd** supplies digital portions of chip
Ground	N/A	102	

6.3 Register function reference guide

Register	Address	Page No.	Comments
Boot Location	#X1A0	87	Startup location to which must be written the clock multiplication factor in PLL mode. Writing to this location sets the Byte counter to zero.
Top of Screen	#X180	88	Read/write register giving ability to reprogram the top of screen pointer at any time.
Control Register	#X160	79	Read/write control register. Read/write accessible at all times, contains all configuration information. Used to start and stop timing generator. Only ADBus[15:0] valid on read, unassigned bits must be written with zero.
Mask Register	#X140	93	Read/write mask register. Read/write accessible at all times, masks each pixel address byte.
Datapath Registers	#X121 to #X12C	80	Read/write registers containing the screen description parameters. These are accessible only when the timing generator is not running.
Datapath Incrementers	#X12D #X12E #X12F	80	Read only incrementers. These are accessible for test purposes only when the timing generator is not running.
Byte Counter	#X100	87	Incrementing counter used in byte access mode. This may be set by writing the current byte number to it. On startup, it is set to zero by the bootstrap routine.
Colour Palette	#X00 to #XFF	93	256 locations of 24 bit colours read/write accessible at all times, programmed via micro port.

All other addresses in the range are reserved and must not be written to.

6.4 The control register and boot location

The bit pattern written to the control register determines the operating mode of the part. The function of each bit is given in table 6.1.

Bit	Function	Comments
23–16	Reserved	Not valid on read, write zero.
15	Turn off blanking	1 = blanking disabled for test 0 = blanking enabled
14	Turn Off DMA	1 = No video RAM management 0 = DMA VRAM update operational
13	Reserved	Write zero
12	Black level	Selects blanking level 0 = Blank = Black level
11–9	Delay value	Delays internal Sync and Blank by 0 to 7 clock cycles
8	Pixel port mode	0 = mode1, 1 = mode2
7	Micro port mode	0 = word mode, 1 = Byte mode
6	Reserved	Write zero
5	Frame flyback pattern	1 = plain synchronising waveform 0 = tesselated synchronising waveform
4	Digital sync format	0 = mixed sync, 1 = separate sync.
3	Analogue video format	1 = video only 0 = video and sync composite
2	Device operating mode	0 = master mode, 1 = slave mode
1	Screen format	0 = non-interlaced, 1 = interlaced
0	Enable VTG	0 = VTG disabled, 1 = VTG running

Table 6.1 Control Register bit allocations

Boot Address	Bit Allocation
#X1A0	**ADbus5–23** = Don't care **ADBus0–4** = Binary coded PLL multiplication factor (when in external clock mode, load zero)

Table 6.2 Boot location bit allocations

6.5 The video timing generator

6.5.1 Introduction

The Video Timing Generator is a programmable finite state machine. It provides composite sync and blanking to the on-chip video DACs, it controls the timing of **BusReq** and **Transfer** and it starts and stops **notShiftClk** to control the flow of pixels onto the screen. It also provides a **FrameInactive** signal which is asserted whenever the display enters frame flyback, enabling the controlling processor to perform frame flipping or major screen updates invisibly.

The timing generator can be configured to control an interlaced or non interlaced monitor and to generate the synchronising waveforms required by the RS170a studio television standard, among others. These options are selectable in software and are controlled by the contents of the control register.
Also controlled by this register is the operating mode of the device; it can be set to free run in which case it will drive synchronising signals out, or it can be set into slave mode when it will lock onto frame and line sync pulses supplied externally.

Programming of the timing generator is achieved by writing a set of screen description parameters to the timing registers. Its resolution is one quarter that of the individual pixels hence the scan lines must be described in 'screen units' of four pixels each (i.e. a line with 1024 pixels is described as having 256 screen units).

6.5.2 The display screen

In a raster scan display system, the picture is built up of a number of visible lines, which are displayed and a much smaller number of frame flyback lines, which are blanked. Each of the displayed lines has a single, visible, display period and a blanked line flyback period made up of front and back porch and line sync. The total linetime is the sum of the displayed and blanked periods.

The frame timing periods are specified in multiples of half a linetime while the line timings are specified in screen units of four pixels duration each.

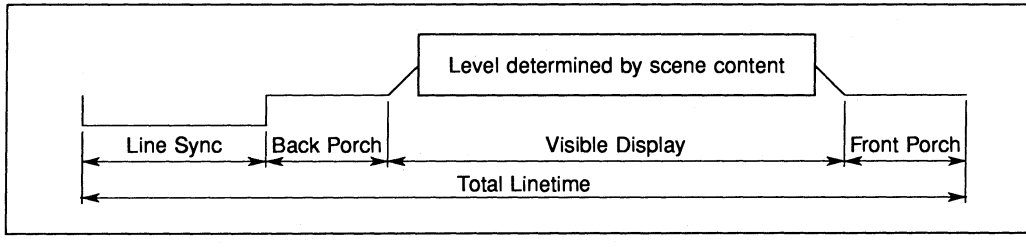


Figure 6.3 Scan line segments

Each displayed scan line of the raster is built up of the sections shown in figure 6.3. The visible portion is contained within the period 'display', so that, if a screen width of 1024 visible pixels is required, this number is reflected in the screen description parameter written to the 'display' register.
At all other times, the display is in line flyback and is therefore blanked.

The total linetime is the sum of all the sections of figure 6.3 and this is the number written to the 'linetime' register.

6.5.3 Line timing parameters

The line segments shown in figure 6.3 are used directly to program the timing generator with two exceptions. First, the line synchronising pulse is split into two states of equal duration which are used in immediate succession — the parameter used for this is 'halfsync'— and second, there is no programmed delay for frontporch, rather the total line time is programmed into a separate register and the machine is reset to line state 'Halfsync1' when this timebase period expires. The resulting flexibility in the duration of frontporch makes the device very easy to program and is essential when it is used as a slave. Any jitter in the global sync is taken up in this front porch period.

Figure 6.4(a) shows the flowchart of a standard displayed or blanked scan line (as distinct from the truncated unscanned lines used in vertical sync and equalisation). The state machine proceeds from one state to the next according to the delay programmed in by the user; on entering a new state the Sync and blanking outputs are modified depending on what part of the cycle is being executed.

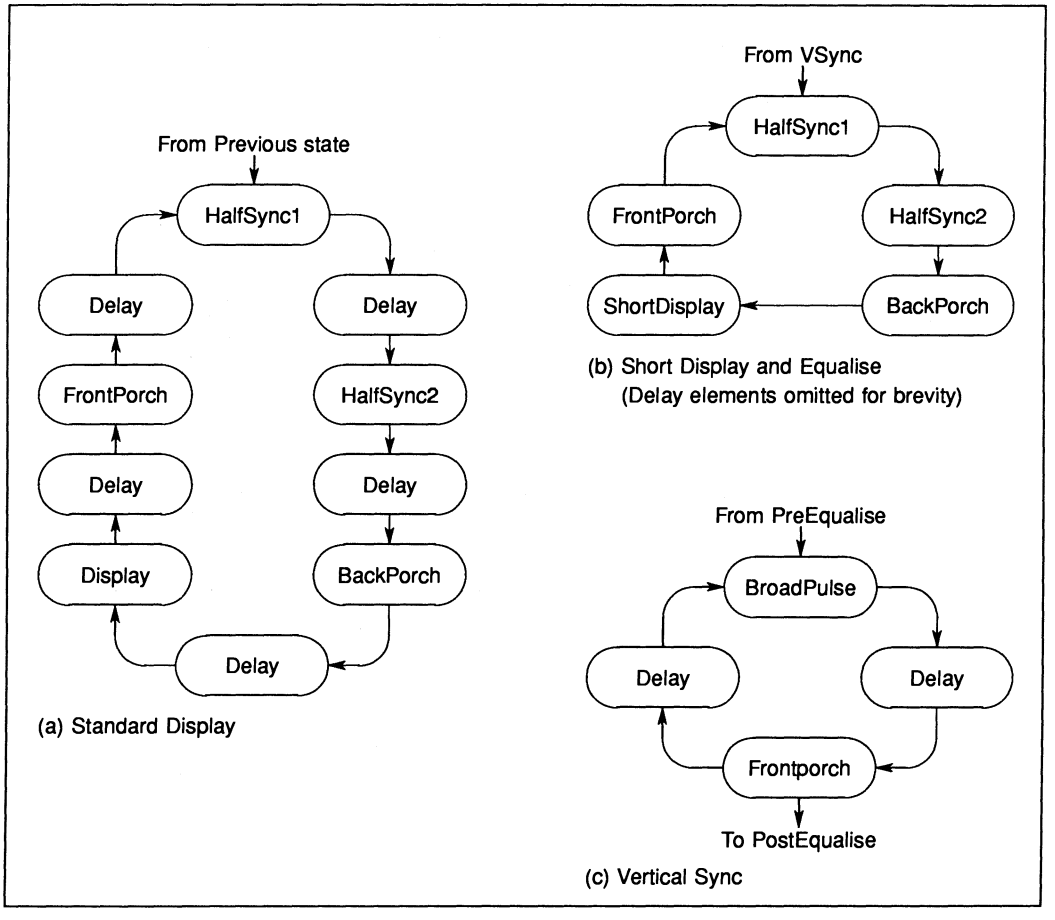


Figure 6.4 Flow diagrams for video timing generator

Figure 6.5a shows the relationship of the screen description parameters to a full scan line. Note that frontporch is undefined and halfsync is used twice in succession to construct the line sync pulse.

6.5.4 Frame timing parameters

The G300 generates synchronising signal timings and levels conforming to both broadcast and closed circuit television standards. This means that, as well as being capable of generating the ordinary frame sync patterns associated with non-interlaced computer graphics systems, it is also able to produce tesselated sync signals for an interlaced television system (see figure 6.6).

A further requirement of the television standards is that each frame may contain an odd number of scan lines. As a result, the frame timing parameters need to be specified in terms of half line times. Thus a non-interlaced screen of 1024 visible lines has the value 2048 written to the VDisplay register. (An interlaced screen of that

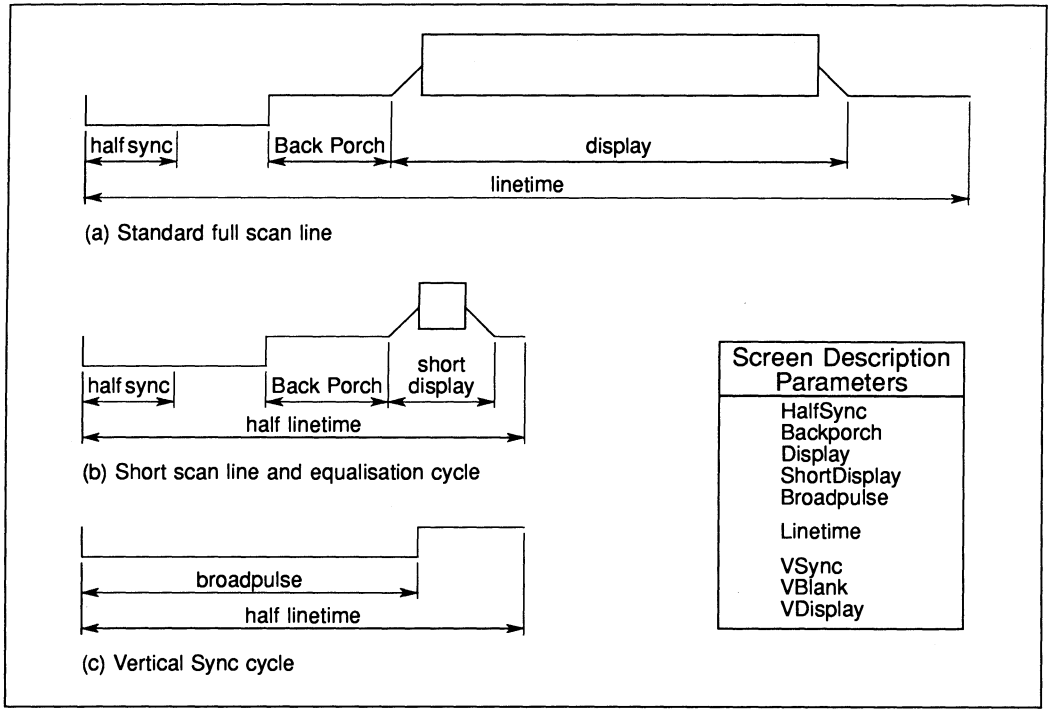


Figure 6.5 Screen description parameter definitions

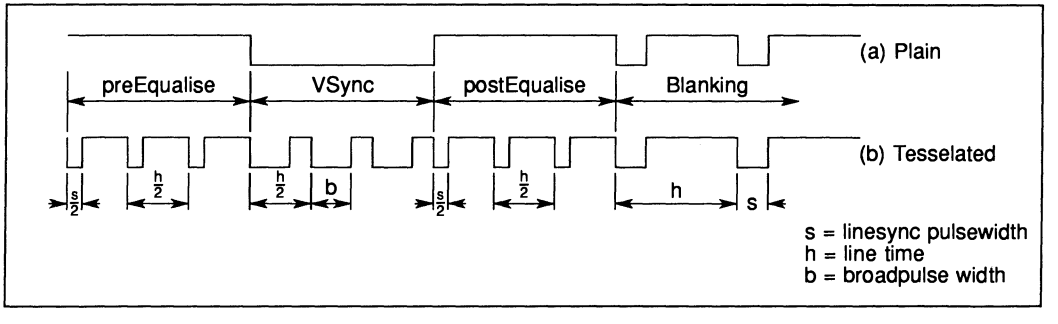


Figure 6.6 Composite Sync Frame Flyback Waveforms

size would have 1024 in that register since in interlace, the VDisplay register decribes the vertical display field rather than the entire frame — see table 6.3).

The duration of preEqualise, postEqualise and VSync are all set by the VSync parameter and are hence always equal, the blanking period is independent and has its own parameter, Vblank.

In order to generate the tesselated equalisation and blanking waveforms shown in figure 6.6(b), some additions to the basic line parameters are needed. The low period during VSync is defined as 'broadpulse' with its duration stored in the 'broadpulse' register. The shorter low period during pre and post equalisation is equal to half the line sync period and hence uses the value stored in the 'halfsync' register.

Screen Type	Lines per Frame	Value in VDisplay Register	Lines per Field
non-Interlace	1024	2048	1024
Interlace	1024	1024	512
non-Interlace	625	1250	625
Interlace	625	625	312.5

Table 6.3 Frame Programming examples

Reference to figure 6.4(b) and (c) shows that, on entering frame flyback, the state machine loop shortens to give a period of half a linetime. In equalisation, this is achieved simply by substituting 'shortdisplay' for 'display' in the sequence, whereas in vsync the sequence is changed to include only 'broadpulse' and 'frontporch'.

6.5.5 Parameter calculation

Calculation of the frame timing parameters is obvious and direct — to produce the flyback waveform in figure 6.6(a) the parameter VSync is set to 3 — and the line parameters are easily derived from the equations in table 6.4.

During a full line cycle (VBlank, VDisplay)		
Halfsync	=	Horizontal Sync/2
BackPorch	=	Backporch
Display	=	Display
FrontPorch	=	Linetime – (2*HalfSync + BackPorch + Display)
During an Equalisation Cycle		
Low period	=	HalfSync
ShortDisplay	=	LineTime/2 – (2*HalfSync + BackPorch + FrontPorch)
High period	=	HalfSync + BackPorch + ShortDisplay + FrontPorch
FrontPorch	=	Linetime/2 – (2*HalfSync + BackPorch + ShortDisplay)
During a VSync cycle		
Low Period	=	BroadPulse
High period	=	FrontPorch
FrontPorch	=	Linetime/2 – BroadPulse

Table 6.4 Screen description parameter equations

The following restrictions on parameter values must be observed:

- All parameters must be non-zero.
- Linetime must be an even multiple of the period of notSerialClk.
- The Halfline point must fall within active display period with at least one notSerialClk period of display on either side of it.
- The total number of displayed lines in each frame must be a whole number. (Note that this means each field of an interlaced frame may have a half line in it)
- The Vertical blanking period must be a whole number of lines.

- Backporch must exceed TransferDelay by at least one notSerialClk period.
- TransferDelay must not exceed ShortDisplay.

(The parameter TransferDelay is described in section 6.8)

6.5.6 The startup sequence

Reading from and writing to the VTG registers, which are memory mapped, is accomplished while the timing generator is disabled.

On startup, after reset, the host processor must write a configuration pattern to the G300 bootstrap location. The effect of this is to set the PLL multiplication factor, if the G300 is to be used in PLL mode, and to set the micro port into a usable state, independent of whether word or byte accesses are to be used. Following this write it must set the micro-port mode by writing to the relevant bits in the control register.

Startup sequence:

1 Assert, then deassert **Reset**.

2 Write configuration pattern to bootstrap location.

3 Write to control register to set microport to desired state.

After this the screen parameters and colour table data can be written to the appropriate locations in any order. The processor must then make another write to the control register to enable the VTG.
It will then either start up immediately at the beginning of frame sync, or wait in Pre-Equalise frontporch for an external sync pulse, depending on the mode to which it has been set. In master mode, it will free run, producing all sync pulses internally, whereas in slave mode, it will lock onto an external sync, resynchronising at the start of each line and at the start of each frame.

Normally the screen parameters are set by the host as part of a powerup sequence and do not change subsequently but there is nothing to prevent the user redefining the screen as often as necessary while the display is being used.

The reprogramming sequence has three steps;

1 Write to the control register, disabling VTG.

2 Write to screen parameter registers chosen for redefinition.

3 Write to the control register, redefining modes if necessary and enabling VTG.

If only the operating mode is to be changed, step 2 only may be omitted, the remainder of the address space is programmed without disabling the VTG. If the clock multiplication factor is to be changed, **Reset** must be asserted first.

6.6 The G300 Address Map

The various register locations of the IMS G300 are memory mapped as shown in the table below. The values given are hexadecimal word addresses driven on to **ADBus2–11** All other locations within the address space occupied by the G300 are reserved and must not be addressed. The datapath incrementers are read only, The boot location is not readable, all other locations are read/write.

Location	Address
Colour Palette	
starts	#X000
ends	#X0FF
Byte Counter	#X100
Mask Register	#X140
Control Register	#X160
Top of Screen	#X180
Boot Location	#X1A0

Location	Address
DataPath Registers	
HalfSync	#X121
BackPorch	#X122
Display	#X123
ShortDisplay	#X124
BroadPulse	#X125
VSync	#X126
VBlank	#X127
VDisplay	#X128
Linetime	#X129
LineStart	#X12A
MemInit	#X12B
TransferDelay	#X12C
Datapath Incrementers	
HIncrementer	#X12D
VIncrementer	#X12E
TBIncrementer	#X12F

Table 6.5 IMS G300 Address Map

6.7 Synchronising signals

6.7.1 Introduction

The video timing generator produces Sync and blank signals to a pattern specified by a combination of the operating mode of the G300 and the screen description parameters. Internally, composite sync and composite blank are supplied to all three video DACs by default. However, both of these functions can be disabled by setting the relevant bits of the control register.

The internal sync and blank signals are supplied with the correct delay to allow for the transfer of data from the video ram array into the G300 and the difference in delay due to the alternate operating modes is automatically catered for.

In order to allow a certain amount of system flexibility, the IMS G300 includes a programmable delay line which can be set (via the Control Register) to insert a further delay of up to seven clock cycles between the outputs of the VTG and the inputs of the DACs.
This enables the system designer to insert pipeline stages between the video ram array and the G300 for the implementation of cursor or text overlay, etc and also allows video data to be buffered along a backplane using TTL parts.

6.7.2 Master mode

When running in master (internal sync) mode, the **VSync** and **CorHSync** pins are outputs and the G300 drives them in the appropriate fashion, active high. Composite or Horizontal sync selection is specified in the Control Register. Untesselated frame sync always appears on the **VSync** pin while the **CorHSync** pin is switchable to supply one of Line sync, untesselated composite sync or tesselated composite sync (see table 6.6).

Control Bits		**Vsync**	**CorHSync**	
			HSync	*CSync*
4	5			
0	0	Plain	–	Tesselated
0	1	Plain	–	Plain
1	0	Plain	Plain	—
1	1	Plain	Plain	—

Table 6.6 Sync Style Selection

6.7.3 Slave mode

In slave mode the **VSync** and **CorHSync** pins are designated as inputs and the G300 will lock onto vertical and horizontal sync pulses supplied to them. The system must provide both horizontal and untesselated vertical sync, active high.

The sampling circuit on the Sync inputs means that the IMS G300 can be locked to a completely asynchronous source without metastability problems. It will tolerate a large amount of instantaneous variation in the synchronising inputs due to the inbuilt flexibility of the timing algorithm. This provides synchronisation guaranteed to within one period of **notSerialClk**, which may not be adequate in a system where the monitor and G300 are synchronised separately from a single external source; because of possible jitter on the sync signal there may be random errors visible on the screen. In this case, it is necessary to observe the timing shown in figure 6.7 in which case, the G300 will give no synchronising errors.

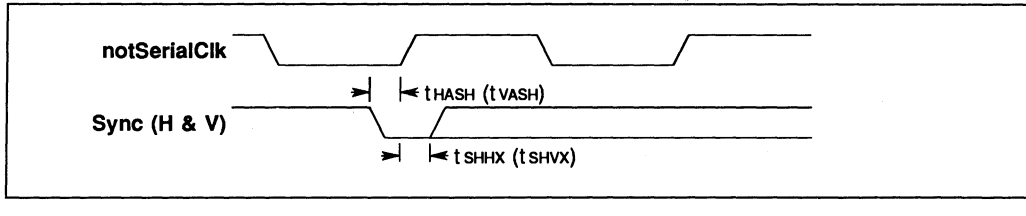


Figure 6.7 External synchronisation

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tVASH	Vsync setup time	SClk/4		ns
tHASH	Hsync setup time	SClk/4		ns
tSHVX	Vsync hold time	0		ns
tSHHX	Hsync hold time	0		ns
Note: These figures are not characterised and are subject to change				

Table 6.7 External sync waveform timings

6.8 The Micro-port

6.8.1 Introduction

The micro-port is a bidirectional 24 bit interface which can be configured to operate in byte wide or 24 bit wide mode (word mode). It consists of a multiplexed address and data bus with several control signals, described below, and is used for programming both the video timing generator screen description registers and the colour lookup table. The micro port timings are asynchronous with the remainder of the G300.

As well as serving as a programming port the interface is also capable of performing a video RAM shift register transfer operation using a fully handshaken DMA. The timing of this operation is synchronous with the pixel port and is arranged so that seamless update of the video RAM shift register is possible.

6.8.2 Initialisation

The choice of clock source is made by a wiring option. If the phase locked loop is to be used, a suitable crystal oscillator must be connected to the **PllClkIn** pin. If the direct drive option is used, the system must supply a dot rate clock to the **PixClkIn** pin. On Power up, the **Reset** pin must be taken high and PllClkIn or PixClkIn must have been running for at least t_{CVRL} after **Vdd** is valid before the end of **Reset**. After deasserting **Reset**, the first access to the Micro-port must be a preliminary configuration access to the boot location as specified in section 6.5. This sets the micro-port byte counter and the PLL multiplication factor if the clock source is to be the PLL.

Following this, a write should be performed to the control register to set the width of the programming port — byte or word. The option is selected by writing to bit 7 in the control register. (Since this is in the lowest byte of the control word, the value is guaranteed to be set correctly with one write cycle). If byte-wide mode is selected, a further two writes to the control register must be made to complete the cycle.

Once these two write cycles have been performed normal operation of the micro-port may commence using the programmed format whether it be byte-wide or 24-bit word-wide.

6.8.3 Programming operation

For normal read and write cycles the address is latched into the G300 on the falling edge of **notCS**. **ReadNotWrite** is sampled 1/2 a period of **notSerialClk** later to establish the cycle type. In a read cycle, the data lines will be driven a certain time later and will remain valid until **notCS** goes high. In a Write cycle, data will be latched into the G300 on the rising edge of either **ReadNotWrite** or **notCS**, whichever occurs first. When the part is configured to byte-wide mode, three complete read or write cycles must be made to the same address in order to complete the cycle. The data is written to or read from **ADBus0–7** least significant byte first. If a byte wide cycle is aborted before completion, the counter must be reset by writing the number one to the byte counter register. If the aborted cycle happened to be a write, data corruption at the written location will occur.

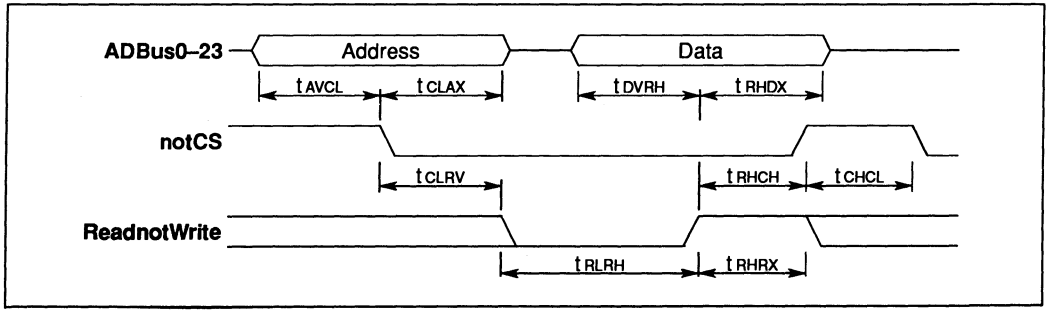


Figure 6.8 Micro-Port Write Cycle

Symbol	Description	Min	Max	Units
t_{AVCL}	address setup time	20		ns
t_{CLAX}	address hold time	10		ns
t_{CLRV}			0.5	periods SClk
t_{CHCL}		1		period SClk
t_{DVRH}	data setup time	0		ns
t_{RHDX}	data hold time	20		ns
t_{RHCH}		0		ns
t_{RLRH}		3		periods SClk
t_{RHRX}		1		period SClk
t_{CLCL}	cycle time	5		periods SClk
where SClk is the period of **notSerialClk**				
Note: These figures are not characterised and are subject to change				

Table 6.8 Write cycle parameters

6.8.4 The screen transfer operation

The G300 provides two software programmable strobes which enable it to perform the necessary screen data-transfer cycles on video RAMs to reload the internal shift registers with new data. These may be synchronous updates which happen part way across a line or updates which occur during flyback.

The user may program these strobes, **busRequest** and **Transfer**, to cause the data transfer cycles to occur at the correct points during the screen display to implement seamless line update, thus decoupling the screen configuration from dependence on the video RAM architecture. These strobes are controlled by values loaded into two special purpose registers, MemInit and TransferDelay. The G300 also outputs a transfer address specifying the new row of pixels to be displayed. It is left to the user to generate RAS, CAS and any other strobes he may need from **busRequest**, **Transfer**, **notSerialClk** and **notShiftClk**.

The G300 is primarily designed to be used with video RAMs, although it can be used with static or standard dynamic rams if desired. In this case the strobes provided can be used to arbitrate bitmap accesses.

6.8.5 The transfer address

The G300 outputs a new 22 bit address on **ADBus2–23** during every transfer cycle it initiates. The first address in each frame is specified in the Top of Screen register, which is programmed on startup but which can be modified at any time.

Unless a new address is supplied by the host, the current row address will be incremented by the G300 and used for the next row transfer until the bottom of screen is reached. The address counter is then reset to Top of screen unless the G300 has been set to interlace mode, in which case the address will carry on being incremented until both fields of the frame have been displayed. The effect of this is to separate out the fields of an interlaced image into two consecutive bitmaps as shown in figure 6.9.

The address will be incremented as one 22-bit number in bits 2–23 and it is left to the user to split this into row and column fields for strobing into the video RAMs. Ordinarily the bottom n-bits of the address would be used as a row value and the top bits for the column value as shown in table 6.9

It is open to the user to modify either or both of these fields at any time (other than during a row transfer operation) so that panning and scrolling can be implemented.

Row Address Field	Col Address Field
ADBus 2 to n–1	ADBus n to 23

Table 6.9 Shift Register Transfer Address Fields

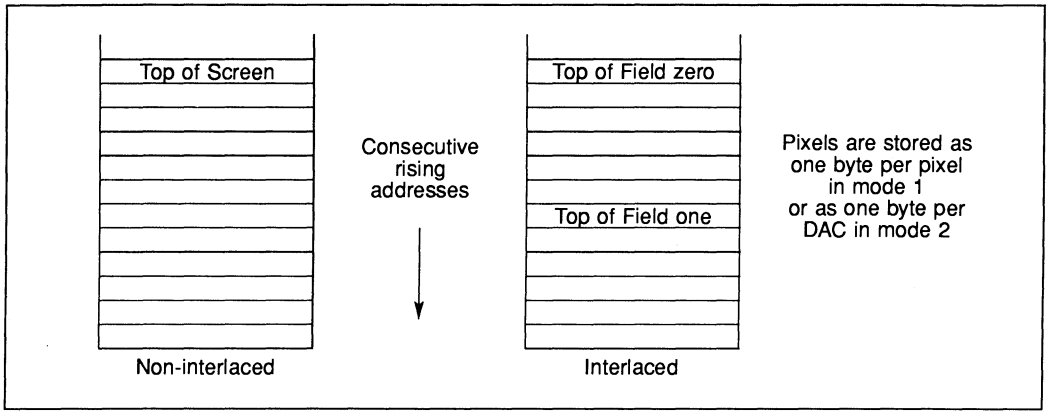


Figure 6.9 Bitmap Formats for interlaced and non Interlaced displays

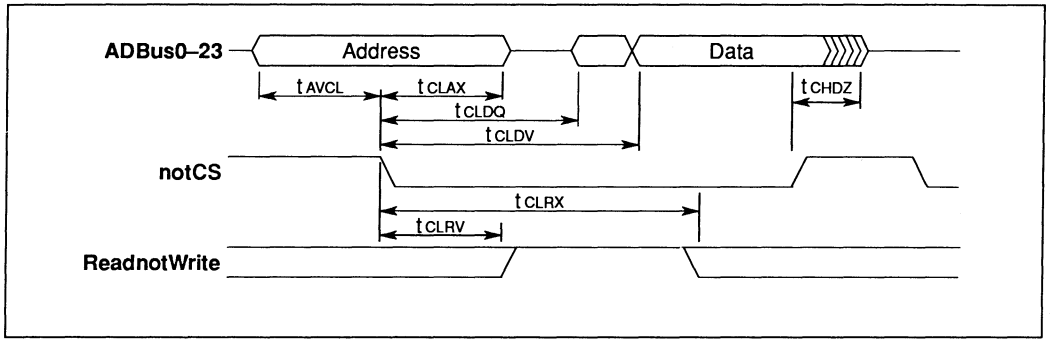


Figure 6.10 Micro-Port Read Cycle

Symbol	Description	Min	Max	Units
tAVCL	address setup time	20		ns
tCLAX	address hold time	10		ns
tCLDQ	time to bus driven	1.5		periods SClk
tCLDV	data access time		4sClk + 20nS	
tCLRV			0.5	periods SClk
tCLRX		1.5		periods SClk
tCHDZ	data turn off delay		20	ns
tCLCL	cycle time	7		periods SClk
where SClk is the period of **notSerialClk**				
Note: These figures are not characterised and are subject to change				

Table 6.10 Read cycle parameters

6.8.6 Transfer cycle timing

Video RAMs reload their shift registers by performing a normal read cycle with a special pin (usually called notDT or notDT/notOE) held low as RAS falls. The address values presented to the VRAM on the falling edges of RAS and CAS define which row is loaded into the shift register and which bit in the shift register is shifted out first, respectively. The instant at which the actual transfer takes place is set by the time at which

notDT is brought high again and this edge alone must be synchronised to the shift clock which clocks data out of the shift registers.

In many systems the reloading of the shift registers takes place at the end of the line during retrace. However, one of the most useful features of using the G300 with VRAMs is the ability to reload the shift registers mid-line. This allows screens with an arbitrary number of pixels per line to be constructed with any length shift register. In order to do this however some look-ahead is required in order to be able to make the transfer at exactly the right point without any discontinuity on the screen. This look-ahead is provided by programming the appropriate values into the MemInit and TransferDelay registers.

At the start of each display frame, the G300 will initiate a transfer cycle at the beginning of the backporch period of the first line and will perform the data transfer with the delay specified in the TransferDelay register.

The G300 has the following requirement:

$$\text{TransferDelay} \leq \text{BackPorch} - 1$$

This ensures that there is data loaded ready for the first line scan to begin.

The G300 will then begin to count **notShiftClk** cycles and will initiate a further transfer cycle after MemInit cycles of **notShiftClk** by asserting **BusReq**. After a further number of cycles of **notShiftClk** equal to TransferDelay, the G300 will take **Transfer** low and the new data will be loaded into the shift registers.

Thus the period of row transfer operations is

$$\text{MemInit} + \text{TransferDelay}$$

and apart from the restriction quoted above, it need bear no relation to the screen line length at all. This permits any display line length with any type of video RAM.

The critical parameter as far as DMA accesses are concerned is TransferDelay which needs to be long enough to allow for the DMA latency of the controlling processor as well as the access time of the video RAMs. The G300 imposes an extra overhead of one notSerialClk period which needs to be added to the Transferdelay parameter but which does not appear as part of the delay between BusReq and notDataTransfer. Thus:

$$\begin{aligned} \text{TransferDelay} = {} & \text{System DMA Latency} \\ + {} & \text{VRAM Access time} \\ + {} & \text{SClk} \end{aligned}$$

If there is a data transfer operation pending when the system enters flyback, (i.e. the G300 would have control of the bus for a considerable length of time) then the transfer cycle is aborted before **BusReq** is made and will be restarted on the next following active display backporch. This ensures that any DRAM is never left unrefreshed during frame flyback and also makes best use of the available memory bandwidth. In order to implement this function, the G300 predicts, after a DMA is internally sheduled but before BusReq is asserted, that the video RAM shift registers are not going to run out of pixels before the end of the current line and hence the Row refresh may be left until the following active backporch. The internal system is pipelined by one delay stage which is the reason for adding one **notSerialClk** cycle extra to the TransferDelay parameter over the actual DMA latency of the system. When **BusReq** is rescheduled the DMA is restarted at the beginning of backporch in the same way as the first line in the frame but the transfer delay parameter is carried over from the previous line (or frame) and is incremented only when the system re-enters active display. This preserves the correct ordering of data onto the screen, while the insertion of the backporch period ensures that the DMA latency is always exceeded.

Figure 6.11 shows the sequence of events during a synchronised VRAM row transfer operation performed by the G300 which takes place part-way along a display line. That is to say an uninterrupted stream of pixels is maintained during a reload of the shift registers.

It should be noted that the G300 signals **notShiftClk**, **notSerialClk** and **Transfer** are all designed to be buffered by inverting buffers outside the G300 and so are the logical inverses of the signals driving the VRAMs.

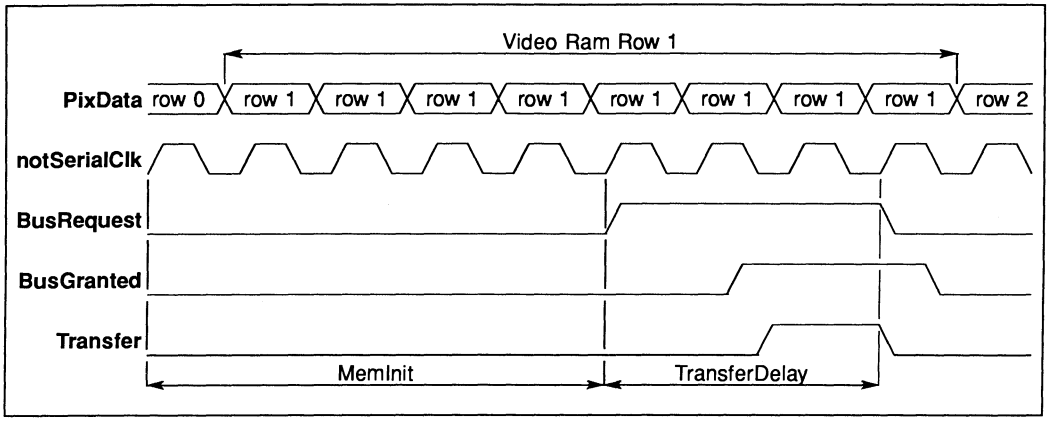


Figure 6.11 Data Transfer Sequence

MemInit defines the number of periods of **notShiftClk** before the G300 asserts **busRequest**. This is the first event which signals the start of a transfer cycle. When the host processor returns **busGranted** the G300 asserts **Transfer** and drives out the new transfer address to be strobed into the VRAMs. Only after a further number of **notShiftClk** cycles equal to TransferDelay, does the G300 remove **Transfer** (synchronously with respect to **notShiftClk**) and so perform the actual transfer. **busRequest** is also taken away at this point to return the **ADBus** back to the host. The user should arrange for TransferDelay to be sufficiently long to allow for the worst case bus request latency plus the time required to strobe RAS and CAS with the address supplied from the G300.

The most memory-efficient way of using the transfer cycle feature is to make Meminit + TransferDelay equal to the length of the video RAM shift registers thus packing the bitmap into the smallest possible space, but it is obviously possible to specify a smaller number and then use the remainder of the bitmap as a larger 'world' which can be panned through by modifying the Top of screen pointer between frames.

The G300 will not respond to a BusGranted signal which it has not itself requested. This feature simplifies connection into a system which includes more than one DMA source.

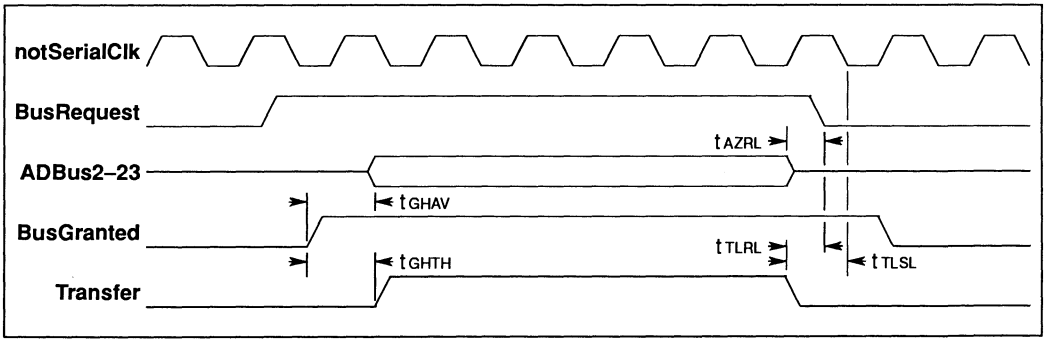


Figure 6.12 Data Transfer Timings

Symbol	Description	Min	Max	Units
t_{GHAV}	**busGranted** high to address valid		3*SClk+30	ns
t_{AZRL}	Address invalid to **busRequest low**	0		ns
t_{GHTH}	**busGranted** high to **Transfer** high		SClk+20	ns
t_{TLRL}	**Transfer** low to **Bus Request low**	−5	5	ns
t_{TLSL}	**Transfer** low to **notSerialClk** low	10	SClk−10	ns
Note: These figures are not characterised and are subject to change				

Table 6.11 Micro port DMA and Transfer timings

6.8.7 FrameInactive

A further timing signal, **FrameInactive**, is provided which can be used to convey frame timing information to the host. This signal may be used in multiboard systems where frame swapping is used to implement animation, for example. **FrameInactive** is asserted whenever the timing generator enters frame flyback and is deasserted on entering active display.

6.9 The pixel ports

6.9.1 Pixel port operation

The pixel port takes in the pixel data from the video RAM and has two modes of operation;

mode 1 — via the lookup table
mode 2 — direct write through to the DACs.

The mode is defined by a single bit in the G300 control register. The clock source is set by a wiring option (See the section on the programming interface). By varying these options it is possible to use the G300 in one of three configurations as shown in table 6.12

Mode	Clock Option	Video Clock Source	Pixel Route
1	**pllClkIn** (nom 5MHz)	output of on-chip PLL	through LUT
1	**pixClkIn** (video rate)	**pixClkIn**	through LUT
2	**pllClkIn** (nom 5MHz)	not available	
2	**pixClkIn** (video rate)	**pixClkIn**	direct to DACs

Table 6.12 Clock and pixel port options

6.9.2 Mode 1 operation

In mode 1 the G300 latches four 8-bit pixels on **PixDataA0–7**, **PixDataB0–7**, **PixDataC0–7** and **PixDataD0–7** on a single falling edge of **notShiftClk**. These four pixels are then serialised to the full pixel rate internally and applied to the colour palette address inputs in turn — A, B, C and D.

The eight bit pixels used in mode 1 allow a choice of 256 simultaneous colours from a palette of 16 million. Changing the palette through the programming interface allows rapid colour selection and modification. The colour palette may be loaded and read back via the programming interface (see the G300 memory map). If the G300 memory interface is being used in word-mode, then a colour word may be loaded in one G300 external memory interface cycle and a complete colour palette may be block moved into or out of the G300 by the processor.

Mode 1 allows the pixel input to be multiplexed 4 into 1, this allows clocking of the video RAMs at 1/4 the pixel clock frequency.
The G300 supplies a signal **notShiftClk** which is designed to be buffered through a single inverting driver outside the G300 directly into the SC (serial clock) of each of the video RAMs. This clock (which runs at 1/4 the pixel clock frequency) pulses once for each new group of 4 pixels required by the display. It is not free running, but stops during line and frame flyback.
A free-running clock **notSerialClk** is also generated by the G300. This provides a continous clock synchronous to the video stream. If this clock is loaded identically to **notShiftClk** then its edges will be coincident to **notShiftClk**, the only difference being that it will not stop during flyback.

By taking 4 pixels into the G300 in one go, the clock rate to the video rams for a nominal 120MHz system can be reduced to 30MHz. It is therefore possible to use standard video RAMs without extra multiplexing on the board. It is also possible to drive the pixel data down a backplane using easily available TTL parts in order to gang up extra boards in a distributed system. It has the further advantage that all external clocks and signals are running at comparatively low frequencies.

A memory mapped mask register is available for masking the incoming pixel address to the LUT in mode 1. The contents of this register (mapped onto **ADBus0–7**) are logically ANDed with the incoming pixel stream. By altering the contents of this register the microprocessor may achieve simple rapid colour changes on the screen.

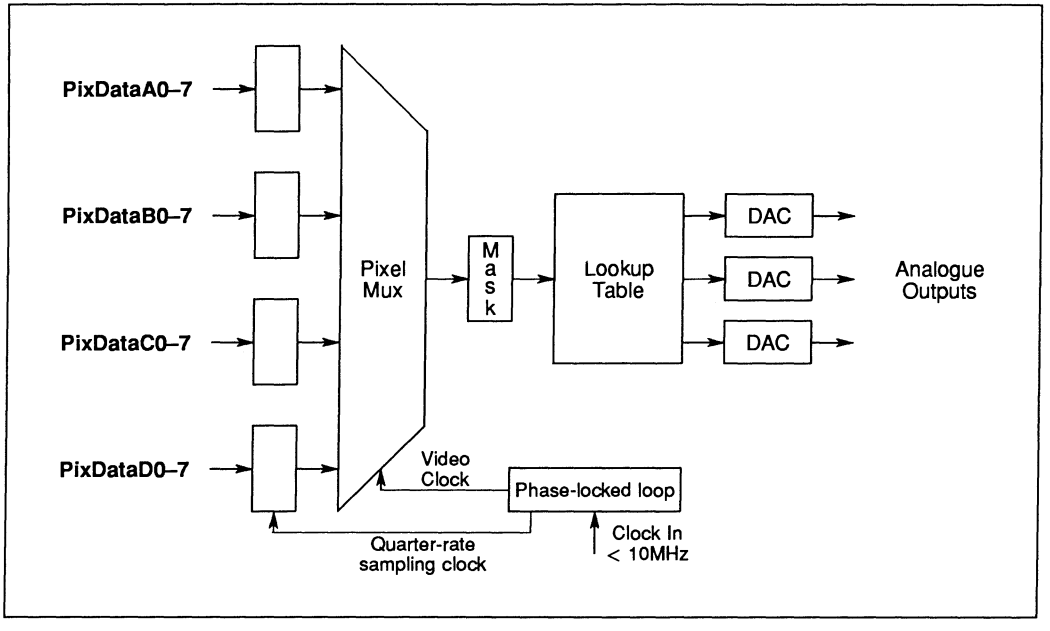


Figure 6.13 Pixel Port in mode 1

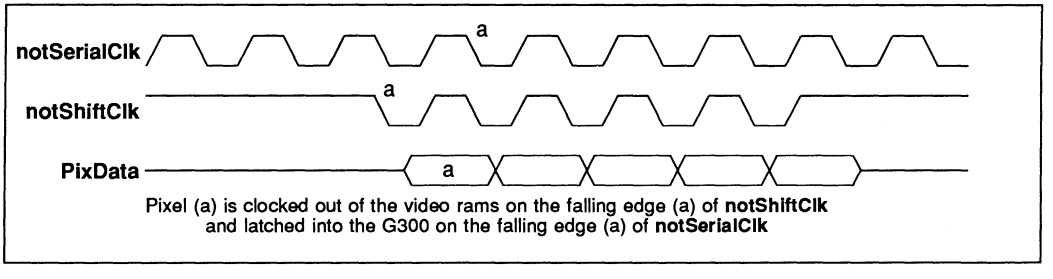


Figure 6.14 Relationship of Serial and Shift Clocks to pixel data

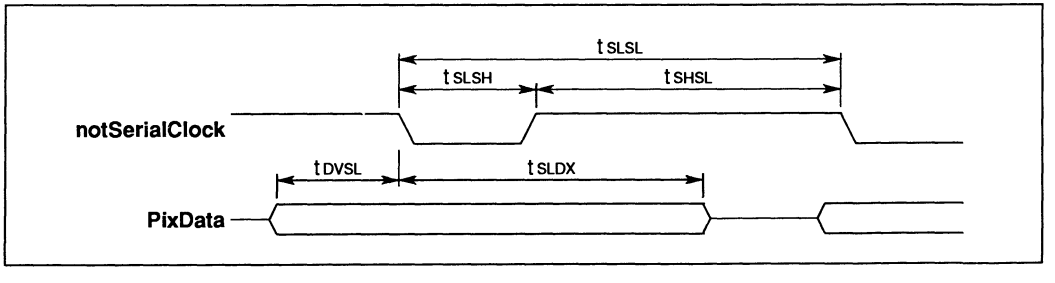


Figure 6.15 Pixel Port signals in mode 1

Symbol	Description	-66 Min	-85 Min	-100 Min	-110 Min	Units
t_{SLSL}	notSerialClk period	61	47	40	36	ns
t_{SLSH}	Clk low time	12	10	10	10	ns
t_{SHSL}	Clk high time	12	10	10	10	ns
t_{DVSL}	data setup time	3	0	0	0	ns
t_{SLDX}	data hold time	25	20	18	15	ns
Note: These figures are not chracterised and are subject to change						

Table 6.13 Pixel port mode 1 timings

6.9.3 Mode 2 operation

In mode 2, direct write, pixel inputs are applied direct to the DACs so bypassing the LUT. This allows the use of the full range of up to 16 million colours simultaneously displayed on the screen but requires pixels to be supplied to the G300 at the full video rate.

One 24-bit wide pixel is latched into the G300 on every *rising* edge of the externally supplied pixel clock — **pixClkIn**. (The PLL is not used in mode 2.)
PixDataA0–7 feeds the red DAC, **PixDataB0–7** feeds the green DAC and **PixDataC0–7** feeds the blue DAC. The DAC outputs will then reflect this pixel data directly on their respective analogue outputs.

Note that in both modes, the specified timings for the pixel setup and hold times must be observed, even during flyback.

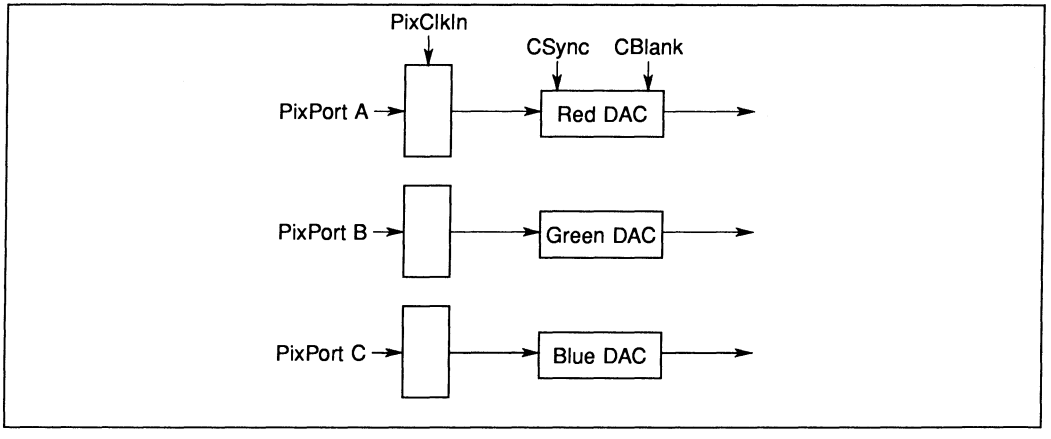


Figure 6.16 Pixel port in mode 2

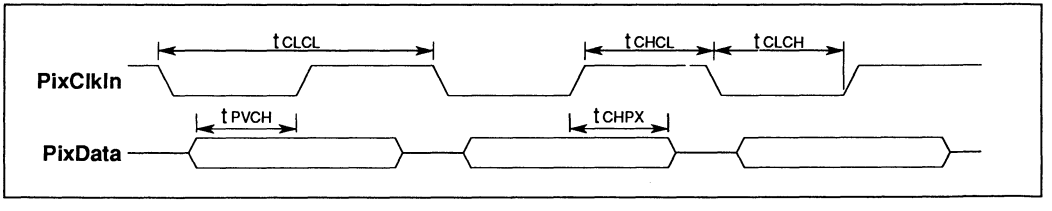


Figure 6.17 Pixel Port signals in Mode 2

Symbol	Description	All Max	-66 Min	-85 Min	-100 Min	-110 Min	Units
t_{CLCL}	pixel period	10000	31	25	20	18	ns
t_{CHCL}	pixClkIn high time	10000	10	8	7	6	ns
t_{CLCH}	pixClkIn low time	10000	10	8	7	6	ns
t_{PVCH}	pixel data setup time		6	5	4	4	ns
t_{CHPX}	pixel data hold time		6	5	4	4	ns
Note: These figures are not chracterised and are subject to change							

Table 6.14 Pixel Port Mode 2 Timings

6.10 The video DACs

6.10.1 General

The video DACs on the G300 have 8-bit resolution at the full video rate. They are designed to drive a doubly terminated 75Ω transmission line and produce analogue video signals compatible with either the RS-170 or RS-343 video standards.

6.10.2 DAC output waveform

The DACs work by sourcing a current proportional to their digital input. The unit current sourced for each digital increment is defined by a reference current drawn from the part using an external current source.

The complete analogue video signal comprises three components as shown in figure 6.20. The current sourced by each component is defined in terms of DACunits. The value of 1 DACunit is set by the reference current drawn from the **Iref** pin :

$$1\ \text{DACunit} = \textbf{Iref}/120$$

The colour information output by each gun ranges from 0 to 255 units under control of the digital input from the colour palette or the pixel port.

A black-level pedestal of 20 DACunits is provided. This extra pedestal distinguishes between a displayed value of intensity 0 during display (ie black) and the 'blacker than black' level present when the electron beam is blanked for flyback. When enabled (by setting the relevant bit in the control register), this extra level is switched on only during the active display time of each line. It is switched off during blanking so as to ensure no visible trace of the beam appears on the screen during this period.

A sync pedestal, again selected using the control register, is provided to allow the superposition of the sync timing signals on the video outputs. When this composite sync option is selected the sync level is added to the output during blanking and active display. Sync pulses are present on all three of the video DACs. The size of the sync pedestal is 108 units.

Table 6.15 defines the value of each of the three components which make up the complete video output current sourced by each DAC.

Both the black-level pedestal and the sync signals may be independently turned on or off by setting bits 12 and 3 in the control register respectively.

(Note that the extra blanking pedestal units, if used, add to the full scale deflection so that the current source must be redefined in order to use this mode).

6.10.3 DAC characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES (1,2)
	Resolution		8		bits	
VO(max)	Output voltage			1.5	V	IO ≤10mA
IO(max)	Output current			−32	mA	VO ≤1V
	Full scale error			±5	%	3
	Sync pedestal error			±10	%	
	Black level pedestal error			±10	%	
	DAC to DAC correlation error			±2.5	%	4
	Integral Linearity error			±1	LSB	5
	Glitch Energy		75		pVSec	6,7
IREF	Reference current	−7		−10	mA	
VREF	Reference voltage	VDD−3V		VDD	Volts	
Note: These figures are not characterised and are subject to change						

Notes

1 All voltages with respect to **Ground** unless specified otherwise.

2 Tested over the operating temperature range and at nominal supply voltage with IREF = −8.88mA.

3 From the value predicted by the design equation, sync and black level pedestals off.

4 About the mid point of the distribution of the 3 DACs measured at full scale deflection.

5 Linearity measured from the best fit line through the DAC characteristic. Monotonicity guaranteed.

6 Load = 37.5Ω + 30 pF with IREF = −8.88mA.

7 This parameter is sampled not 100% tested.

SYMBOL	PARAMETER	−66 MAX	−85 MAX	−100 MAX	−110 MAX	UNITS	NOTES
	DAC Risetime	6	6	4	4	ns	1
	DAC Settling Time	15.3	11.7	10	9.1	ns	1,2,3
Note: These figures are not characterised and are subject to change							

Notes

1 Load = 37.5Ω + 30pF, IREF = −8.88mA.

2 From a 2% change in output voltage until settling to within 2% of the final value.

3 This parameter is sampled not 100% tested.

6.10.4 Power supply and reference current

The DACs in the G300 draw current from a positive supply pin designated **AVdd** (analogue VDD). This pin is separate from the rest of the positive supply pins to the G300 which power the digital circuitry. It is recommended that a high frequency decoupling capacitor (preferably a chip-capacitor) in parallel with a larger tantalum capacitor (22μF to 47μF) be placed between **AVdd** and **Ground** to provide the best possible supply to the analogue circuitry of the DACs.

In cases where the positive supply local to the G300 is unavoidably noisy, an inductor may be placed in series with the entire positive supply to improve the local supply to the G300. If this approach is taken however, care should be taken to ensure that there is no significant DC voltage drop across the inductor during operation.

The G300 requires a simple current source to provide a reference current for the DAC outputs. This current

is drawn from the positive rail. The principle considerations when choosing a current source for a video DAC are accuracy, stability and a fast AC response.

Figure 6.18 shows a recommended current source based around the LM334 precision current reference. The device is used in its temperature compensated mode. This device can supply reference currents up to 10mA. the resistor RSET sets the basic current drawn, with the second resistor R1 and the silicon diode (IN4148) providing temperature compensation.

The component values shown in the figure are chosen to set the reference current at 8.88mA; this is the normal reference current for the G300 used with doubly terminated DAC outputs.

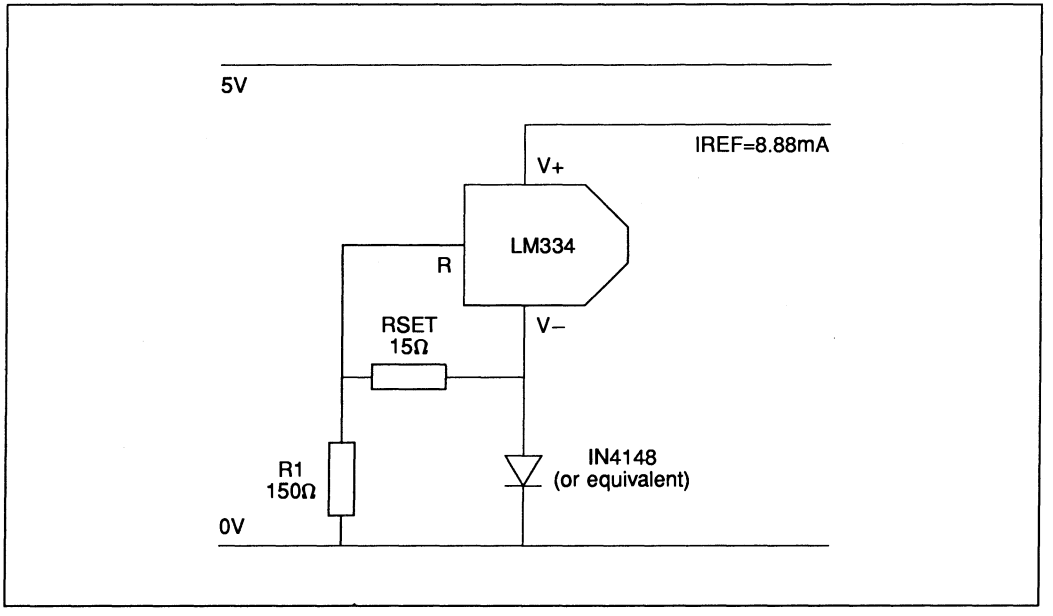


Figure 6.18 Current reference based on the LM334

6.10.5 Analogue output — line driving

The G300 is designed to drive a doubly terminated 75Ω line. This arrangement is illustrated in figure 6.19. The effective load seen by the G300 video outputs with this circuit is 37.5Ω.

The connection beteween the DAC outputs on the G300 and the input to the colour monitor should be regarded as a transmission line. Impedance changes along this line will result in reflection of part of the video signal back along the line. These reflections can result in a degradation of the picture displayed by the monitor. To ensure good fidelity RF techniques should be used; in particular the PCB trace from the G300 video output pins to the video sockets on the graphics board should be kept short (less than 3 inches is ideal). If this is done then any reflections due to a mismatched impedance at the video connectors will occur within the risetime of the DAC waveform and not cause a degradation of the image quality.

6.10.6 Analogue output — protection

CMOS devices are susceptible to damage from high electrostatic voltages. Normal antistatic precautions should be observed when handling the IMS G300 during system manufacture.

Once assembled into a system devices are much less exposed to static damage. However if the analogue outputs of the IMS G300 are made available at connectors outside the graphic system they are still exposed

to static damage and other hazardous voltages. Protection diodes to the power rails are recommended at this exposed interface.

	Colour Data (Full Scale)	Black Level Pedestal	Sync
units	255	20	108

Table 6.15 DAC output level components

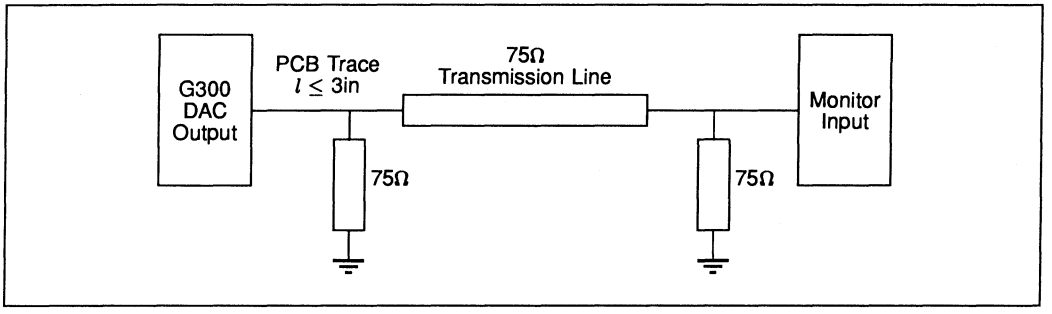


Figure 6.19 Dac Output Loading

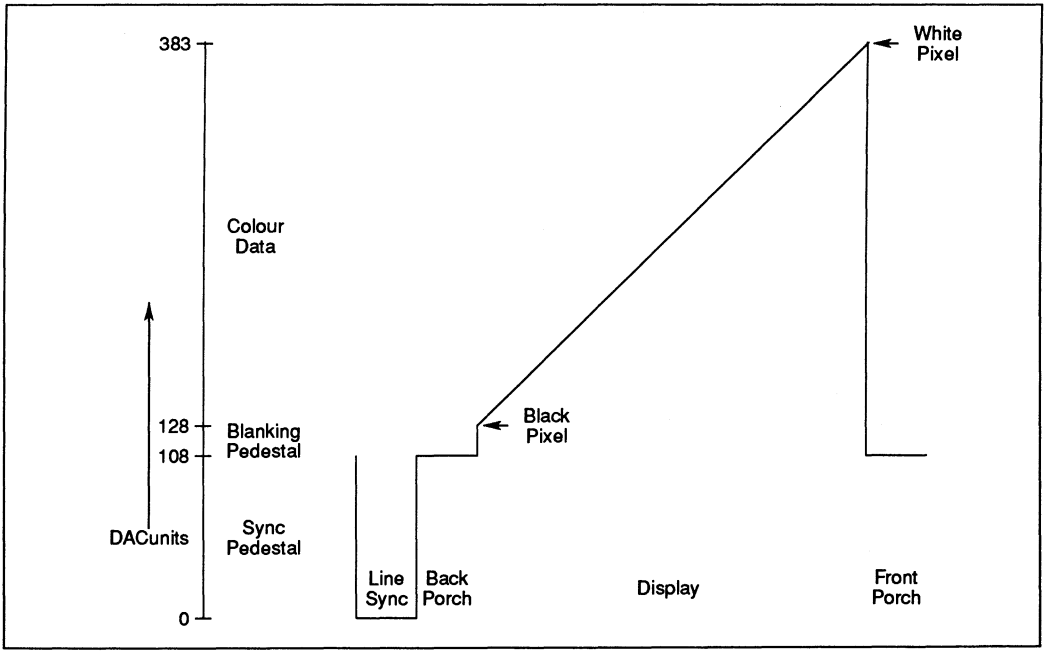


Figure 6.20 Dac Output Levels

6.11 Clock generation and phase locked loop

6.11.1 Introduction

The IMS G300 has two alternate clocking schemes which between them provide a high degree of system flexibility. The primary clocking system uses a phase locked loop on the chip to multiply the low frequency (<10MHz) input clock up to the required video data rate. This scheme is used only when the part is in mode 1 and contributes to its overall ease of design. A full dot-rate clock is supplied to the **PixClkIn** pad for the alternate scheme, which must be used when the IMS G300 is in mode 2 and when mode 1 is to be driven in 'times one' configuration.

6.11.2 PllClkIn

A clock must be supplied to this pad whenever the phase locked loop is to be used. **PllClkIn** must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. **PllClkIn** must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits. Phase locked loop mode is selected by placing a capacitor between **CapPlus** and **CapMinus**.

SYMBOL	PARAMETER	MIN	NOM	MAX	UNITS	NOTES
TDCLDCH	ClockIn pulse width low	20			ns	
TDCHDCL	ClockIn pulse width high	20			ns	
TDCLDCL	ClockIn period	110		200	ns	1
TDCerror	ClockIn timing error			±1.5	ns	2
TDCr	ClockIn rise time			10	ns	3
TDCf	ClockIn fall time			8	ns	3
Note: These figures are not characterised and are subject to change						

Table 6.16 **PllClkIn** timings

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their normal times.

3 Clock transitions must be monotonic within the range **VIH** to **VIL**.

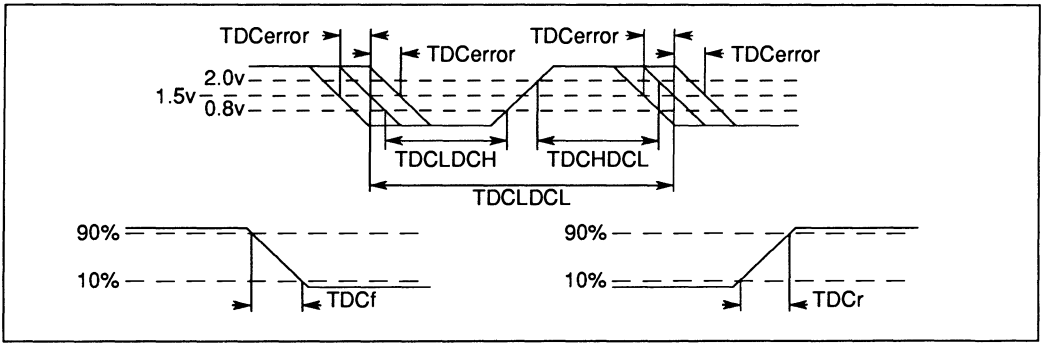


Figure 6.21 ClockIn timing

6.11.3 CapPlus, CapMinus

The internally derived power supply for internal clocks requires an external low leakage, low inductance 1uF capacitor to be connected between **CapPlus** and **CapMinus**. A ceramic capacitor is preferred, with an impedance of less than 3Ω between 100kHz and 10MHz. If a polarised capacitor is used the negative terminal must be connected to **CapMinus**. Total PCB track length should be less than 50mm. The connections must not touch power supplies or other noise sources.

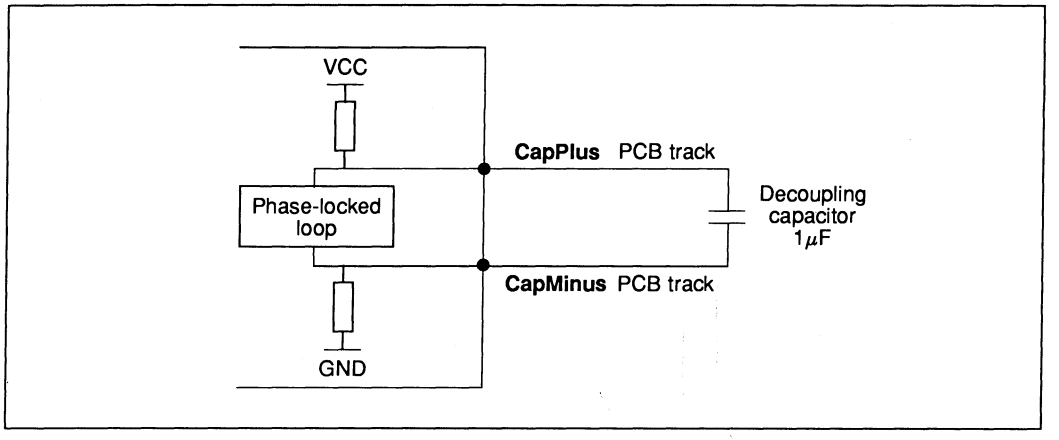


Figure 6.22 Recommended PLL decoupling

6.11.4 Speed selection

The multiplication factor of the phase locked loop is set by writing a binary value to the IMS G300 boot location. This location is enabled for writing by performing a reset cycle. Once it has been written to, another reset must be performed before reprogramming is possible. Only **ADBus**[4:0] are valid as data during these write cycles, in all other respects they conform to the diagrams given in section 6.8 . Although all possible multiplication factors will work with all permissible input frequencies up to the speed rating of the part, the quoted figures are guaranteed only if the recommended combinations are adhered to. The multiplication factor selected is the binary number written to the boot location.

6.11.5 Recommended input clock and multiplication factors

Video data rate (MHz)	PllClkIn (MHz)	Clock Multiplication
30	6	5
40	6.66	6
50	7.142	7
60	7.5	8
70	7.777	9
80	8	10
90	8.181	11
100	8.333	12
110	8.461	13
120	8.571	14

Intermediate video data frequencies can be produced by choosing the multiplication factor for the quoted frequency closest to that desired and varying the input clock frequency to achieve the correct value. Clock multiplication factors less than 5 are not allowed.

6.11.6 PixClkIn

This clock input must be used whenever mode 2 is selected or if mode 1 is to be used without the phase locked loop. Times one mode is selected by shorting **CapPlus** to **CapMinus** using a wire link or a switch.

6.12 General parametric conditions and characteristics

6.12.1 Operating conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VDD	Positive Supply Voltage	4.75	5.0	5.25	Volts	
GND	Ground		0		Volts	
VIH	Input Logic '1' Voltage	2.0		VDD+0.5	Volts	
VIL	Input Logic '0' Voltage	−0.5		0.8	Volts	
TCPGA	Maximum Case Temperature			**tbd**	deg C	1
TCQC	Maximum Case Temperature			**tbd**	deg C	1
Note: These figures are not characterised and are subject to change						

Notes

1 Measured on the lid of the package at maximum power dissipation.

6.12.2 Operating characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
IDD	Power Supply Current		300	400	mAmps	
IIN	Digital Input Current			± 10	uAmps	
IOZ	Off State Dig Output Current			± 50	uAmps	
VOH	Output Logic '1' Voltage	2.4			Volts	
IOH	Output Logic '1' Current	−5			mAmps	
VOL	Output Logic '0' Voltage			0.4	Volts	
IOH	Output Logic '0' Current	5			mAmps	
Note: These figures are not characterised and are subject to change						

6.12.3 Output drive capability

PIN	MIN	TYP	MAX	UNITS
notShiftClk			25	pF
notSerialClk			25	pF
Transfer			25	pF
ADBus [23:0]			25	pF

6.13 Package specifications

6.13.1 84 pin grid array package

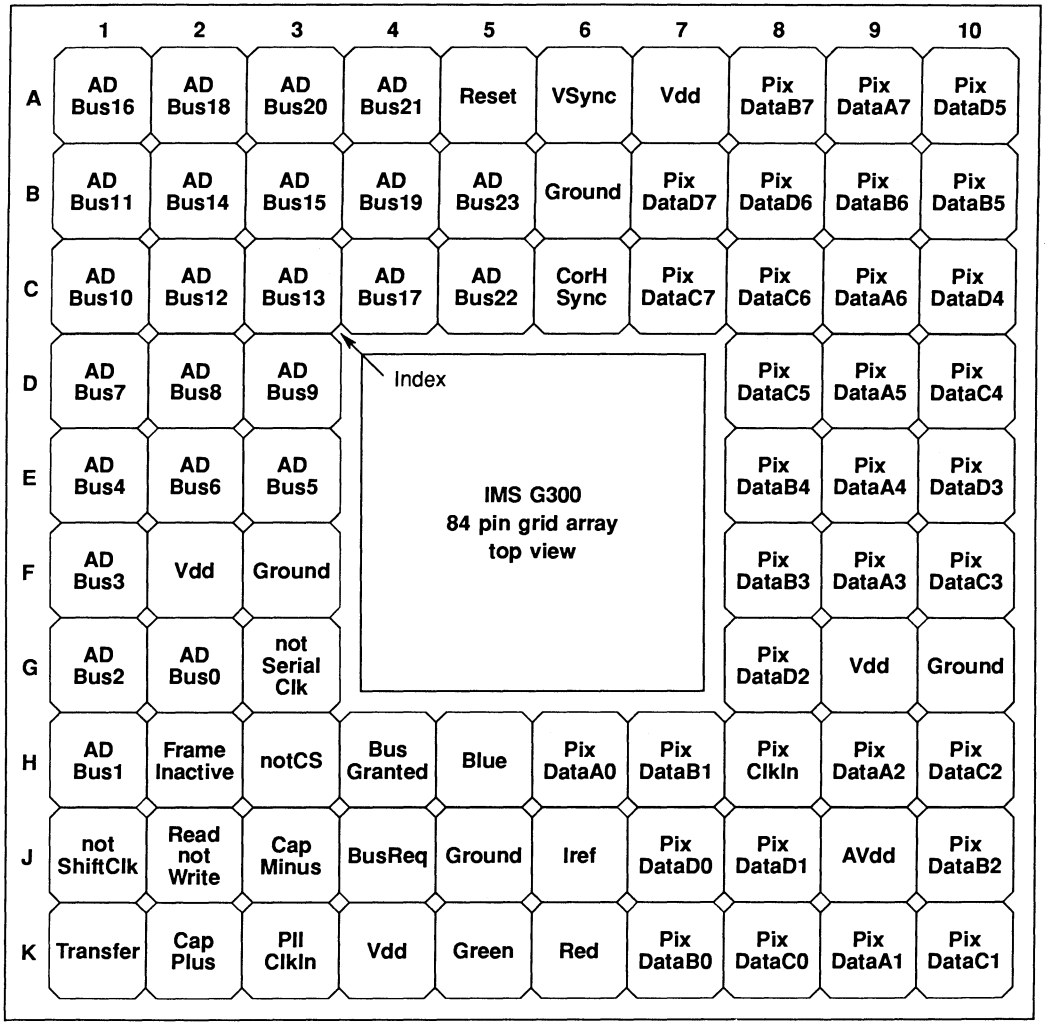


Figure 6.23 IMS G300 pin configuration

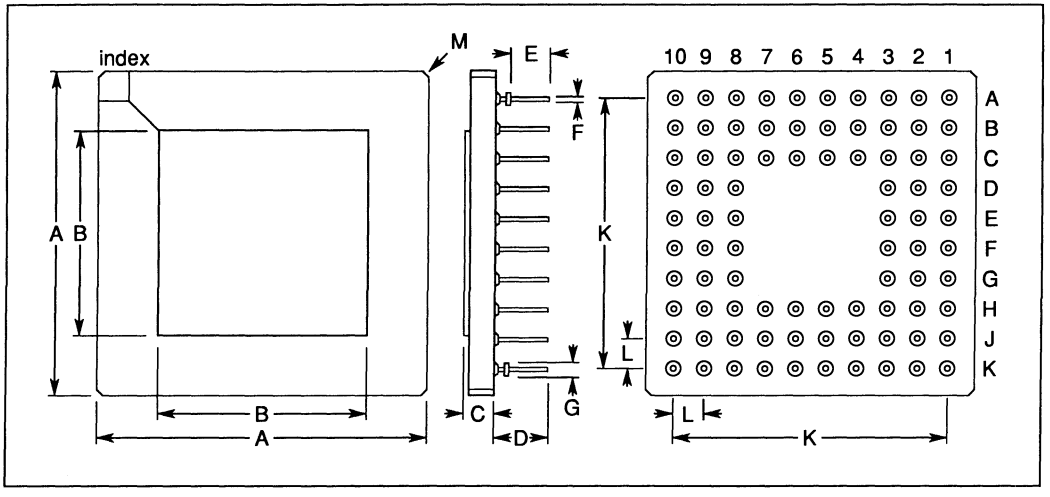


Figure 6.24 84 pin grid array package dimensions

DIM	Millimetres		Inches		Notes
	NOM	TOL	NOM	TOL	
A	26.924	±0.254	1.060	±0.010	
B	17.019	±0.127	0.670	±0.005	
C	2.456	±0.278	0.097	±0.011	
D	4.572	±0.127	0.180	±0.005	
E	3.302	±0.127	0.130	±0.005	
F	0.457	±0.025	0.018	±0.001	Pin diameter
G	1.143	±0.127	0.045	±0.005	Flange diameter
K	22.860	±0.127	0.900	±0.005	
L	2.540	±0.127	0.100	±0.005	
M	0.508		0.020		Chamfer
Package weight is approximately 7.2 grams					

Table 6.17 84 pin grid array package dimensions

6.13.2 84 lead quad cerpack package

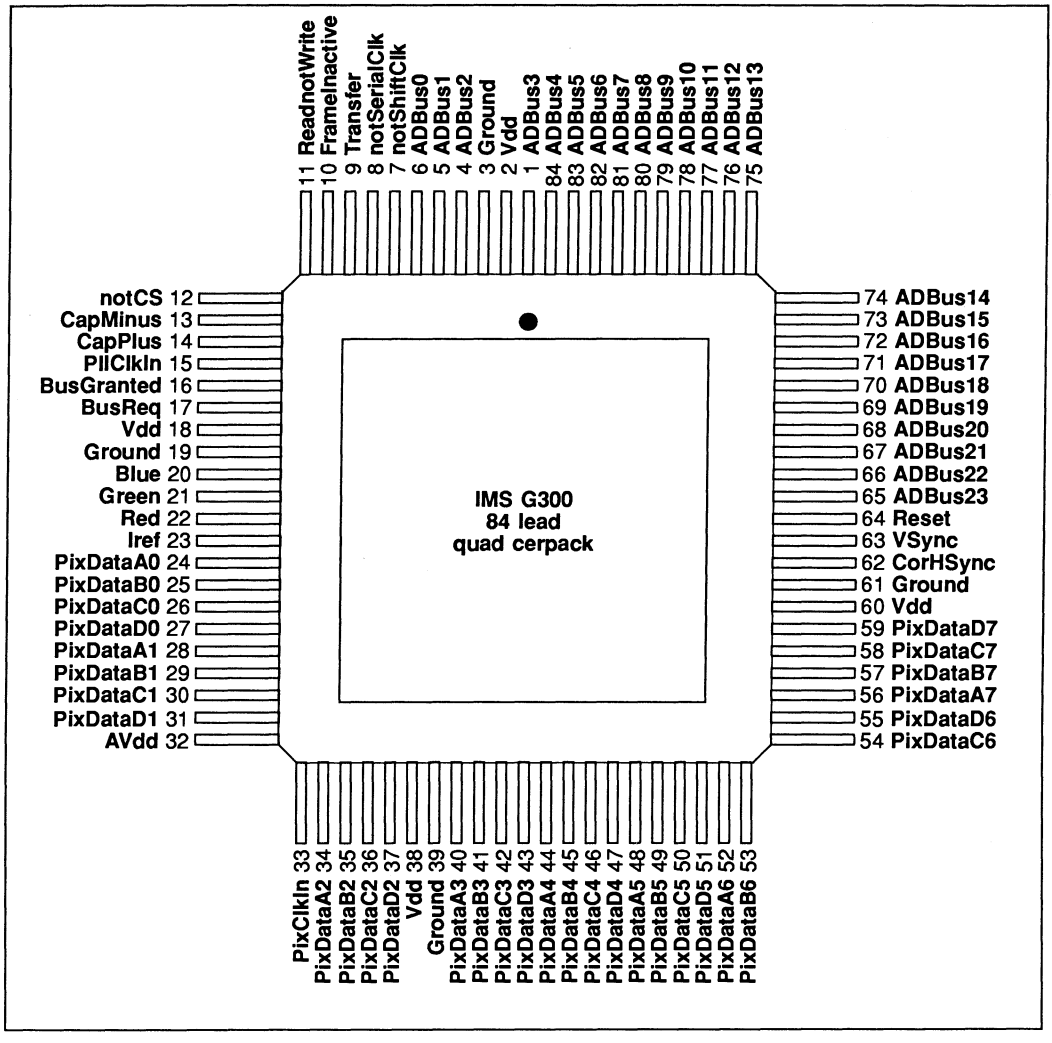


Figure 6.25 IMS G300 pin configuration

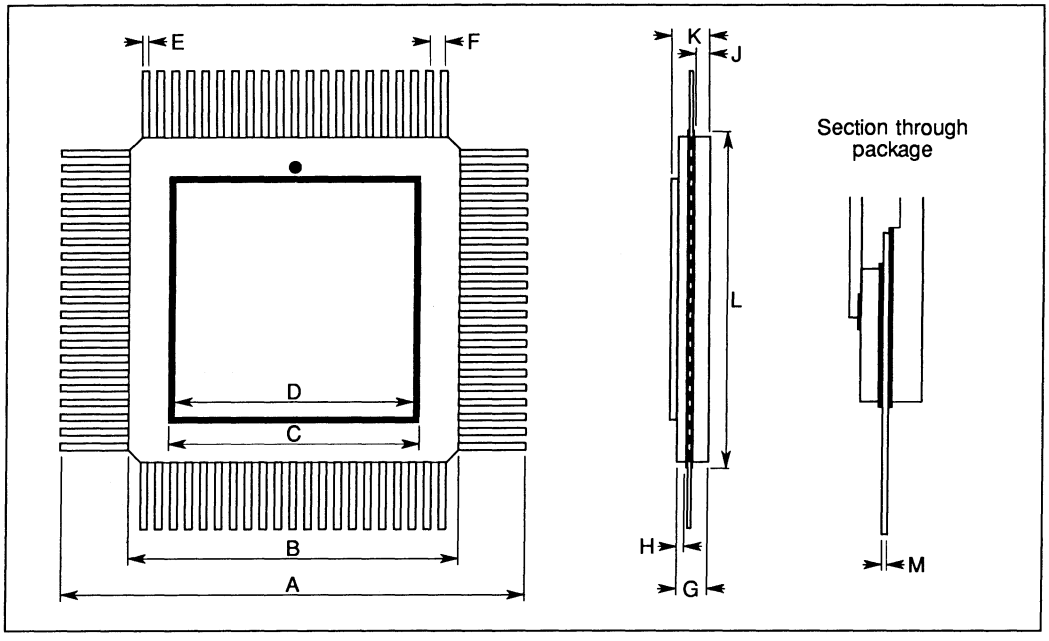


Figure 6.26 84 lead quad cerpack package dimensions

	Millimetres		Inches		
DIM	NOM	TOL	NOM	TOL	Notes
A	38.100	±0.508	1.500	±0.020	
B	26.924	±0.305	1.060	±0.012	
C	20.574	±0.203	0.810	±0.008	
D	19.558	±0.254	0.770	±0.010	
E	0.508		0.020		
F	1.270	±0.051	0.050	±0.002	
G	2.489	±0.305	0.098	±0.012	
H	0.635	±0.076	0.025	±0.003	
J	1.143	±0.102	0.045	±0.004	
K	3.099		0.122		Max.
L	27.940		1.100		Max.
M	0.178	±0.025	0.007	±0.001	

Table 6.18 84 lead quad cerpack package dimensions

6.13.3 Ordering information

Device	Clock rate	Package	Part number
IMS G300	66 MHz	84 pin PGA	IMS G300G-66
IMS G300	85 MHz	84 pin PGA	IMS G300G-85
IMS G300	100 MHz	84 pin PGA	IMS G300G-10
IMS G300	110 MHz	84 pin PGA	IMS G300G-11
* IMS G300	120 MHz	84 pin PGA	IMS G300G-12
IMS G300	66 MHz	84 pin QUAD CERPAC	IMS G300Q-66
IMS G300	85 MHz	84 pin QUAD CERPAC	IMS G300Q-85
IMS G300	100 MHz	84 pin QUAD CERPAC	IMS G300Q-10
IMS G300	110 MHz	84 pin QUAD CERPAC	IMS G300Q-11
* IMS G300	120 MHz	84 pin QUAD CERPAC	IMS G300Q-12
* Available 2nd half 1989			

6.14 Programming example for Hitachi HM-4219/4119 monitor

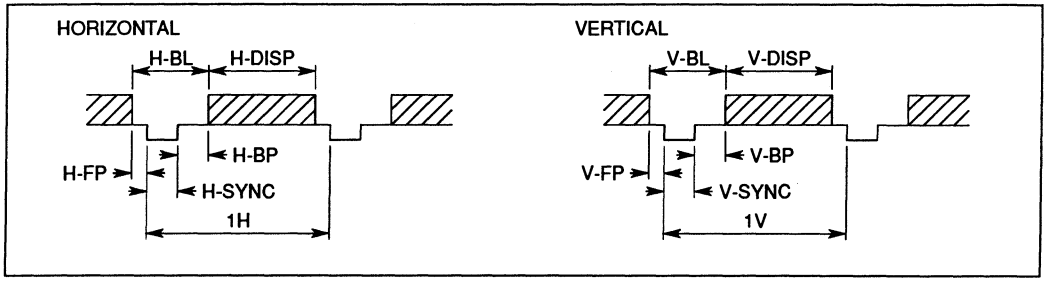


Figure 6.27 Hitachi HM-4219/4119 timing

	Item	Equation	Rating (64KHz Version)	Unit
a	Resolution H		1280	Pixel
b	Resolution V		1024	Pixel
c	Pixel rate		9.296	ns
d	Pixel frequency	1/c	107.573	MHz
e	H-DISP	a × c	11.899	μs
f	H-BL	g + h + i	3.800	μs
g	H-FP		0.200	μs
h	H-SYNC		1.600	μs
i	H-BP		2.000	μs
j	1H		15.699	μs
k	H frequency	1/j	63.7	KHz
l	V-DISP	b × j	(1024H)	ms
m	V-BL	n + o + p	(37H)	ms
n	V-FP		(0H)	ms
o	V-SYNC		(3H)	ms
p	V-BP		(34H)	ms
q	1V	l + m	(1061H)	ms
r	V frequency	1/q	60.0	Hz

Table 6.19 Recommended timings for monitor (64Khz version)

6.14.1 Calculation of parameters

At the recommended pixel rate of 9.296ns,

1 screen unit = 4 × 9.296ns = 37.184ns

All line timing parameters are calculated as multiples of this figure.

Line Scan period

Linetime = 15.699μs / 37.184ns = 422.19

so set Linetime = 422

This obeys the rule associated with the Linetime parameter; that it should be an even number of screen units.

If it is absolutely necessary to meet the recommended linescan frequency then it is best to specify the input clock frequency as the variable but, in practice, all monitors will synchronise to a close approximation.

Line sync pulse

The G300 constructs this from two halfsync periods so:

$$\text{Halfsync} = 1.6\mu s / (2 \times 37.184ns) = 21.5$$

so set Halfsync = 21 screen units

Backporch

$$\text{Backporch} = 2\mu s / 37.184ns = 53.7$$

so set Backporch = 54 screen units

Display

This parameter is set in terms of the number of pixels you wish to display so in this case:

$$\text{Display} = 1280 / 4 = 320 \text{ screen units.}$$

Frontporch

There is no explicit frontporch parameter; this period being implied as the difference between the sum of the other parameters and the linetime period.

$$\begin{aligned}\text{Frontporch} &= \text{Linetime} - ((\text{Halfsync} \times 2) + \text{Backporch} + \text{Display}) \\ &= 422 - (21 \times 2 + 54 + 320) \\ &= 6 \text{ screen units} \\ &= 6 \times 37.184 \text{ ns} = 0.223\ \mu s\end{aligned}$$

Which compares with the monitor requirement of 0.2 μs.

The 'halfline point' rule is obeyed by these timings since:

$$(\text{HalfSync} \times 2) + \text{Backporch} + \text{Display} < \text{Linetime} / 2 > (\text{HalfSync} \times 2) + \text{Backporch}$$

In a non interlaced system such as this the remaining two line parameters are actually used only during frame flyback in order to count in multiples of half a line time. In an interlaced system, the parameter Shortdisplay is used to construct the short displayed lines at top and bottom of the screen if the total number of displayed lines is odd. BroadPulse is used to produce the low pulses in a tesselated frame sync period. Both of these parameters must always be programmed whether or not your system explicitly uses them.

ShortDisplay

$$\begin{aligned}\text{Shortdisplay} &= (\text{Linetime} / 2) - (\text{HalfSync} \times 2) + \text{Backporch} + \text{FrontPorch} \\ &= 211 - (42 + 54 + 6) \\ &= 109 \text{ screen units}\end{aligned}$$

$$\begin{aligned}\text{BroadPulse} &= (\text{Linetime} / 2) - \text{Frontporch} \\ &= 211 - 6 \\ &= 205 \text{ screen units}\end{aligned}$$

Frame timing parameters

All frame timings are specified in terms of half line times.

Number of Displayed lines is 1024

$$\text{VDisplay} = 1024 \times 2 = 2048$$

Which complies with the requirement that each frame must contain an even number of half lines.

The G300 produces frame flyback waveforms in accordance with the broadcast standards which means that:

$$VSync = PreEqualisation = PostEqualisation$$

$$VSync = 6$$

Total Blanked period is 37H so :

$$VBlank = 74 - (6 \times 3) = 56$$

Which is a whole number of lines.

Thus the complete list of screen parameters is:

HalfSync	=	21
BackPorch	=	54
Display	=	320
LineTime	=	422
ShortDisplay	=	109
BroadPulse	=	205
VSync	=	6
VBlank	=	56
VDisplay	=	2048

The remaining three parameters are concerned with management of the video ram bitmap. Assuming that 256K video rams are being used, the shift register length will be 256 bits. The sum of the parameters MemInit and TransferDelay must not exceed this figure unless some external form of multiplexing is used which generates an effective register length greater than this. It is possible to use parameters which total less than 256 in order to implement a hardware pan function, but for the purpose of this example, we will assume that all of the bitmap is to be displayed. Thus:

$$Meminit + TransferDelay = 256$$

Transfer delay is

$$System\ DMA\ latency + VRAM\ access\ time + 1\ Screen\ unit$$

Assume DMA latency to be around 500ns and the VRAM access time to be 100ns then:

$$\begin{aligned} TransferDelay &= 600ns / 37.184ns + 1 = 17.13 \\ &= 18\ screen\ units \end{aligned}$$

Which obeys the conditions for TransferDelay that:

$$TransferDelay < Backporch$$
$$TransferDelay < ShortDisplay$$

(These are the only screen related limitations on the value of the VRAM management parameters)

$$MemInit = 256 - 18 = 238\ screen\ units.$$

LineStart is the top of screen pointer and it can be programmed to any value but with the following restrictions.

If the bitmap is to appear byte-linear to the processor, the SAM start address must be zero.

The SAM start address must never become greater than (256 – TransferDelay)

INMOS colour look-up tables

7.1 Introduction to colour look-up tables

The INMOS Colour Look-Up Table family is a range of graphics components, each of which integrates the functions of a colour look-up table (or colour palette), digital to analogue converters and microprocessor interface onto a single monolithic device.

The first member of the family, the IMS G170, was introduced in 1984 to replace a number of functional blocks of a colour graphics system which had previously been implemented in many discrete components or costly hybrids. INMOS drew on its previous experience with high-speed memory devices to produce parts handling up to 50MHz pixel data rates initially, though this has been surpassed by subsequent product releases. Next generation graphics products are targetted at 100MHz + whilst maintaining low-speed TTL compatible external signals and CMOS device technology.

The INMOS G17x family achieved a rapid acceptance by most of the industry's biggest colour graphics users, the greatest testament being their use by IBM in their entire range of PS/2 machines for the VGA graphics system. The IMS G171 in this case has set the new industry standard for colour look-up tables in its performance range, and is used by the majority of PS/2 clones and VGA add-in board manufacturers.

INMOS intends to keep pace with this volume market and is now offering higher speed and higher colour resolution devices in the same family. In addition INMOS is offering a device to address the growing workstation-type market by integrating yet further graphics system functionality and performance onto a single device. The IMS G300 Colour Video Controller (CVC) combines all the previously available functionality with a programmable video timing generator and VRAM refresh controller interface onto a single device and supports a totally flexible and truly upgradeable graphics system architecture (further details available from your local INMOS sales office.) With this and other graphics devices currently under development INMOS intends to remain a dominant force in the exciting colour graphics marketplace.

This note begins with an introduction to the Colour Look-Up Table concept and explains some of the commonly used terms to describe features in a graphics system. It then goes on to give some advice on how to choose a device for your application and gives some application hints for designing circuits with colour look-up tables to maximise performance. Finally it offers some suggestions on areas for investigation should problems arise.

7.1.1 What is a CLUT and where does it fit into a graphics system ?

Modern bit-mapped graphic displays work by building up a complete image from a two-dimensional array of picture elements or *pixels*. Each picture element defines the colour of its respective point on the screen. The number of pixels across one line and down one column of the image defines the *screen resolution* of the system.

Generally the image is stored pixel-by-pixel in a *frame store* built from RAM. For every pixel a code is stored to represent the colour of that pixel (in the case of a monochrome system this will be just a representation of the intensity). If a colour graphics system allocates n bits of data for each pixel then clearly each pixel can be displayed as one of 2^n colours. 8-bit pixels, for example, allow 256 possible colours, 24-bit pixels allow approximately 16 million colours.

The task of turning digital pixels into analogue red, green and blue signals to feed to a colour monitor is the function performed by a Colour Look Up Table or *CLUT*.

CLUTs use the digital pixel as an address into a table of *colour values*. For an eight bit pixel there will be 256 entries in this table, one for each colour. Each entry in the colour table is divided into three components, one each for the red, green and blue intensity components of that colour. In the case of the G171 each intensity value is a 6-bit number and so the total colour value contains 18 bits.

Whilst the number of locations in the colour table determines the number of available colours on the screen at any one time, it is the size of each entry in the colour table which determines the total number of colours from which the choice can be made. If there are 18 bits in each colour value, then the colour value may be chosen from 2^{18} or 256K possible colours. However since there are only 256 locations in the colour table only 256 of these are available for display at any given time. The choice is therefore 256 from 256K colours.

Once a colour value has been fetched from the location addressed by the pixel address it is split into its

three components and fed to three DACs to convert the red, green and blue values to analogue form. The analogue signals generated by the DACs are then driven out of the CLUT to the monitor. It is the resolution of the DAC which determines the *colour resolution* of the system. The 6-bit DACs in the G171 for example allow 2^6 or 64 different intensity levels for each of the red, green and blue components of a pixel. 4-bit DACs would allow 16 levels and 8-bit DACs would allow 256 levels.

7.1.2 Why use a colour table?

There are several reasons for using a colour table in a graphics system.

One of the major advantages of using a colour table is that it allows smaller size frame stores. By constraining the pixel size (to 8 bits in the case of the G17x family), the size of the frame store is reduced to a fraction of that which would otherwise be required to get the same colour resolution. Since the frame store is usually quite large this implies a considerable cost saving. The function of a CLUT can be viewed as one of colour expansion, expanding a colour representation of 8 bits to a representation containing 18 bits in the case of the G171. The basic rationale therefore is that for a particular colour graphics application, whilst a large *total* range of colours is desirable, only a limited sub-set of the range will be displayed at any one time, and is it this fact that allows the smaller frame store to be used.

Another advantage of using a colour table is that the controlling host or microprocessor has the ability to define the colours in the colour table, and may rapidly change the available colours at any time. An example of this would be to blank the screen. By writing 0 to each of the 256 locations in the colour table the screen may be blanked in a matter of milliseconds without any alteration of the image in the framestore.

Colour tables are often used in image processing or enhancement type applications. For example — choosing a specific colour table to enhance certain colour changes in an image, and thereby highlight features or object boundaries in the image. This sort of technique again requires no modification of the primary image stored in the frame store.

Overall, CLUTs provide a convenient and cost effective route to integrating the colour expansion facilities of a look-up table with the sensitive circuitry required for generating analogue video signals.

7.1.3 The INMOS CLUT range

The INMOS family of CLUT products currently extends to 4 members with further products under development. Those available now offer a range of different functionality and maximum pixel data rates as summarised below:

Part no.	Pixel rates	Composite video	Read-back	DAC resolution
IMS G170	35,50	√		6 bits
IMS G171	35,50		√	6 bits
IMS G176	40,50,65		√	6 bits
IMS G178	40,50,65,80	√	√	6/8 bits

The IMS G170 offers pixel rates up to 50MHz as well as the ability to generate composite video waveforms (see Glossary of Terms.)

The IMS G171 is the device used by IBM in all PS/2 machines, so is fully VGA compatible. It offers pixel rates up to 50MHz.

The IMS G176 is an upward compatible route from the IMS G171 and provides pixel rates up to 65MHz and a choice of package options.

The IMS G178 is a further upward compatible step from the IMS G176, and adds the option of 8-bit DACs as well as the ability to generate the composite video signals present on the IMS G170.

7.1.4 Choosing your device — functionality

For most medium-high resolution colour displays it is accepted that 6-bit DAC resolution is sufficient. This gives a total colour choice of 262,144 colours which can be programmed into the CLUT. For very high resolution applications such as CAD/CAE workstations where 3-D solid modelling requires ultra-smooth shading, INMOS provides the IMS G178. This has 8-bit DAC resolution, giving a total colour choice of over 16 million colours, but can also be switched back to offer compatibility with 6-bit DAC application software.

The provision of horizontal and vertical synchronization signals to a monitor are required to indicate the end of a line or frame of display information. These sync signals can be provided on a separate wire to the monitor or superimposed onto the analogue video signals to give Composite Video (see Glossary of Terms.) The choice of method is largely dependent on the type of monitor used. Some are switchable to operate on either scheme. This superimposition of video and sync signals can be performed internally on the IMS G170 or G178 devices.

On parts with read-back the contents of the colour table may be read as well as written, i.e. the microprocessor interface is bi-directional. This is used mainly for self-testing purposes, and also avoids any need to keep a shadow copy of the colour table when one application is 'switched out' to make way for another application requiring a different colour selection. The IMS G171, G176 and G178 all provide this facility.

7.1.5 Choosing your device — speed selection

A first-pass calculation for the pixel data rate required can be obtained by multiplying:

Horizontal Resolution x Vertical Resolution x Frame Refresh Rate

$$H_{RES} \times V_{RES} \times F_{RSH}$$

e.g. 480 x 320 x 60Hz = 18.5MHz

However, as the desired resolution increases the amount of time which the monitor spends in horizontal and vertical blanking (while the electron beam retraces to the start of the line or frame) becomes significant. Since this reduces the actual time available for pixel refreshing, the pixel data rate must increase accordingly. These blanking parameters are a function of the particular monitor used. To display higher resolution images a better quality monitor is required which has shorter retrace times.

If Horizontal Blanking Time = H_{BLK}

Vertical Blanking Time = V_{BLK}

Time taken per second in blanking:

$$T_{BLK} = (V_{RES} \times F_{RSH} \times H_{BLK}) + (F_{RSH} \times V_{BLK})$$

So time remaining for pixel refreshing:

$$T_{RFH} = 1 - T_{BLK}$$

Pixels to be refreshed per second:

$$P_{RFH} = V_{RES} \times H_{RES} \times F_{RSH}$$

Therefore the pixel data rate required:

$$= \frac{P_{RFH}}{T_{RFH}} = \frac{V_{RES} \times H_{RES} \times F_{RSH}}{1 - F_{RSH}[(V_{RES} \times H_{BLK}) + V_{BLK}]}$$

In this way the actual maximum pixel data rate required for the particular application and monitor used can be calculated, and the appropriate device selected.

7.1.6 A glossary of terms

The following glossary covers many of the common terms and parameters describing Colour Look-Up Tables and their application.

CLUT Colour Look-Up Table

Colour Table The memory inside the CLUT, containing the colour values.

Colour Value A word stored in the colour table defining the colour of a pixel in terms of its red, green and blue intensity.

Frame Store The digital representation of the displayed image in the form of a 2-dimensional array of pixels.

Pixel Address The pixel value stored in the frame store and used to address colour values in the CLUT.

DAC Digital to Analogue Converter

Resolution The number n, where 2^n is the number of discrete analogue levels which the DAC is capable of converting. For example 6 bit resolution allows the conversion of 64 discrete output levels.

Accuracy Accuracy defines how close the output of a DAC is to the correct output as predicted by the design equation for the DAC at any point in the transfer function. The most common figure specified is the full-scale accuracy, that is the accuracy of the DAC when generating its maximum value.

Integral Linearity Defines the deviation of any point in the output signal from a theoretical straight line through the DAC output signal.

Differential Linearity Defines the deviation between, the magnitude of a unit output change between any two adjacent conversion levels, and the correct unit change as predicted by the design equation for the DAC.

Monotonicity A DAC is monotonic if the sign of the output change, from each level to its successor level, remains constant across the entire conversion range of the DAC.

Risetime The time required for a DAC output signal to switch from its minimum output level to its maximum output level, whilst operating under specified load conditions. For practical reasons the time is usually measured from quoted threshold levels just above zero and just below full-scale.

Settling Time The time required for a DAC output signal to switch from one level (usually zero) to another (usually full-scale) and settle within a specified range close to the final value. Like risetime, this parameter will be a function of the loading conditions (R, L and C) placed on the DAC output.

Glitch Energy Glitch energy quantifies the deviation between the actual transition of a DAC output waveform switching between two levels, and the ideal transition waveform between these two levels. Real DACs often suffer from glitches when switching between levels, the most common glitch being the major transition at the half-way point in the conversion range. Glitch energy, usually quoted in pVSec for video DACs, is a measure of the area of this glitch on a graph of DAC output voltage against time. (The term 'energy' is a misnomer, since Volt.Sec is not a unit of energy)

Composite Sync To provide a timing reference to the colour monitor indicating the point where a new frame or a new line starts, all monitors require two types of sync pulses — frame sync and line sync pulses. Frame and line sync pulses are distinguished by their duration. Frame sync pulses are longer than line sync pulses, For a typical high-resolution monitor, a frame sync pulse might be 50–100μs whereas line sync pulses would be in the region 2–6μs.

Composite Video There are two different approaches to providing sync pulses. Composite video superimposes these timing pulses onto the analogue video signal (approximately a 0.3V pedestal on a 0.7V video signal using the RS170 standard). Most monitors strip the sync information from just the green channel, even though G17x devices with composite sync supply it on all three channels. A separate sync video system, as its name suggests, supplies the sync pulses on a separate line. This system has the disadvantage of requiring an extra signal line to the monitor; although clearly it has the advantage of not requiring a circuit to strip the sync timing from the video inputs inside the monitor.

Frame Refresh Rate Frame rate defines the frequency at which each new frame is drawn on the screen. Too low a frame rate can lead to a perception of the image flickering on the screen. Common frame refresh rates are 50–70Hz.

Interlaced Screen A technique used to lower the video dot rate whilst still maintaining a high screen resolution. Interlaced displays refresh just alternate lines of the image on every frame scan, swapping between odd and even lines on each successive sweep.

7.2 Using INMOS CLUTs

7.2.1 General board layout

To get the best performance from an analogue component such as a Colour Look-Up Table (CLUT) in the noisy environment of a graphics board, it is important to pay some attention to the board layout, in particular components surrounding the CLUT.

First and foremost, it is essential to use a four-layer board with VDD and GND planes separating the wiring planes. Large continuous power planes on adjacent layers ensure a good low-inductance power supply to all parts of the board with distributed capacitve coupling between the power planes across the board. This minimises undershoot on the digital signals routed round the board. In addition VDD and GND planes minimise the power radiated from signal tracks and thereby reduce the energy coupled into other sensitive conductors on the board, such as the the analogue outputs of the CLUT.

VDD and GND planes should be periodically coupled with high frequency (i.e. low series inductance) capacitors. Chip-capacitors in the range 100 – 500nF are the best for this; being leadless chip capacitors have very low series inductance. If chip-capacitors are not available then ceramic capacitors with the absolute minimum lead length are the next best.

Other general hints include positioning the CLUT as close to the edge of the board as possible, keeping the current reference circuit close to the CLUT, not laying analogue output tracks over digital tracks and keeping the pixel input buffer as close to the CLUT as possible. A number of these points are explained further in later sections of this note.

7.2.2 The power supply to the CLUT

In order to minimise the noise on the the DAC outputs of a CLUT it is important to minimise the noise on the power supply to the CLUT since the DAC output current is referenced to the positive power supply — VDD. Ideally the noise should be no more than 200 – 300mV and preferably less.

A more important factor than the absolute magnitude of the noise is the ability of the current source to track the power supply noise on the IREF pin. This is because the instantaneous current out of the DAC is always set by the **voltage difference** between the VDD pin and the IREF pin. In practice then, it is quite possible to achieve a very clean analogue output, even with large noise fluctuations on the power supply, so long as the current source has a sufficiently fast response time to keep the voltage on IREF tracking these fluctuations, and so keep the voltage difference between VDD and the IREF pin constant. Clearly though, whilst a high speed tracking current reference will minimise power supply noise on the DAC outputs it is preferable to avoid the VDD noise in the first place.

In many systems which have a clean global power supply, achieving a noise free supply to the CLUT will require no more than a good high frequency coupling of the supplies right next to the device. Excessive PCB design work to provide separate digital and analogue VDD and GND planes would be uneccessary and unjustified. Again a high frequency 100nF capacitor in parallel with a larger 47μF capacitor (preferably tantalum) should be used.

7.2.3 Decoupling the CLUT supply

In situations where the main board supply is too noisy to achieve acceptable results by local capacitive coupling next to the CLUT, then it is possible to provide a locally decoupled supply for just the CLUT using a simple L-C circuit, figure 7.1.

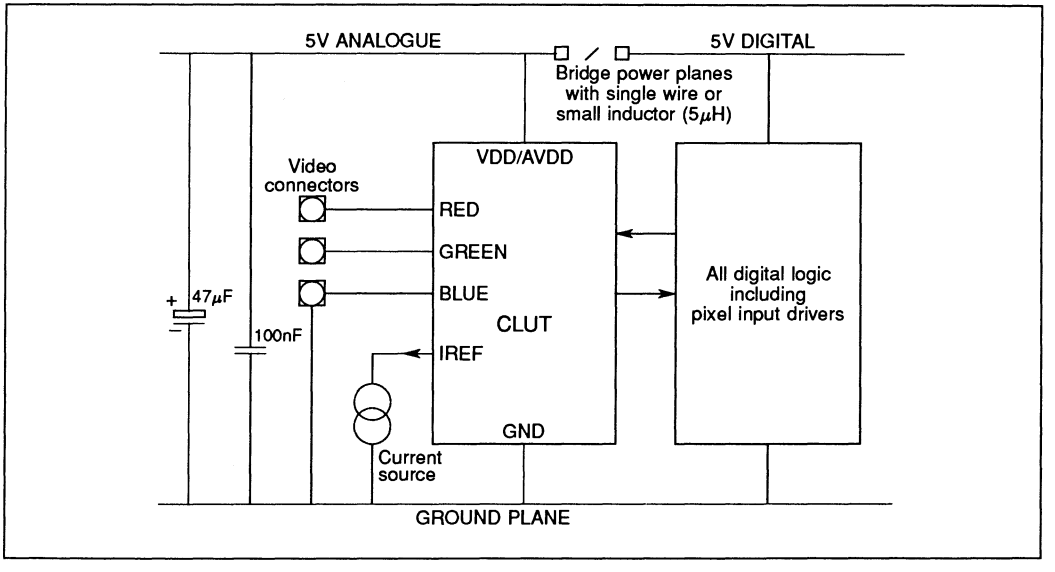


Figure 7.1 Locally decoupling the CLUT supply with an L-C circuit.

This separate analogue supply should be maintained on a single island power plane. It should overlap just the analogue parts of the CLUT package: RED, GREEN, BLUE, the IREF circuitry and the VDD pin. This will ensure minimum pick-up from the other digital circuitry and wiring.

A practical value for the inductor is in the region 1–5μH. Small PCB and surface mount inductors in this range are readily available with current ratings sufficient to supply the 150–200mA supply current required by

INMOS CLUTs. The capacitor should be 47μF, but again a 100nF low inductance capacitor should be used in parallel.

In the case of a part with a separate analogue power pin AVDD as well as a digital VDD pin, (such as the G176 in a surface mount package), both pins should be taken to the separate analog power plane.

7.2.4 The pixel inputs

Edge rates on the pixel inputs should be kept as slow as possible, consistent with the timing requirements on the pixel port; this will ensure the minimum of clock noise pick up on the analogue outputs. On many graphics boards the major source of noise on the DAC outputs will be noise coupled through from the pixel lines and the pixel clock itself.

Since both the pixel clock and the pixel data lines run at the full video rate it is preferable to keep these lines short (less than 3 inches.) Ideally the buffers which drive these lines should be positioned close to the CLUT to reduce the reflection time and thereby minimise undershoot and ringing.

If board layout constraints make long tracks unavoidable, or if very fast drivers have to be used to meet the required timing specification, then series termination at the buffer output is recommended to minimise undershoot. Typically a resistor around 100Ω placed in series with the output will improve the matching between the buffer output impedance and the impedance of the PCB track. To achieve perfect matching the characteristic impedence of the lines should be determined empirically, and a series resistor of the same value used. Parallel termination may also be used with the same value of resistors, but this has the disadvantage of consuming D.C. power and may load the pixel buffer outputs beyond their drive capability.

7.2.5 The DAC outputs

The analogue outputs of all INMOS CLUTs come from switched current sources drawing current from the positive supply. The output may drive either a singly or doubly terminated 75Ω load according to the device used. Double termination is the preferred method since, with both ends of the transmission line being correctly matched, outputs are less likely to suffer from reflections returning from any mismatch along the length of the transmission line between DAC outputs and the monitor. With long monitor cables, mismatches will lead to reflected components returning to the monitor after the first pixel edge and degrading the quality of the image. Another advantage is that it gives sharper DAC edge rates (due to the lower RC time-constant). Double termination is illustrated in figure 7.2.

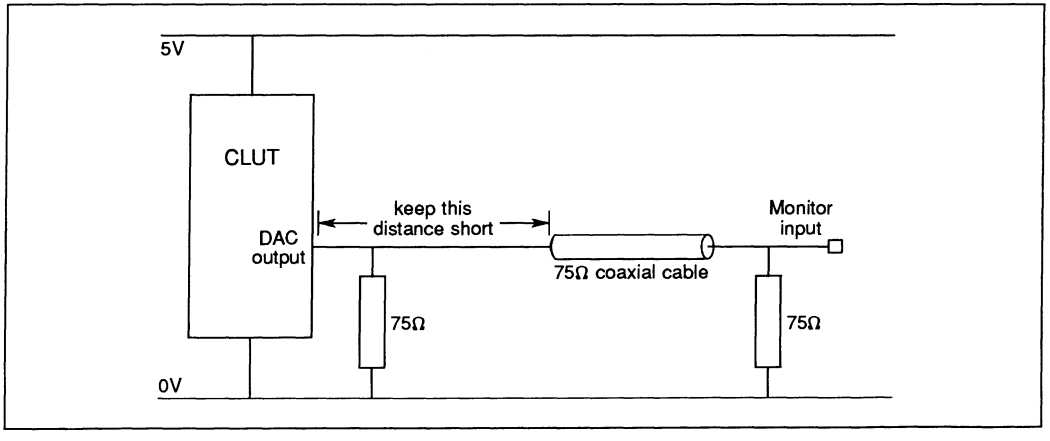


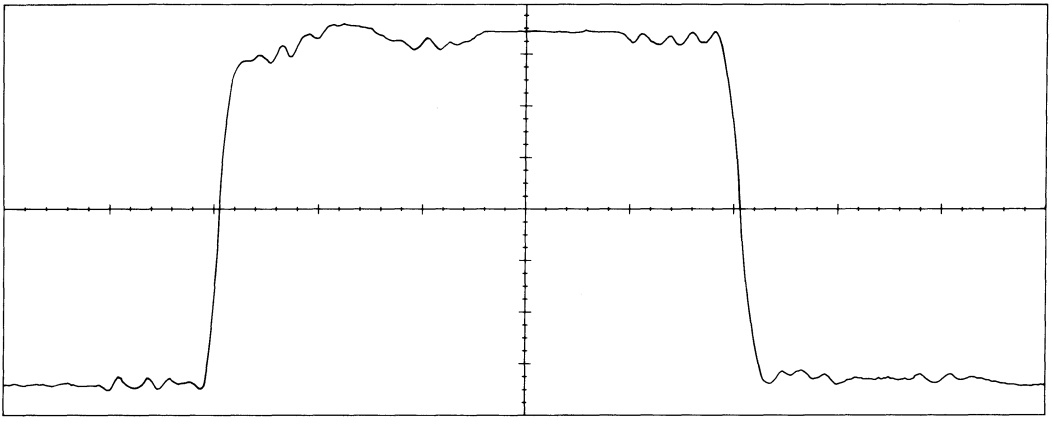
Figure 7.2 Double termination of DAC output.

The resistors used should be high-accuracy metal or carbon film types. Often the monitor will contain its own terminating impedance which can be switched in, so only the resistors at the CLUT outputs will be of concern to the board designer.

DAC output traces should also be treated as transmission lines and mismatches anywhere in the path leading from the analogue output pins on the CLUT package to the monitor RGB inputs will degrade the final image quality. In most systems the simplest way of ensuring minimal reflections is to keep the distance from the DAC output pins on the CLUT to the video connectors on the PCB down to the absolute minimum — less than 2–3 inches is ideal. If this is done then any reflected components coming back from the video connectors will occur well within the risetime of the pixel edge and little or no loss of image quality will result. The ideal position for a CLUT on a graphics board is at the edge of the board with the video connectors feeding out from the edge. This will also serve to minimise noise pickup on the analogue output traces.

As with any other CMOS device, members of the IMS G17x family can be damaged if exposed to high electrostatic voltages. Once assembled into a system they are much less exposed, though the analogue outputs are usually still made available externally through the connector to the monitor. If these are likely to be subject to stray electrostatic voltages, particularly if cables to the monitor are frequently connected and disconnected, then some kind of protection device should be considered on these outputs. Any fast silicon diode is usually sufficient, e.g. 1N4148's have been found to be a cheap and effective solution.

Figure 7.3 shows a typical DAC output waveform generated by a G176 device. The DAC is shown switching through its full range 0–63. The voltage amplitude is approximately 650mV and the edge rates are between 2 and 3ns.



Ch. 1 = 100.0 mvolts/div
Timebase = 10.0 ns/div

Figure 7.3 DAC output waveform showing reflection and clock noise.

A minor reflection after the rising and falling edges is clearly visible, as is a small component of clock and pixel noise.

7.2.6 Current sources

All INMOS CLUTs require a simple current source to provide a reference current for the DAC outputs. This current is drawn from the positive rail. The principal considerations when designing a current source for a CLUT are accuracy, thermal stability and a fast AC response. A number of different circuits are possible, and there is the usual tradeoff between cost and performance to consider. Some recommended current sources are described below which cover the range of cost and performance.

1 The simplest and cheapest reference circuit can be made with just a transistor and 3 resistors, as shown in Figure 7.4. This is appropriate in very cost sensitive designs where accuracy and stability are not critical.

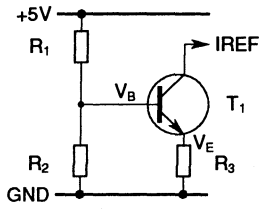


Figure 7.4

In this circuit IREF is set by the potential divider of R_1 and R_2. There is no compensation for variations in the base-emitter voltage of T_1. Assuming a high gain transistor the equation for this circuit is:

$$V_{CC} \times \frac{R_2}{R_1 + R_2} - 0.6 = IREF \times R_3$$

2 Figure 7.5 shows a current source based on the TL431 voltage reference. Note that it is only appropriate when there is a negative supply rail VNEG available, such as used for disk drives or communication ports.

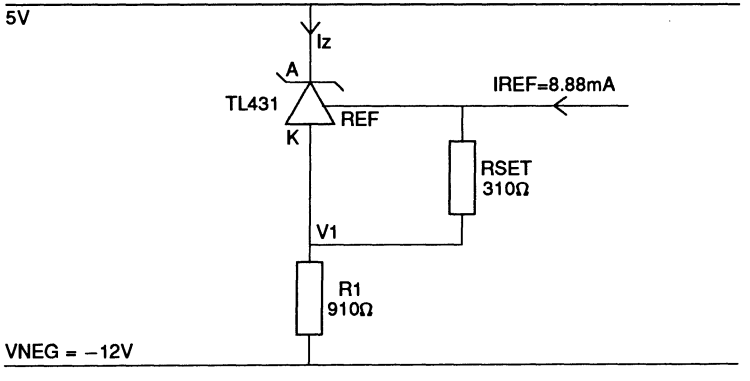


Figure 7.5 Current reference based on the TL431 voltage reference.

This circuit requires just two resistors together with the 431. The 431 works by maintaining the voltage across RSET at 2.75V. Since the current into the reference pin of the 431 is negligible (it never exceeds 10μA), the value of RSET determines the IREF drawn from the CLUT:

$$IREF = \frac{2.75V}{RSET}$$

IREF is summed with the regulator current Iz flowing through the 431 and passes to the negative rail through R1. The value of R1 should be chosen so that Iz comfortably exceeds 2mA (say 5mA);

this ensures that the 431 is biased correctly. For IREF currents in the range 4 to 10mA, the voltage on the IREF pin will typically be around 3V. Subtracting the 2.75V developed across RSET means that the voltage V1 will be around 0.25V. Knowing the voltage of the negative supply, R1 can be chosen to set the current Iz to approximately 5mA:

$$R1 = \frac{0.25V - VNEG}{IREF + Iz}$$

The component values shown in the figure are again chosen to set IREF at 8.88mA and Iz at approximately 4.6mA. Clearly, VNEG need not necessarily be −12V, a −5V rail could just as well be used provided R1 is chosen to keep Iz well above 2mA.

If no negative power rail is available then the addition of one extra transistor allows the circuit to operate on the normal single 5V rail as shown in figure 7.6.

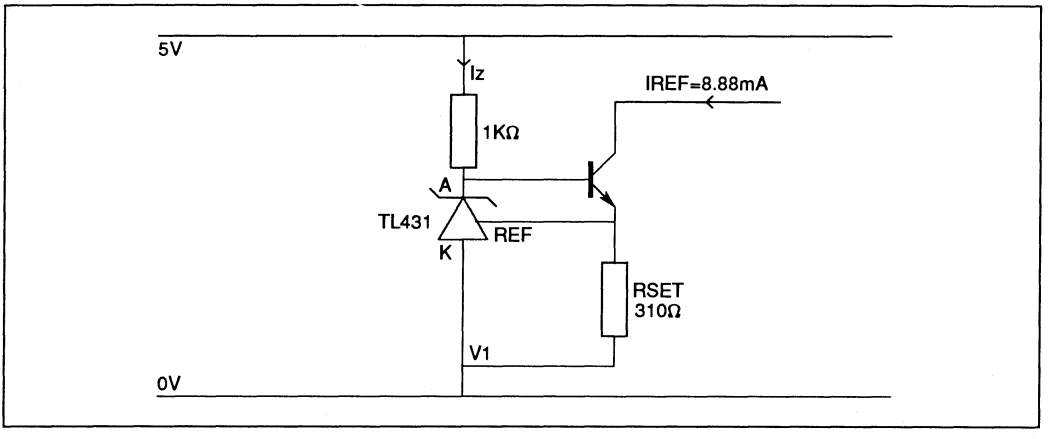


Figure 7.6 TL431 reference circuit operating on a single 5V rail.

Again the TL431 maintains the voltage across RSET at 2.75V which in turn sets the emitter current through the transistor, and hence the reference current.

3 Figure 7.7 shows a current reference based on the LM-334 device.

The device is used in its zero temperature coefficient mode. This device can supply reference currents up to 10mA. The value of RSET sets the basic current drawn, and must be a precision resistor, with the second resistor R1 and the silicon diode (IN4148) providing temperature compensation. From the LM-334 datasheet the relevant calculations are:

$$RSET = \frac{66.7mV \times 2}{IREF}$$

$$R_1 = 10 \times RSET$$

The component values shown in the above figure are chosen to set the reference current at 8.88mA. This is the normal reference current for INMOS CLUTs used with doubly terminated DAC outputs to give a peak white signal of 0.7V.

7.2.7 Radiated power from graphics systems

In order to comply with FCC regulations concerning computing devices, all computing systems, including their graphics components, must not emit Radio Frequency Interference beyond set limits. The following guidelines are intended to help designers minimise the RFI emitted from the video components of a graphics system, including the CLUT circuitry.

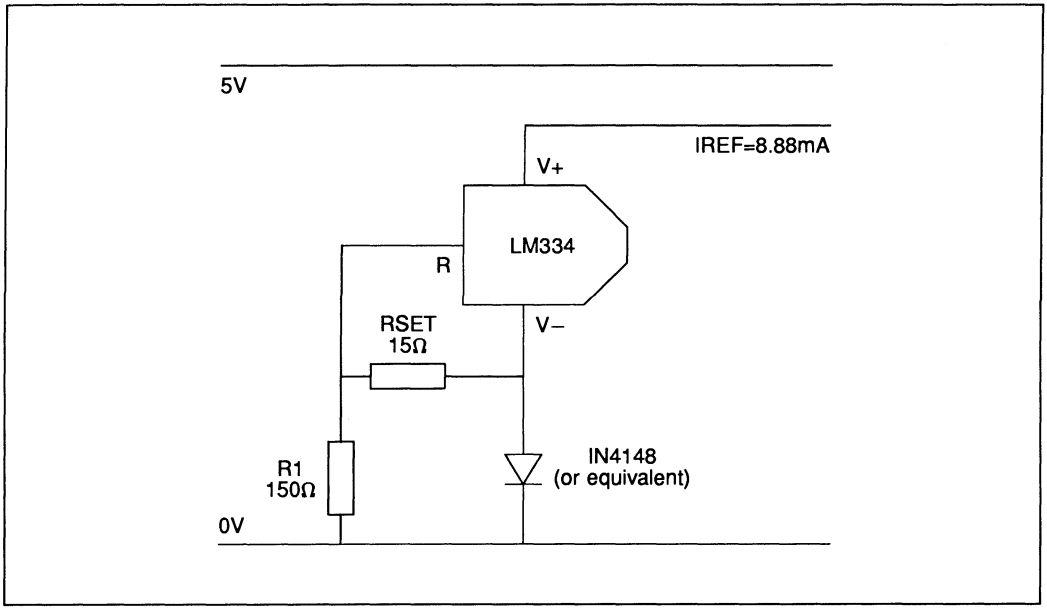


Figure 7.7 Current reference based on the LM334.

All conductors carrying time varying currents radiate electromagnetic radiation. This radiation in turn may induce currents in other conductors nearby. Radiated power from a conductor increases when it is physically large and is separated by a large distance from any ground plane. That is to say, good radiating ariels are large open systems. In a typical graphics board, the major radiating ariels are the tracks and wires surrounding the video components which carry the high frequency video signals.

To minimise the radiated power from a board a number of basic rules can be applied:

1 Keep tracks leading to and from the CLUT short, particularly the pixel address, pixel clock and DAC outputs.

2 Always use a four-layer board with VDD and GND planes.

3 Avoid flying leads carrying high frequency signals which are not screened.

4 Place load resistors as close as possible to the analogue outputs.

Major current transients occur when CLUT DACs are switched on and off, since this current is drawn from VDD it is important to ensure that VDD to GND coupling close to the CLUT is efficient both at low and high frequencies.

Radiated power increases with the frequency of the radiating signal (to the fourth power). It is therefore desirable to have as few signals as possible with very fast edge rates since these will have high frequency components. For example, do not use FTTL where LS will meet the timing requirements; as well as giving greater undershoot on PCB traces, the fast edges produced by the faster logic will radiate more power.

The DAC outputs themselves will in many systems be a significant radiating source. Here again any high frequency noise transients should be kept to a minimum. These may be coupled through from the pixel lines or VDD noise. Ferrite beads may be used on the analog outputs to remove these high frequency transients, though some experimentation will be required to achieve the maximum suppresion consistent with an acceptably fast risetime on the DAC output.

It should be noted that any risetime much faster than the bandwidth of the monitor it is feeding serves little purpose other than to generate more RFI and will not improve the sharpness of the displayed image.

Although not a significant contributor the bond wires of a package can behave like ariels for radiated power. In very critical high-speed applications it may be preferable to use a device in a PLCC package (IMS G176 or IMS G178) since the bond wires in such a package are shorter than in the 28-pin DIL package and overall RFI emissions may be reduced.

In summary, to minimise RFI emissions, keep all tracks carrying video and near-video rate signals as short as possible, keep edge rates as slow as possible and ensure good power supply coupling around all the video circuitry.

7.2.8 Minimising the power dissipation of a CLUT — Power-down mode

In some cases, portable battery equipment in particular, it may be necessary to minimise the power dissipated by a CLUT by putting it into a power-down mode. An example would be a lap-top computer which ordinarily used an LCD display but had the option to generate full colour displays on a standard colour monitor using a G171.

Although not documented in the data sheets there are several things that can be done to minimise the power consumption of G17x devices by putting them into an effective "power-down" mode. Firstly the DAC current can be reduced to zero. The simplest method of doing this is to reduce the reference current, IREF, to zero. This will switch off the DACs completely, pulling the maximum D.C. current down to below 100mA.

Stopping the pixel clock supplied to the CLUT will reduce the digital current drawn by the part to something less than 10mA; this remaining current is drawn by DC paths inside the G17x. One of these DC paths is in the input stage of each pixel input, and by taking the pixel inputs low this path too can be turned off.

In summary, by switching off the IREF current, stopping the pixel clock and holding the pixel inputs low, the DC current of the G17x can be reduced to something in the range 5–10mA, thus reducing overall power consumption to 25–50mW.

7.3 Circuit techniques using the G17x family

7.3.1 Adding composite sync to the G171/6

The major functional difference between the IMS G170 and the G171/6 devices is that the former provides the facility for adding composite sync, whereas the latter two devices offer the alternative facility of reading back the colour table contents. It quite possible however to add the composite sync function externally to the G171 or G176 and have both features. The component count to do this is small and it requires only minimal redesign around the CLUT socket.

The circuit shown below is used to superimpose a simple step waveform onto the DAC outputs of the G171/6. When this offset is momentarily removed a sync pulse is transmitted. The circuit basically has three sections:

1 A SYNC Shifter. All IMS G17x parts achieve high pixel rates by pipelining the memory accesses over a number of clock cycles. Thus there is a delay between the input of pixel data to the look-up table and the output of the appropriate analogue value. To ensure that the SYNC signal remains aligned to the picture it must be delayed by a similar number of clock cycles by using a shift register. For the IMS G171/6 the SYNC signal must be delayed by 3 clock cycles.

2 A Current Reference. Since the IMS G171/6 DACs are current sources a SYNC type waveform can be added simply by providing an additional sync reference current to the DAC output.

3 A Current Dump. This part of the circuit ensures that the current, and thus the voltage, appearing at the video outputs drops to zero when the delayed SYNC signal is applied. When the current dump is turned off the video signal generated is the normal output of the DACs plus the offset provided by the additional sync reference current. When the current dump turns on it steals all the output current, since it provides a much lower impedance path to GND, so no voltage will appear on the video outputs.

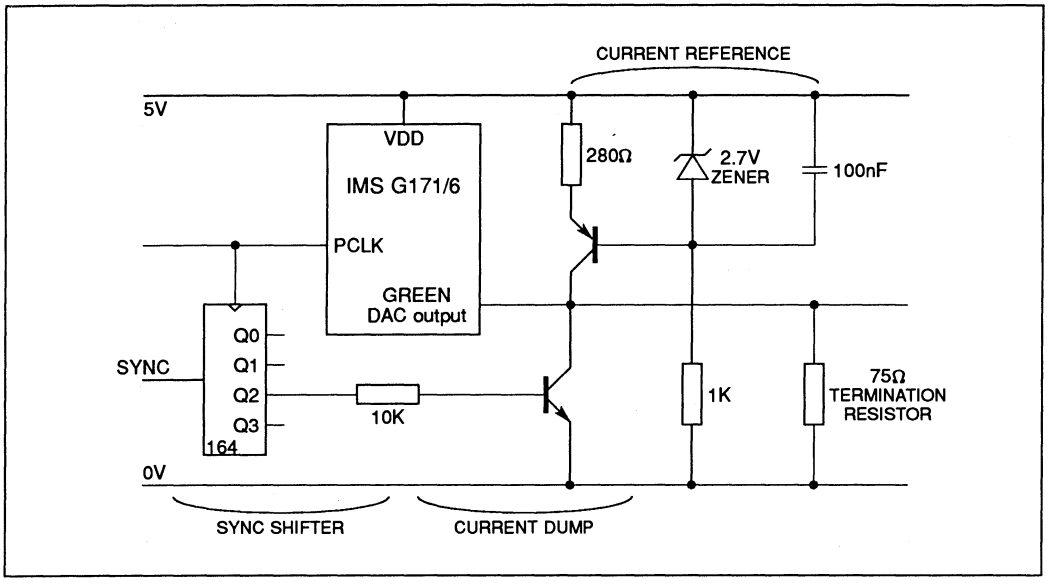


Figure 7.8 Adding an external sync pulse circuit to the G171/6.

Note that it is only necessary to build this circuit round the GREEN analogue output. Although all G17x parts with composite video provide sync signals on all 3 video outputs, most colour monitors only use the information provided on the GREEN channel.

The current reference circuit shown here should be perfectly adequate for most applications. Although the reference voltage established by the Zener diode may only be accurate to ±10% the absolute value of the sync offset should not be critical since most monitors are only A.C. coupled and are fairly tolerant to the magnitude of sync pulse provided. However, if a more accurate sync pedestal is required for a critical application, then the zener reference circuit should be replaced by one of the precision current reference circuits recommended for the IREF pin using either the LM-334 or the TL431.

7.4 Troubleshooting — common problems and their solutions

7.4.1 Unexplained colour changes on the screen

There are a number of possible causes for this effect which is due to corruption of the look-up table contents.

1 **Pixel setup and hold times not being met** — It is essential that the pixel inputs to the CLUT are stable within the window defined by the set-up and hold times on every sampling edge of the pixel clock, even during blanking periods. Any change of the pixel data applied to the device that occurs while the device is sampling its pixel input may result in an invalid address being applied to the look-up table. This asynchronous event may occur if for example the pixel data stream switches between banks of frame store RAM or a video RAM shift register is reloaded under the control of a system asynchronous to the pixel clock. Some mechanism must be put in place to re-synchronise this event to the pixel clock.

2 **Video data going tri-state** — In some system the pixel data stream is made to go tri-state during blanking periods. If there is not a valid TTL level on the pixel inputs on the rising edge of pixel clock an invalid address may be applied to the RAM. The solution to this is either to leave the pixel data enabled, or to use pull-up resistors on the pixel inputs.

3 **Excessive undershoot on pixel inputs** — Due to the mismatch between the low impedence outputs of the TTL device driving the CLUT and the high impedence CLUT inputs, the pixel data port and pixel clock are the most common areas for signal undershoot. If this exceeds 1V this can cause device malfunction, or at worst latch-up. The section on "Pixel Inputs" details termination methods and other recommendations to eliminate this problem.

4 **Asynchronous mask register updates** — On the IMS G170 and IMS G171 devices the pixel mask register must be updated synchronously with the data stream to avoid the possibility of the colour look-up table contents being corrupted. The timing and suggested hardware to achieve this are described in the appropriate datasheet. The pixel mask register synchronisation takes place internally on the IMS G176 and IMS G178 so all accesses to these devices can take place asynchronously without risk of look-up table corruption.

7.4.2 Grey streaks on light/dark boundaries

The possible causes for this effect are as follows:

1 **Noise on VCC and IREF pins of CLUT** — To get a constant full-scale DAC output the voltage between VCC and IREF must remain constant. If there is appreciable noise on VCC supply and the current reference cannot track the variations, this voltage difference will not be constant and incorrect DAC output will occur. In this case coupling capacitors should be used between IREF and VCC, typically a 100nF low-inductance chip capacitor in parallel with a 47μ tantalum should be used.

2 **Unneccessary decoupling on current reference** — Many current reference circuits in reality will have a high enough bandwidth to track any variations in VCC very well. In such cases it may well be that, particularly for high-speed applications, any decoupling between IREF and VCC will serve to slow down the current reference response so that it does not track VCC correctly. It is therefore worth trying both with and without current reference decoupling in applications where this streaking occurs.

3 **Poor quality monitor** — It should be noted that the above problem may not be due to the graphics system design at all. If the monitor used is of poor quality and has insufficient HT regulation then this effect will occur however good the system design is.

quality and reliability

The INMOS quality programme is set up to be attentive to every phase of the semiconductor product life cycle. This includes specific programmes in each of the following areas:

- Total Quality Control (TQC)
- Quality and Reliability in Design
- Document Control
- New Product Qualification
- Product Monitoring Programme
- Production Testing and Quality Monitoring Procedure

A.1 Total quality control (TQC) and reliability programme

Our objective to continuously build improved quality and reliability into every INMOS part has resulted in a comprehensive Quality/Reliability Programme of which we are proud. This programme demonstrates INMOS' serious commitment to supporting the quality and reliability needs of the electronics marketplace.

INMOS is systematically shifting away from a traditional screening approach to quality control and towards one of building in Experimental Design quality through Statistical Process Control (SPC). This new direction was initiated with a vigorous programme of education and scientific method training.

In the first year of the programme approximately 80 INMOS employees worldwide received thorough SPC training. This training has been extended to cover advanced SPC and experimental design. Some of the courses taught are listed below:

- Experimental Design Techniques
- Statistical Process Control Methods
- Quality Concepts
- Problem Solving Techniques
- Statistical Software Analysis Techniques

Today INMOS utilizes experimental design techniques and process control/monitoring throughout its development and manufacturing cycles. The following TQC tools are currently supported by extensive databases and analysis software.

1. Pareto charts
2. Cause/Effect Diagrams
3. Process Flow Charts
4. Run Charts
5. Histograms
6. Correlation Plots
7. Control Charts
8. Experimental Design
9. Process Capability Studies

A.2 Quality and reliability in design

The INMOS quality programme begins with the design of new INMOS products. The following procedures are examples from the INMOS programme to design quality and reliability into every product.

Innovative design techniques are employed to achieve product performance using, whenever possible, state of the art techniques. For example, INMOS uses 300 nanometre gate oxides on its high performance graphics and MICRO products to obtain the reliability inherent in the thicker gate oxide. Additionally, the circuit design engineers work hand in hand with process engineers to optimise the design for the process and the process for the product family. The result of this is a highly reliable design implemented in a process technology

achievable within manufacturing.

INMOS products are designed to have parametric margins beyond the product target specifications. The design performance is verified using simulations of circuit performance over voltage and temperature values beyond those of specified product operation, including verification beyond the military performance range. In addition, the device models are chosen to ensure tolerance to wide variations in process parameters beyond those expected in manufacture.

The design process includes consideration of quality issues such as signal levels available for sensing, reduction of internal noise levels, stored data integrity and testability of all device functions. Electro-static damage protection techniques are included in the design with input protection goals of 2K volts for MIL-STD-883 testing methods. Specific customer requirements can be met by matching their detailed specifications against INMOS designed in margins.

The completion of the design includes the use of INMOS computer aided design software to fully check and verify the design and layout. This improves quality as well as ensuring the timely introduction of new products.

A.3 Document control

The Document Control Department maintains control over all manufacturing specifications, lot travellers, procurement specifications and drawings, reticle tapes and test programmes. New specifications and changes are subject to approval by the Engineering and Manufacturing managers or their delegates. Change is rigorously controlled through an Engineering Change Notice procedure, and QA department managers screen and approve all such changes.

An extensive archiving system ensures that the history of any Change Notice is readily available.

Document Control also has responsibility for controlling in-line documentation in all manufacturing areas which includes distribution of specifications, control of changes and liaison with production control and manufacturing in introducing changed procedures into the line.

Extensive use is made of computer systems to control documentation on an international basis.

A.4 New product qualification

INMOS performs a thorough internal product qualification prior to the delivery of any new product, other than engineering samples of prototypes to customers.

Care is taken to select a representative sample from the final prototype material. This typically consists of three different production lots. Testing is then done to assure the initial product reliability levels are achieved. Product qualifications are done in accordance with MIL-STD-883, methods 5004 and 5005, or CECC/BS9000.

The initial INMOS qualification data, and the ongoing monitor data can be very useful in the user qualification decision process. INMOS also has a very successful history of performing customer qualification testing in-house and performing joint qualification programmes with customers. INMOS remains committed to joint customer/vendor programmes.

A.5 Product monitoring programme

At the levels of quality and reliability performance required today (low PPM and FIT levels), it is essential that a large statistically significant, current product database be maintained. One of the programmes that INMOS uses to accomplish this is the Product Monitoring Programme (PMP).

The PMP is comprehensive ongoing programme of reliability testing. A small sample is pulled from production lots of a particular part type. This population is then used to create the specific samples to put on the various operating and environmental tests. Tests run in this programme include extended temperature operating life, THB and temperature cycle. Efforts are continuing to identify and correlate more accelerated tests to be used

in the PMP.

A.6 Production testing and quality monitoring procedure

A.6.1 Reliability testing

INMOS' primary reliability test method is to bias devices at their maximum rated operating power supply level in a 140° C ambient temperature. A scheme of time varying input signals is used to simulate the complete functional operation of the device. The failure rate is then computed from the results of the operating life test using Arrhenius modelling for each specific failure mechanism known. The failure rate is reported at a temperature that is a typical worst case application environment and is expressed in units of FITs where 1 FIT = 1 Fail in 10E9 device hours, (100 FIT = 0.01%/1000 Hrs). The current database enables the failure rate to be valid over various environmental conditions.

The failure rate goal for INMOS products is 100 FITs or less at product introduction with a 50 FIT level to be attained within one year.

For plastic packaged product, additional testing methods and reliability indices become important. Humidity testing is used to evaluate the relative hermeticity of the package, and thermal cycling tests are used principally to evaluate the durability of the assembly (e.g. die/bond attach).

The Humidity Test comprises of temperature, humidity bias (THB) at 85°C, 85% Relative Humidity, and a 5V static bias configuration selected to maintain the component in a state of minimum power dissipation and enhance the formation of galvanic corrosion. INMOS reliability goals have always been to meet or better the current 'industry standards' and a target of less than 1% failures through 1000 hours of THB at 90% confidence has been set.

The Thermal Cycling tests are performed from −65°C to + 150 °C for 500–1000 cycles, with no bias applied. Thermal Shock tests using a liquid to liquid (Freon) method are cycled between −55°C and + 125 °C. The INMOS Reliability qualification and monitoring goal for the above tests is less than 1% failures at 90% confidence.

A.6.2 Production testing

Electrical testing at INMOS begins while the devices are still in wafer form before being divided into individual die. While in this form, two different types of electrical test are performed.

The Parametric Probe test is to verify that the individual component parameters are within their design limits. This is accomplished by testing special components on the wafer. The results of these tests provide feedback to our wafer fab manufacturing facilities which allows them to ensure that the components used in the actual devices perform within their design limits. This testing is performed on all lots which are processed, and any substandard wafers being discarded. These components are placed in the scribe streets of the wafer so they are destroyed in the dicing operation when they are not of any further use. By placing them there, valuable chip real estate is saved, thereby holding down cost while still providing the necessary data.

The Electrical Probe test performed on all wafers is the test of each individual circuit or chip on every wafer. The defective die are identified so they may be later discarded after the wafer has been separated into individual die. This test fully exercises the circuits for all AC and DC datasheet parameters in addition to verifying functionality.

After the die have been assembled into packages they are again tested in our Final Test operation. In a mature product the typical flow is:

- Preburn-in test
- Burn-in at 140°C
- Final test

- PDA (Percent Defect Allowed)
- Device Symbolisation
- QA Final Acceptance

The temperature setting used for hot testing is selected so that the junction temperature is the same as it would be after thermal stabilisation occurred in the specified environment. This is calculated using the hot temperature power dissipation along with the thermal resistance of the package used. All INMOS product is electrically tested and burned-in prior to shipment. Historically, the industry has selected burn-in times using the MIL Standards as a guide (when the market would support the cost) or on a 'best guess' basis dominated by cost considerations. Whereas INMOS invoke a burn-in reduction exercise to ensure the reduced time has no reliability impact.

A.6.3 Quality monitoring procedure

In the Outgoing Quality Monitoring programme, random samples are pulled from lots, that have been successfully tested to data sheet criteria. Rejected lots are 100% retested and more importantly, failures are analysed and corrective actions identified to prevent the recurence of specific problems.

The extensive series of electrical tests with the associated Burn-in PDA limits and Quality Assurance tests ensure we will be able to continue to improve our high quality and reliability standards.