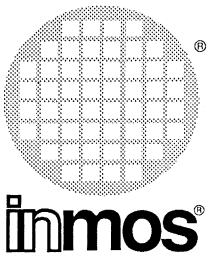

MEMORY DATABOOK

Second Edition 1990

INMOS Databook Series

Transputer Databook
Military Micro-products Databook
Transputer Development and *i*q Systems Databook
Memory Databook
Graphics Databook
Digital Signal Processing Databook
Transputer Applications Notebook: Architecture and Software
Transputer Applications Notebook: Systems and Performance

INMOS is a member of the SGS-THOMSON Microelectronics Group

INMOS document number: 42-1261-01

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Contents

Preface

1 Preface and selection Guide

High performance memory devices form an integral part of the INMOS product range. The INMOS Memory Databook has been published to provide comprehensive information regarding the current range of INMOS memory devices.

CMOS Static RAMs					
	Commercial		Military		
Organisation	Device	Speed(ns)	Device	Speed(ns)	Packages *
4K x 1	IMS1203	25, 35, 45	IMS1203M	25, 35, 45	P, S, A
1K x 4	IMS1223	25, 35, 45	IMS1223M	25, 35, 45	P, S, A
16K x 1	IMS1403	25, 35, 45, 55	IMS1403M(1)	35, 45, 55	P, S, W, N
4K x 4	IMS1423	25, 35, 45, 55	IMS1423M	35, 45, 55	P, S, E, W, Y, N
64K x 1	IMS1600(1)	25, 30, 35, 45, 55	IMS1600M(1)	45, 55, 70	P, S, E, W, N
16K x 4	IMS1620	25, 30, 35, 45, 55	IMS1620M(1)	45, 55, 70	P, S, E, W, N
16K x 4	IMS1624(2)	25, 30, 35, 45, 55	IMS1624M(1)	45, 55, 70	P, S, E, W, N
8K x 8	IMS1630L(2)	45, 55, 70, 100, 120	IMS1630M(1)	45, 55, 70	P, S, H, W, N
Generic 16X5					
64K x 1	IMS1605	15, 20, 25	IMS1605M	20, 25, 35	P, S, E, W, N
16K x 4	IMS1625	15, 20, 25	IMS1625M	20, 25, 35	P, S, E, W, N
16K x 4	IMS1629(2)	15, 20, 25	IMS1629M	20, 25, 35	P, S, E, W, N
16K x 4	IMS1626(2)(3)	15, 20, 25	IMS1626M	20, 25, 35	P, S, E, W, N
16K x 4	IMS1627(2)(4)	15, 20, 25	IMS1627M	20, 25, 35	P, S, E, W, N
8K x 8	IMS1635(2)	15, 20, 25	IMS1635M	20, 25, 35	P, S, E, W, N
8K x 9	IMS1695(2)	15, 20, 25	IMS1695M	20, 25, 35	P, S, E, W, N
256K x 1	IMS1800	25, 30, 35, 45	IMS1800M	30, 35, 45	P, S, E, W, N
64K x 4	IMS1820	25, 30, 35, 45	IMS1820M	30, 35, 45	P, S, E, W, N

NMOS RAMs (Military Only)				
Organisation	Type	Device	Speed(ns)	Packages
16K x 1	Static	IMS1400M	45, 55, 70	S, N, Y
4K x 4	Static	IMS1420M	55, 70	S, N, Y
64K x 1	Dynamic	IMS2600M	100, 120, 150	S, N, K

(1) Low-power/battery back-up versions available.
(2) With Output Enable function.
(3) Separate I/O. Outputs track inputs during write mode.
(4) Separate I/O. High impedance outputs during write mode

* Solder dip lead finish available for all products, refer to Appendix D for details.

The databook comprises a selection guide, INMOS overview and engineering data for the current range of commercial and military memory devices. Additional information is provided detailing military qualification, quality and reliability information and general information covering thermal performance, product numbering, packaging and ordering.

All INMOS military products are designed to satisfy the requirements of a military environment in terms of temperature and reliability under adverse conditions. The majority of the military versions of INMOS memory

devices fully comply with MIL-STD-883C and the US Government Standard Military Drawing (SMD) Program.

In addition to memory devices, the INMOS product range also includes transputer products, digital signal processing devices and graphics devices. For further information concerning INMOS products, please contact your local sales outlet.

INMOS

1 INMOS

1.1 Introduction

INMOS is part of the SGS-THOMSON Microelectronics Group and supplies high performance memory and microprocessor products to companies manufacturing systems in the United States, Europe, Japan and the Far East. The current INMOS product lines include very fast static random access memories (SRAMs), microprocessors called transputers, colour graphics products and digital signal processing devices.

The Company's fabrication facility is at Newport, South Wales with final test facilities located both at Newport and Colorado Springs, Colorado, USA. The corporate headquarters, product design team and worldwide sales and marketing are all based at Bristol, UK.

1.2 Static RAMs

INMOS designs and manufactures a broad range of fast static RAMs, ranging from 4K to 256K bits, in a number of configurations. Revenues from memory products in 1988/89 accounted for approximately one third of total revenues.

As microprocessors become faster, so the demand for fast memory products increases. Despite the semiconductor recession of 1985/86 the number of fast static RAMs shipped worldwide continued to grow throughout the period. The growth of the computer market coupled with the increasing amount of memory in each computer has led to the continued demand for static RAMs. From Dataquest's actual figures of $353M in 1986 for the worldwide fast static RAM market ('fast' includes 70ns cycle time and above) it is anticipated that market growth will continue rising to $763M by 1991. INMOS is the largest supplier of fast SRAMs outside Japan.

1.3 Manufacturing

All products are manufactured at the INMOS Newport, Duffryn facility which began operations in 1983. This is an 8000 square metre building with a 3000 square metre cleanroom operating to Class 10 environment in the work areas. The facility operates a 4 inch wafer line and has the capacity to upgrade to a 6 inch sub micron capability.

To produce high performance products, where each microchip may consist of up to 600,000 transistors, INMOS uses advanced manufacturing equipment. Wafer steppers, plasma etchers and ion implantors form the basis of fabrication.

1.4 Assembly

Sub-contractors in Korea, Taiwan, Hong Kong and the UK are used to assemble devices.

1.5 Test

The final testing of commercial products is carried out at the INMOS Newport, Coed Rhedyn facility. Military final testing takes place in Colorado Springs.

1.6 Quality and Reliability

Stringent controls of quality and reliability provide the customer with early failure rates of less than 1000 ppm and long term reliability rates of better than 100 FITs (one FIT is one failure per 1000 million device hours). Requirements for military and space applications are even more stringent.

1.7 Military

Most INMOS static RAMs are available in military versions processed in full compliance with MIL-STD-883C. INMOS also supports the US Government Defense Electronics Supply Center (DESC) Standard Military

Drawing (SMD) program and is an approved supplier of a range of the SMDs already established by DESC.

1.8 Future developments

1.8.1 Research and Development

INMOS has achieved technical success based on a position of leadership in products and process technology in conjunction with substantial research and development investment. R and D investment has averaged 18 percent of revenues since inception and it is anticipated that future investment levels will be maintained at this level.

1.8.2 Process developments

One aspect of the work of the Technology Development Group at Newport is to scale the present technology to 1.0 micron for products to be manufactured in 1989/90. Additionally, work is in progress on the development of 0.8 micron CMOS technology.

A new process technology developed in Colorado Springs for an advanced range of 256K static RAMs and other products has successfully transferred to Newport. A new 64K static RAM based on the new technology will also be brought into production.

1.9 Package developments

Where surface mount technology is desirable, the range of fast 64K static RAMs are now offered in SOJ packaging.

commercial RAMs

IMS1203
CMOS
High Performance
4K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 1 Bit Organization
- 25, 35, and 45 nsec Access Times
- 25, 35, and 45 nsec Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- 18 Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

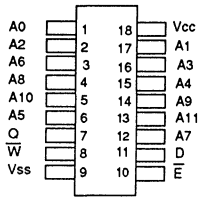
DESCRIPTION

The INMOS IMS1203 is a high performance 4Kx1 CMOS static RAM. The IMS1203 allows speed enhancements to existing 4Kx1 applications with the additional benefit of reduced power consumption.

The IMS1203 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1203 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

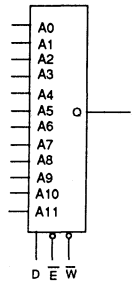
The IMS1203M is a MIL-STD-883 version intended for military applications.

PIN CONFIGURATION

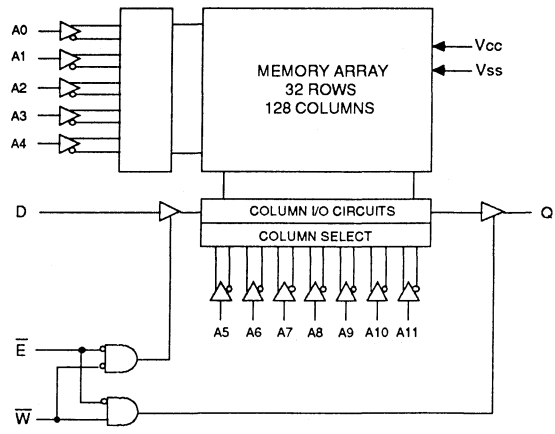


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc POWER
$\overline{W}$	WRITE ENABLE	Vss GROUND
D	DATA INPUT	
$\overline{E}$	CHIP ENABLE	
Q	DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on Q . . . . . −1.0 to (V_{CC} + 0.5V)
Temperature Under Bias. . . . . −55°C to 125°C
Storage Temperature . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc +.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current		80	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\overline{E} \geq V_{IH}$ All other inputs $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		6	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All other inputs at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		13	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ Inputs cycling at $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	$I_{OUT} = -4mA$
V_{OL}	Output Logic "0" Voltage		0.4	V	$I_{OUT} = 12mA$

Note a: I_{CC} is dependent on output loading and cycle rate. the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE ($T_A = 25°C$, f = 1.0 MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

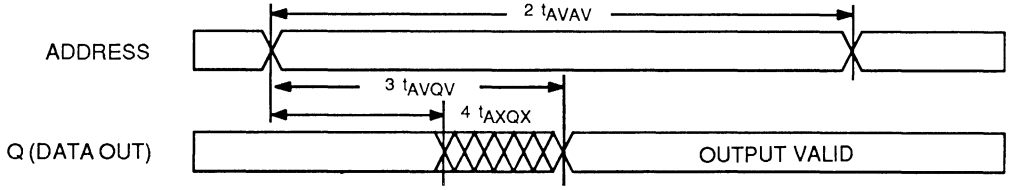
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

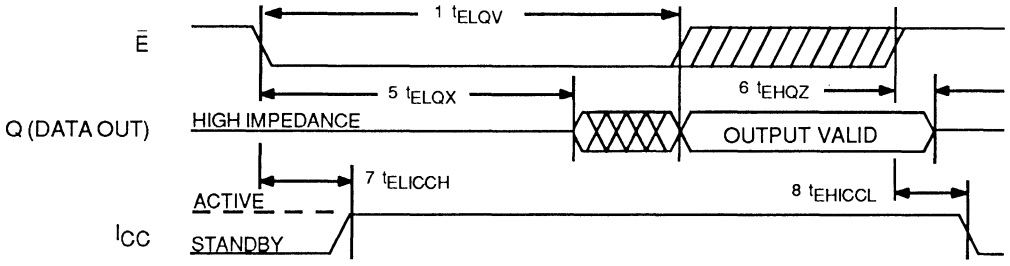
NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	30	0	30	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		20		20		20	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



DEVICE OPERATION

The IMS1203 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), a data in (D_{IN}) and a data out (D_{OUT}). The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one memory cell out of 4096. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

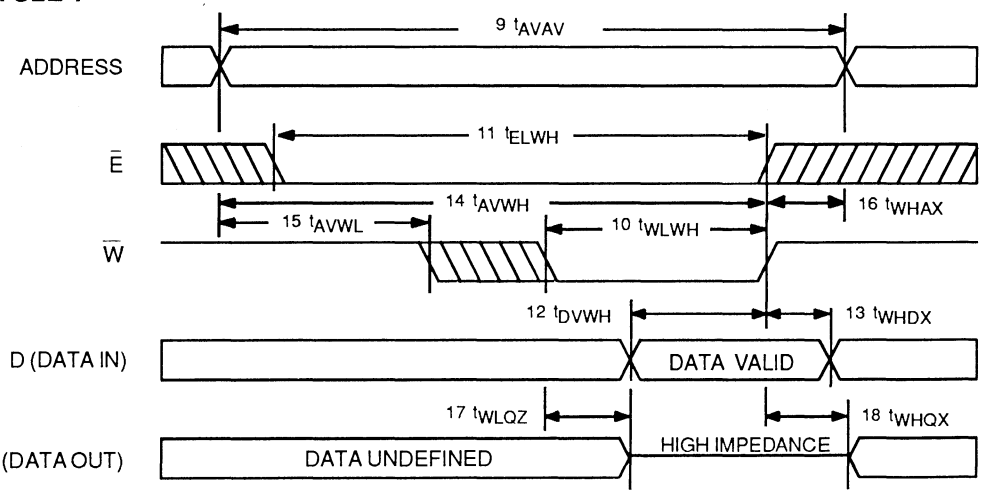
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1203 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to fall. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of

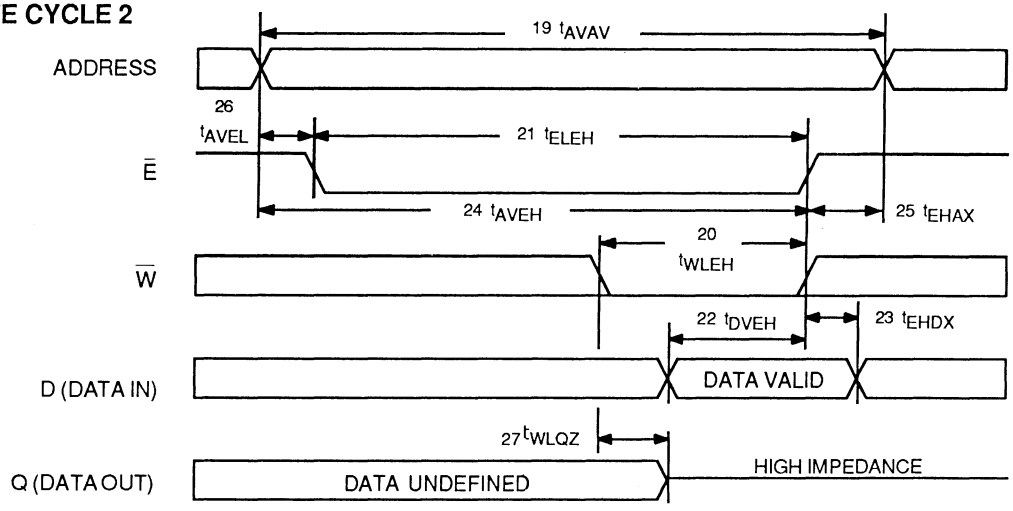
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1203-25		1203-35		1203-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1203, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1203. The impedance in the decoupling path from the power pin (18) through the decoupling capacitor to the ground pin (9) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1203 have very high frequency

components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

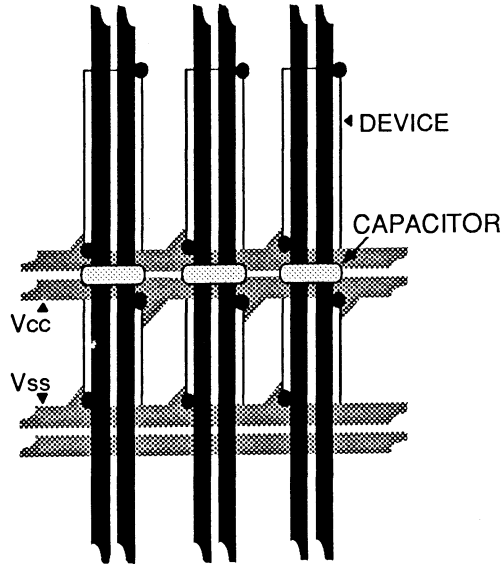
The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

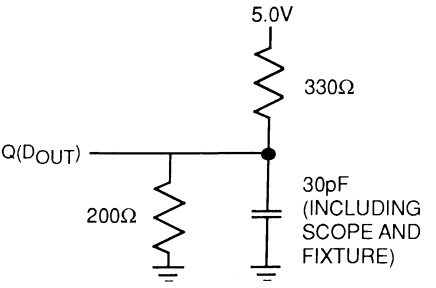
The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

FIGURE 1. OUTPUT LOAD



DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1203	25ns	PLASTIC DIP	IMS1203P-25
	25ns	CERAMIC DIP	IMS1203S-25
	35ns	PLASTIC DIP	IMS1203P-35
	35ns	CERAMIC DIP	IMS1203S-35
	45ns	PLASTIC DIP	IMS1203P-45
	45ns	CERAMIC DIP	IMS1203S-45

IMS1223
CMOS
High Performance
1K x 4 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 1K x 4 Bit Organization
- 25, 35, and 45 nsec Access Times
- 25, 35, and 45nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Output
- Three-state Output
- 18 Pin, 300-mil DIP
- Single +5V ± 10% Operation
- Power Down Function

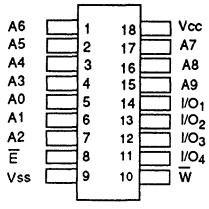
DESCRIPTION

The INMOS IMS1223 is a high performance 1Kx4 CMOS static RAM. The IMS1223 allows speed enhancements to existing 1Kx4 applications with the additional benefit of reduced power consumption.

The IMS1223 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1223 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

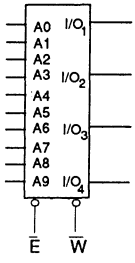
The IMS1223M is a MIL-STD-883 version intended for military applications.

PIN CONFIGURATION

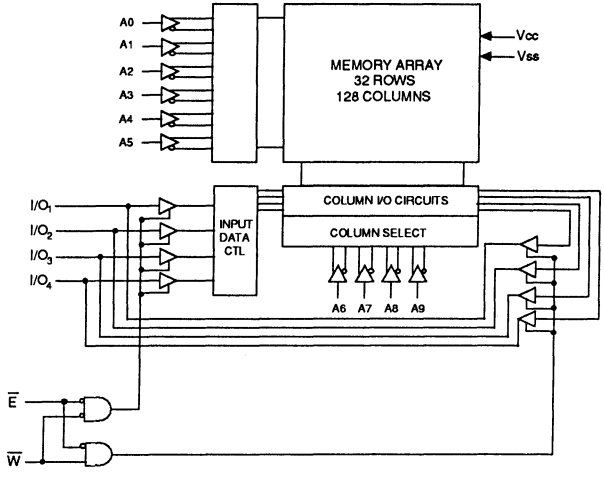


DIP

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_9	ADDRESS INPUTS	Vcc	POWER
W̄	WRITE ENABLE	Vss	GROUND
Ē	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −2.0 to 7.0V
Voltage on Q . . . . . −1.0 to (V_{CC} + 0.5V)
Temperature Under Bias . . . . . −55°C to 125°C
Storage Temperature . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC}+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	**-1.0***		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	**400 linear ft/min air flow**

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC_1}	Average V_{CC} Power Supply Current		100	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC_2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\overline{E} \geq V_{IH}$ All other inputs V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC_3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		6	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ All other inputs at V_{IN} ≤ 0.2V or ≥ (V_{CC} −0.2V)
I_{CC_4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		8	mA	$\overline{E} \geq (V_{CC} - 0.2V)$ Inputs cycling at V_{IN} ≤ 0.2V or ≥ (V_{CC} −0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = −4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

CAPACITANCE (T_A = 25°C, f = 1.0 MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

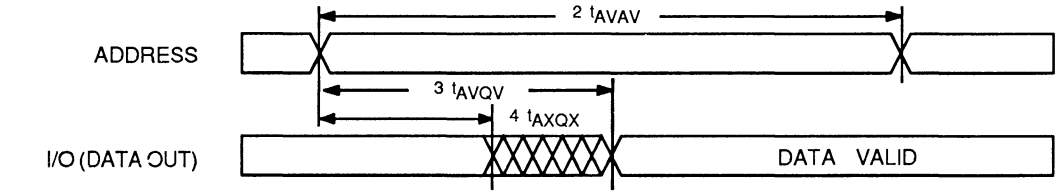
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

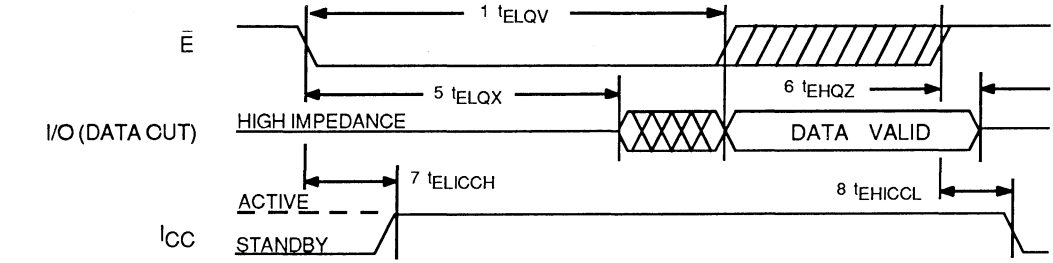
NO.	SYMBOL		PARAMETER	1223-25		1223-35		1223-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	0		0		0		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive		15		20		20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		20		20		20	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



DEVICE OPERATION

The IMS1223 has two control inputs: Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), ten address inputs (A_0-A_9), and four data I/O lines. The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the ten address inputs are decoded to select one 4 bit word out of 1024. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the outputs are disabled, and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

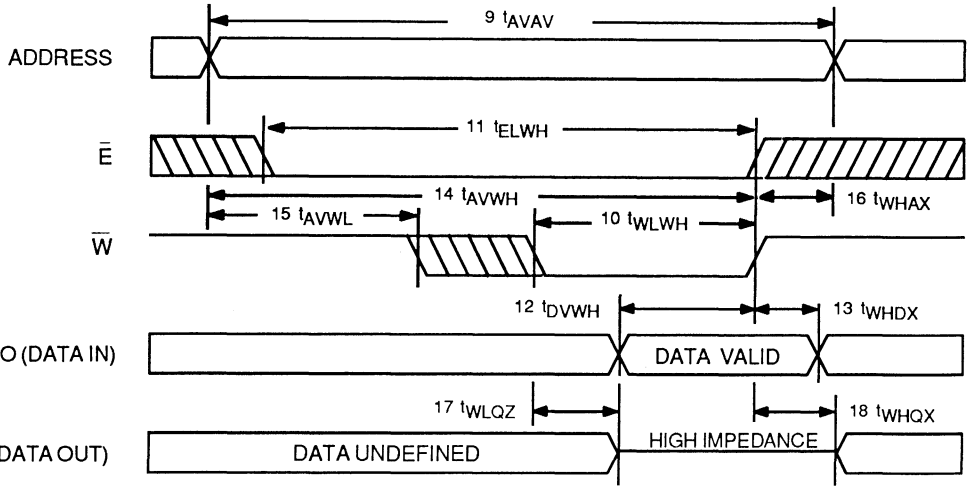
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1223-25		1223-35		1223-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		35		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	10		15		15		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		25		35		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable		15		20		20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	5		5		5		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1223 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to a low. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common I/O configurations. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

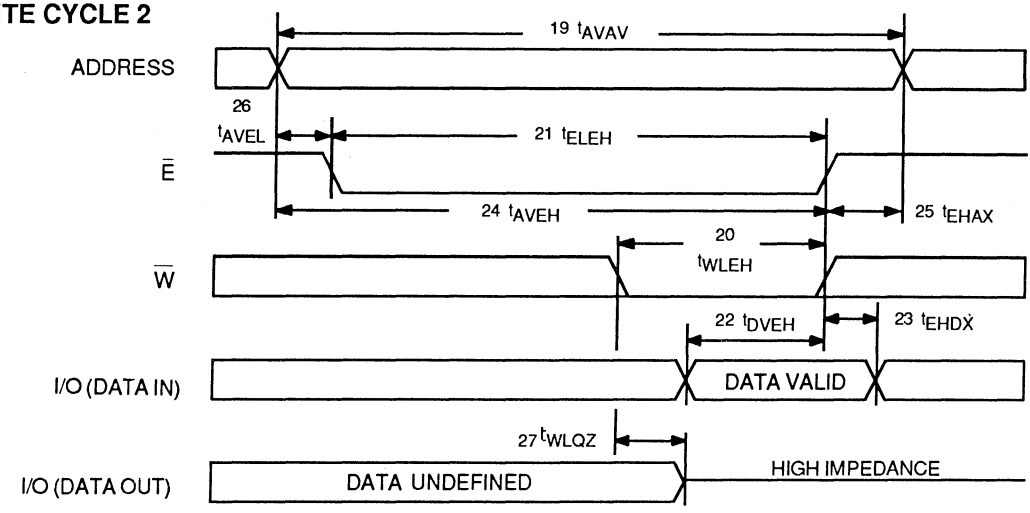
RECOMMENDED AC OPERATING CONDITIONS ($-0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1223-25		1223-35		1223-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		25		35		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		15		15		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		35		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable		15		20		20	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1223, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1223. The impedance in the decoupling path from the power pin (18) through the decoupling capacitor to the ground pin (9) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1223 have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy

for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad. and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

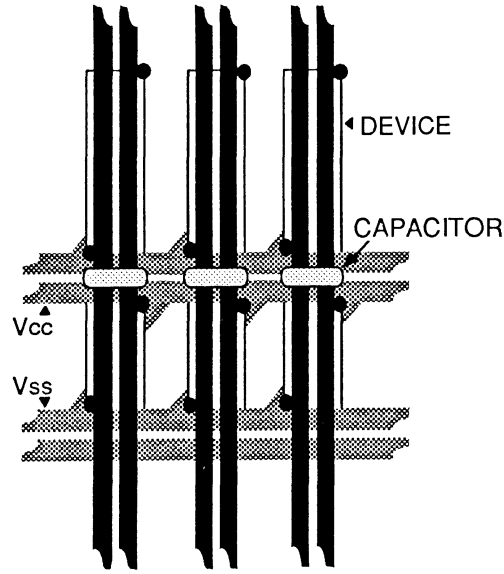
The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

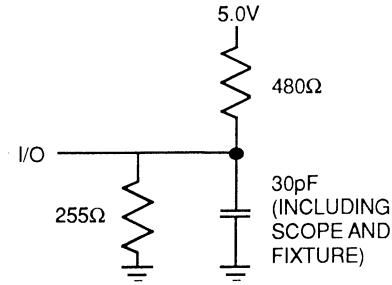
The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1223	25ns	PLASTIC DIP	IMS1223P-25
	25ns	CERAMIC DIP	IMS1223S-25
	35ns	PLASTIC DIP	IMS1223P-35
	35ns	CERAMIC DIP	IMS1223S-35
	45ns	PLASTIC DIP	IMS1223P-45
	45ns	CERAMIC DIP	IMS1223S-45

IMS1403

CMOS High Performance 16K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 1 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

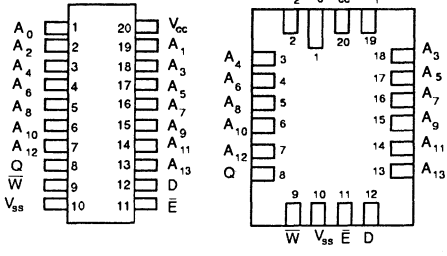
DESCRIPTION

The INMOS IMS1403 is a high performance 16K x 1 CMOS Static RAM. The IMS1403 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1403 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

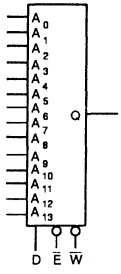
The IMS1403M and IMS1403LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION

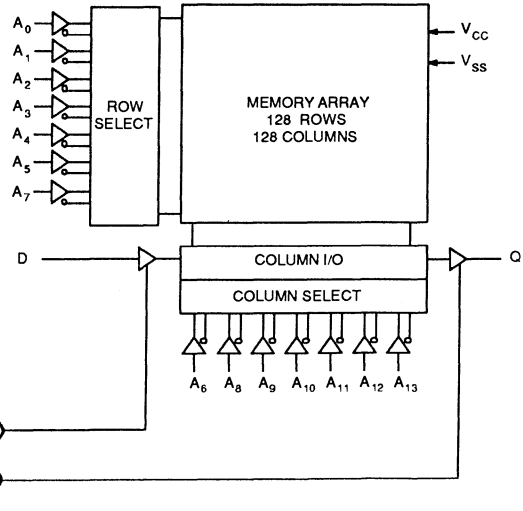


DIP CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	V_{CC}	POWER
$\overline{E}$	CHIP ENABLE	V_{SS}	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q .....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		75	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	$\bar{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\bar{E} \geq$ (Vcc - 0.2). All other inputs at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E} \geq$ (Vcc - 0.2). Inputs cycling at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OL} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OH} = 16mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

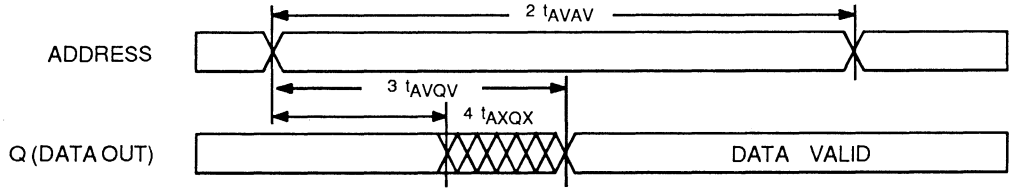
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

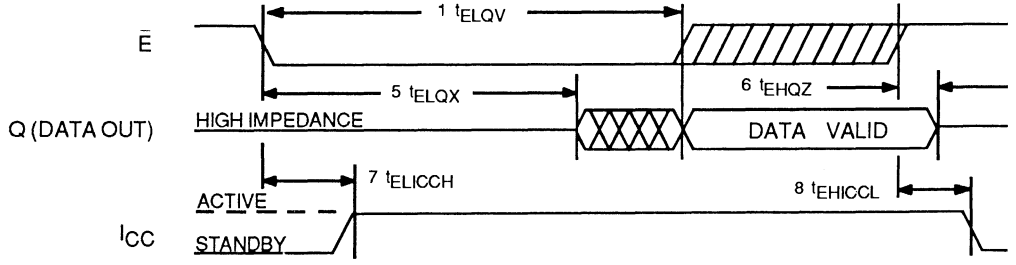
NO.	SYMBOL		PARAMETER	1403-25		1403-35		1403-45		1403-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		40		50		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		40		50	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	20	0	20	0	25	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable To Power Down		30		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



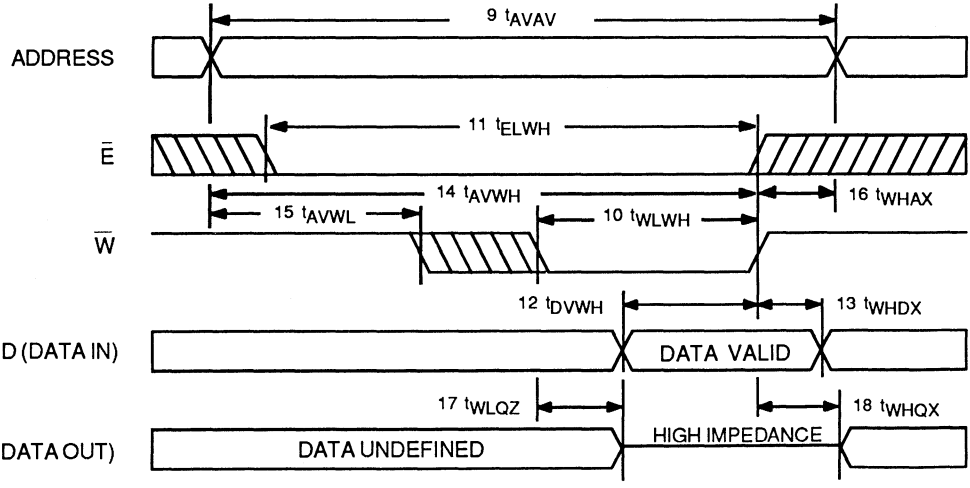
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) (V_{CC} = 5.0V ± 10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1403-25		1403-35		1403-45		1403-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	20		30		40		50		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		35		45		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		15		15		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		30		35		45		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		0		ns	i

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



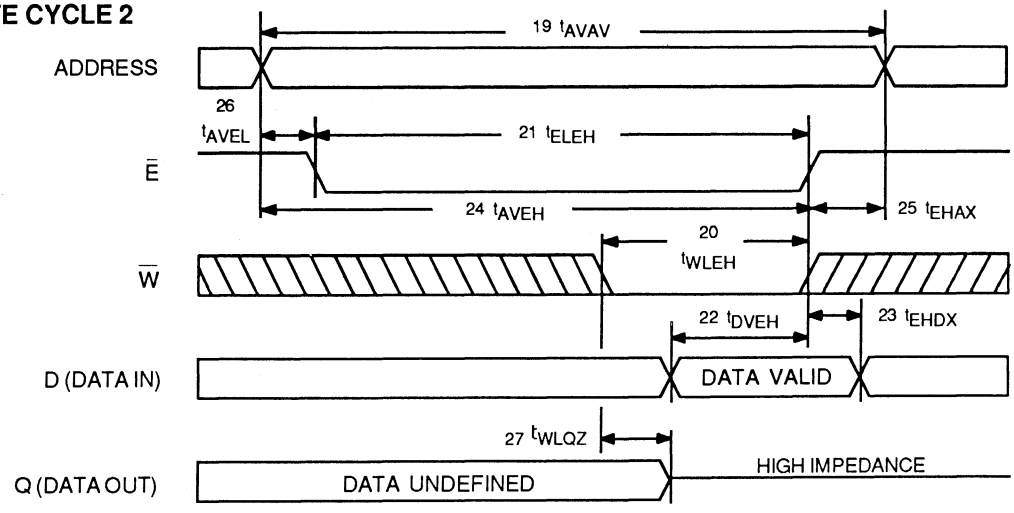
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1403-25		1403-35		1403-45		1403-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	20		30		40		50		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		35		45		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		15		15		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		35		45		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	20	0	25	ns	f, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1403 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), fourteen address inputs (A_0 - A_{13}), a Data in (D) and a Data out (Q). The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the fourteen address inputs are decoded to select one bit out of 16K bits. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle of the IMS1403 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to a low. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

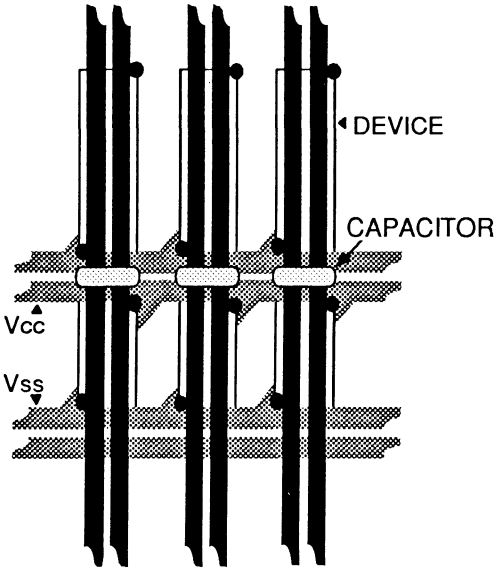
APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1403, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1403. The impedance in the decoupling path from the power pin through the decoupling capacitor, to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1403 have very high frequency components, the line inductance is the dominating factor.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

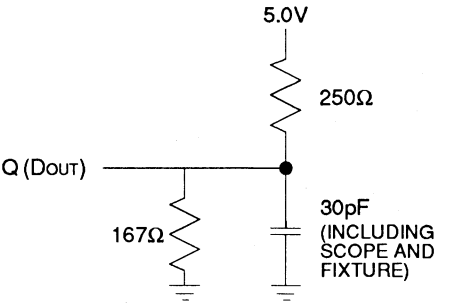
TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1403	25ns	PLASTIC DIP	IMS1403P-25
	25ns	CERAMIC DIP	IMS1403S-25
	25ns	CERAMIC LCC	IMS1403W-25
	35ns	PLASTIC DIP	IMS1403P-35
	35ns	CERAMIC DIP	IMS1403S-35
	35ns	CERAMIC LCC	IMS1403W-35
	45ns	PLASTIC DIP	IMS1403P-45
	45ns	CERAMIC DIP	IMS1403S-45
	45ns	CERAMIC LCC	IMS1403W-45
	55ns	PLASTIC DIP	IMS1403P-55
	55ns	CERAMIC DIP	IMS1403S-55
	55ns	CERAMIC LCC	IMS1403W-55

IMS1423
High Performance 4K x 4 CMOS Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 4K x 4 Bit Organization
- 25, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP & SOJ (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Pin Compatible with IMS1420

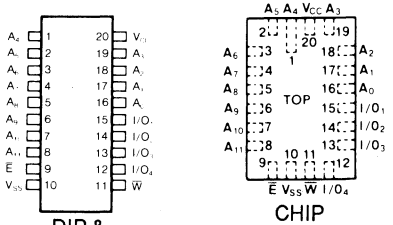
DESCRIPTION

The INMOS IMS1423 is a high performance 4K x 4 CMOS static RAM. The IMS1423 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

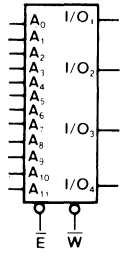
The IMS1423 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1423M is a MIL-STD-883 version intended for military applications that demand superior performance and reliability.

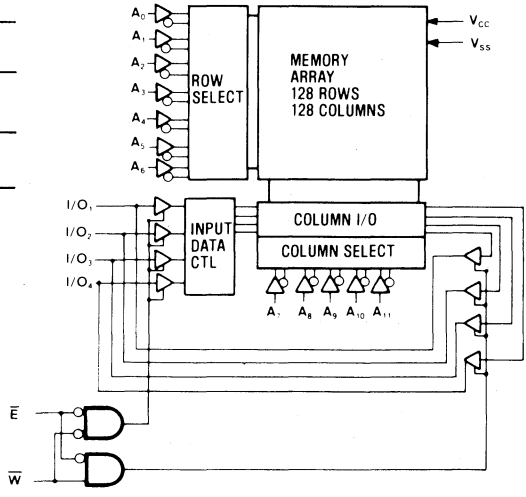
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} ..... −2.0 to 7.0V
Voltage on I/O (Pins 13-16)..... −1.0 to (V_{CC} + 0.5V)
Temperature Under Bias..... −55°C to 125°C
Storage Temperature (Ambient)..... −65°C to 150°C
Power Dissipation..... 1W
DC Output Current..... 25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc + .5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		105 100 100	mA mA mA	t_{AVAV} = 25ns t_{AVAV} = 35ns t_{AVAV} = 45ns & 55ns
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		15	mA	$\bar{E} \geq V_{IH}$ All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\bar{E} \geq (V_{CC} - 0.2)$ All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\bar{E} \geq (V_{CC} - 0.2)$ Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

Input Pulse Levels..... V_{SS} to 3V
Input Rise and Fall Times..... 5ns
Input and Output Timing Reference Levels..... 1.5V
Output Load..... See Figure 1

CAPACITANCE[b] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

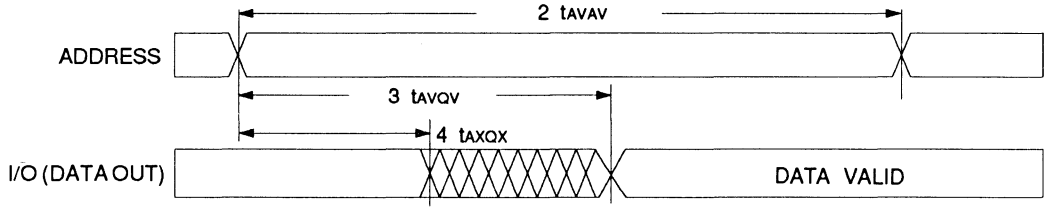
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

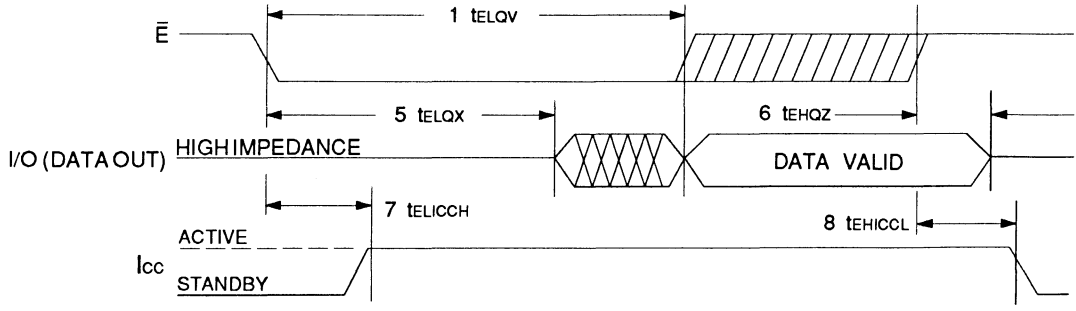
NO.	SYMBOL		PARAMETER	1423-25		1423-35		1423-45		1423-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		40		50		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		40		50	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		3		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	15	0	15	0	15	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Disable To Power Down		30		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1 [c,d]



READ CYCLE 2 [c]



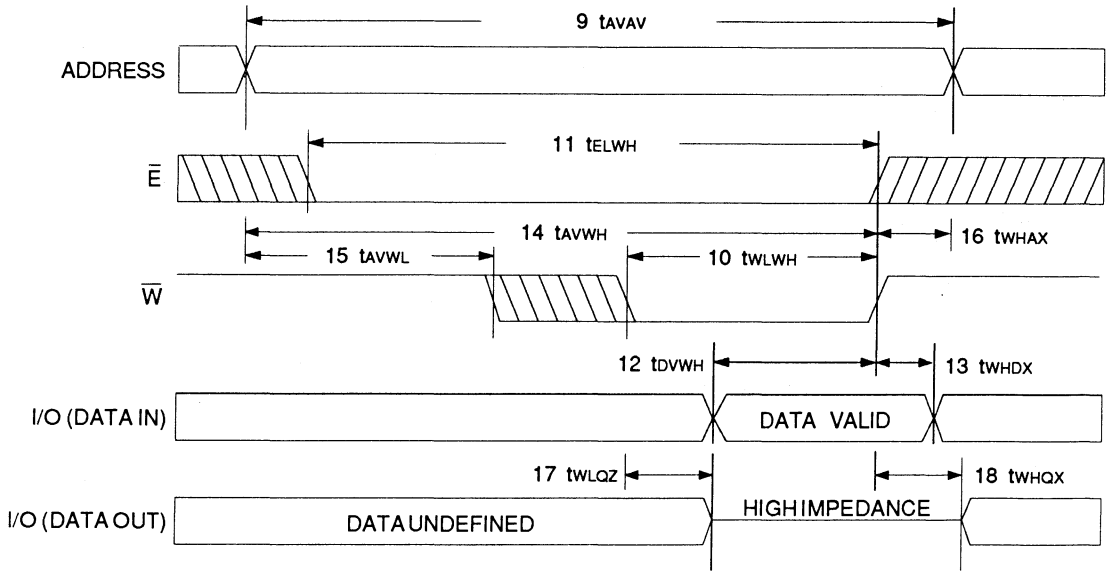
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1423-25		1423-35		1423-45		1423-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		40		50		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		35		45		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		25		35		45		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	10		13		15		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	2		2		3		3		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		25		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	2		3		5		5		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	15	0	20	0	25	ns	f,j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	6		6		6		6		ns	i

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



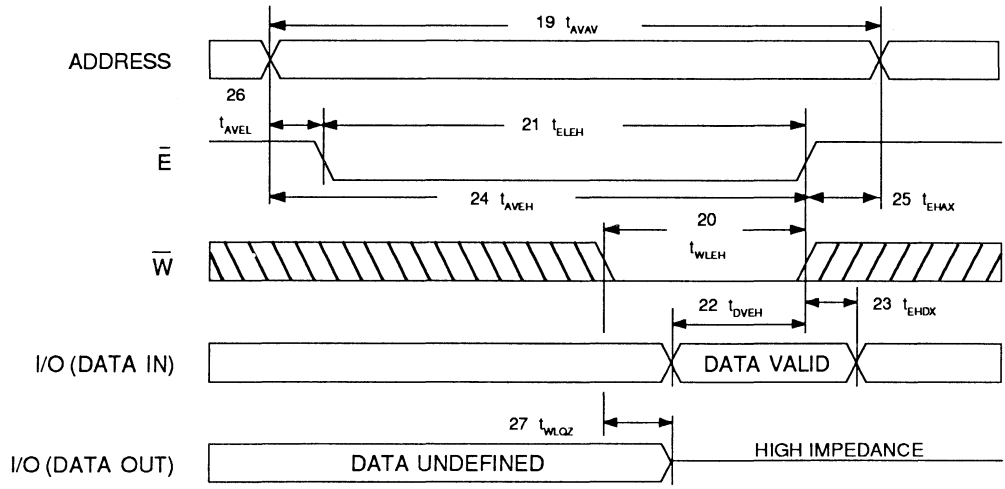
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1423-25		1423-35		1423-45		1423-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		40		50		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		35		45		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		35		45		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		13		15		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	3		3		3		5		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		25		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	2		3		5		5		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	15	0	20	0	25	ns	f,j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1423 has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), and four Data I/O lines. The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4K words. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

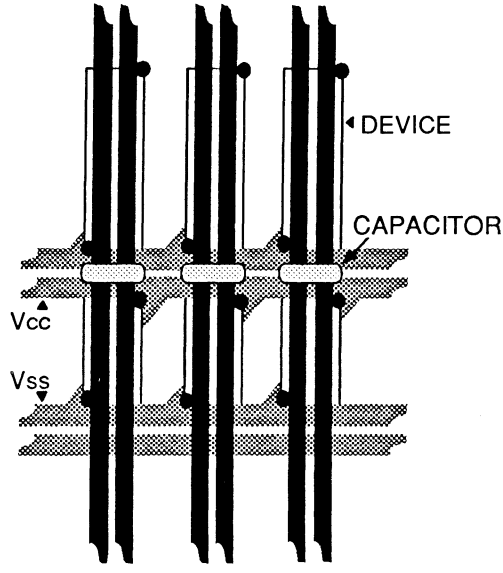
The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1423 is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high level to a low level. In the case of $\overline{W}$ falling last, the output buffers will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLQZ} to avoid bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the outputs of the memory become active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

APPLICATION

It is imperative, when designing with any very high speed memory such as the IMS1423, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS1423. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1423 have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

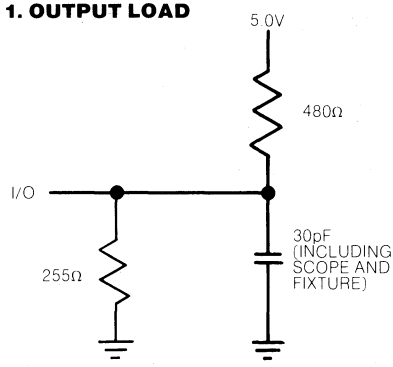
TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1423	25ns	PLASTIC DIP	IMS1423P-25
	25ns	PLASTIC SOJ	IMS1423E-25
	25ns	CERAMIC DIP	IMS1423S-25
	25ns	CERAMIC LCC	IMS1423W-25
	35ns	PLASTIC DIP	IMS1423P-35
	35ns	PLASTIC SOJ	IMS1423E-35
	35ns	CERAMIC DIP	IMS1423S-35
	35ns	CERAMIC LCC	IMS1423W-35
	45ns	PLASTIC DIP	IMS1423P-45
	45ns	PLASTIC SOJ	IMS1423E-45
	45ns	CERAMIC DIP	IMS1423S-45
	45ns	CERAMIC LCC	IMS1423W-45
	55ns	PLASTIC DIP	IMS1423P-55
	55ns	PLASTIC SOJ	IMS1423E-55
	55ns	CERAMIC DIP	IMS1423S-55
	55ns	CERAMIC LCC	IMS1423W-55

IMS1600
IMS1601L
CMOS
High Performance
64K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 64K x 1 Bit Organization
- 25, 30, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ
- Battery Backup Operation - 2V Data Retention (L version only)

DESCRIPTION

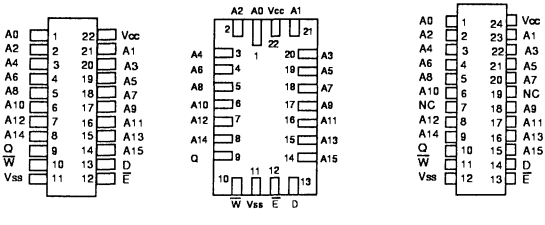
The INMOS IMS1600 is a high performance 64K x 1 CMOS Static RAM. The IMS1600 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1600 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1601L is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1600M and IMS1601LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION

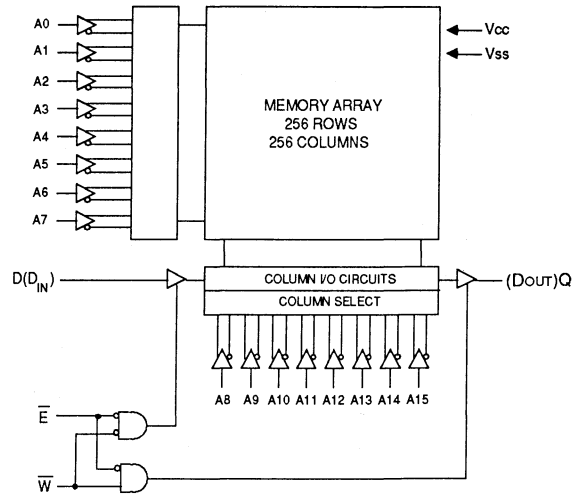


DIP CHIP CARRIER SOJ

PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		77 70	mA mA	tAVAV = 25ns and 30ns (PRELIM) tAVAV = 35, 45 and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\overline{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
	IMS1601L version		15		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E} \geq$ (Vcc - 0.2). All other inputs at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
	IMS1601L version		2		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	$\overline{E} \geq$ (Vcc - 0.2). Inputs cycling at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
	IMS1601L version		5		
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OL} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OH} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

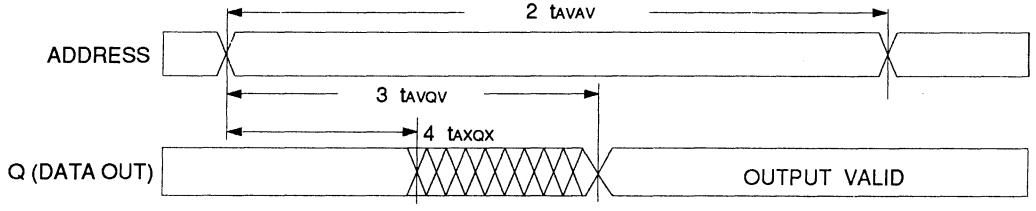
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

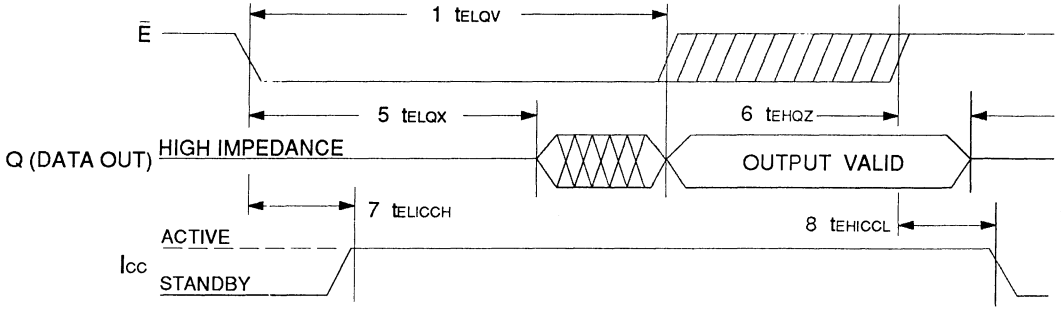
No.	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 & 1601-35 MIN	IMS 1600-35 & 1601-35 MAX	IMS 1600-45 & 1601-45 MIN	IMS 1600-45 & 1601-45 MAX	IMS 1600-55 & 1601-55 MIN	IMS 1600-55 & 1601-55 MAX	UNITS	NOTES
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		30		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		30		35		45		55		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		30		35		45		55	ns	d
4	t_{AXQX}	t_{OH}	O/P Hold After Address Change	3		3		5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to O/P Active	3		3		5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to O/P Inactive	0	15	0	15	0	20	0	25	0	30	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		25		30		35		45		55	ns	j
		t_T	I/P Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



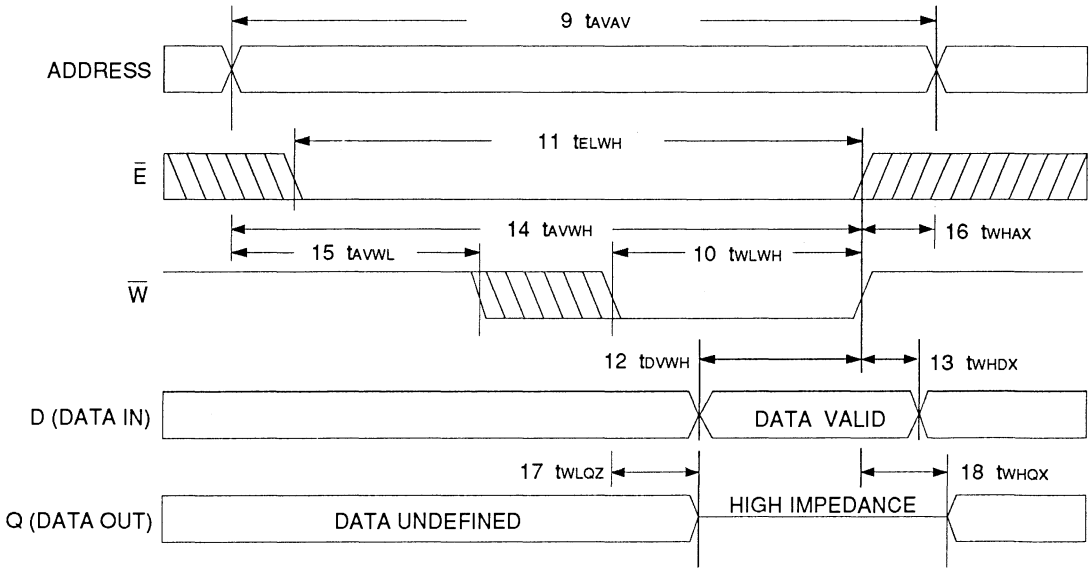
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 & 1601-35 MIN	IMS 1600-35 & 1601-35 MAX	IMS 1600-45 & 1601-45 MIN	IMS 1600-45 & 1601-45 MAX	IMS 1600-55 & 1601-55 MIN	IMS 1600-55 & 1601-55 MAX	UNITS	NOTES
9	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
10	tWLWH	tWP	Write Plus Width	20		20		20		20		25		ns	
11	tELWH	tCW	Chip Enable to End of Write	20		20		30		30		30		ns	
12	tDVWH	tDW	Data Setup to End of Write	15		15		15		20		20		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
14	tAVWH	tAW	Address Setup End of Write	20		20		25		25		30		ns	
15	tAVWL	tAS	Address Setup to Start of Write	5		5		5		5		5		ns	
16	tWHAX	tWR	Address Hold after End of Write	5		5		5		5		5		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j
18	tWHQX	tOW	Write Enable to Output Disable	0		0		0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



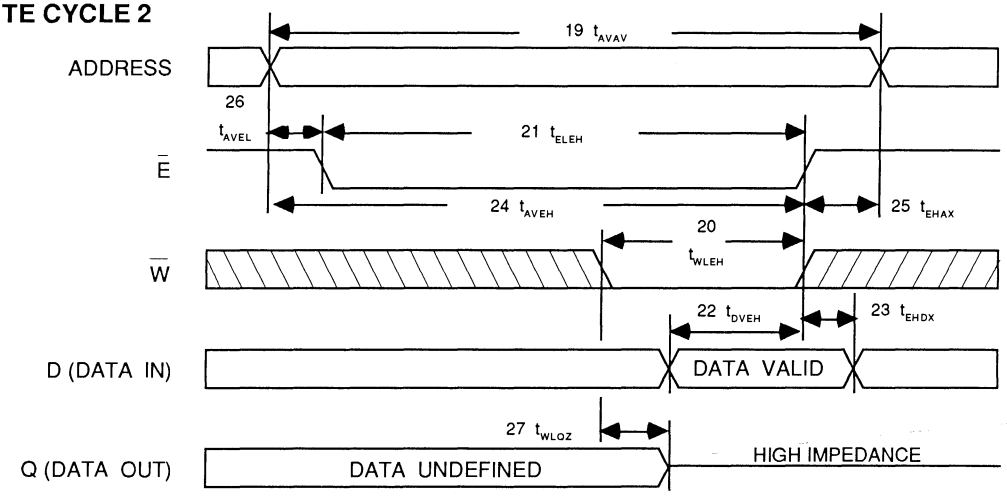
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1600-25 PRELIM MIN	IMS 1600-25 PRELIM MAX	IMS 1600-30 PRELIM MIN	IMS 1600-30 PRELIM MAX	IMS 1600-35 1601-35 MIN	IMS 1600-35 1601-35 MAX	IMS 1600-45 1601-45 MIN	IMS 1600-45 1601-45 MAX	IMS 1600-55 1601-55 MIN	IMS 1600-55 1601-55 MAX	UNITS	NOTES
19	tAVAV	t WC	Write Cycle Time	25		30		35		45		55		ns	
20	tWLEH	t WP	Write Plus Width	20		20		20		20		25		ns	
21	tELEH	t CW	Chip Enable to End of Write	20		20		30		30		30		ns	
22	tDVEH	t DW	Data Setup to End of Write	15		15		15		20		20		ns	
23	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVEH	t AW	Address Setup to End of Write	20		20		30		30		30		ns	
25	tEHAX	t WR	Address Hold after End of Write	5		5		5		5		5		ns	
26	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1600 has two control inputs, Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), a data in (D) and a data out (Q).

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one memory cell out of 65,536. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1600 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1600. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

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Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

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Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) ($0°C \le T_A \le 70°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		8	100	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		5	70	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µs from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION

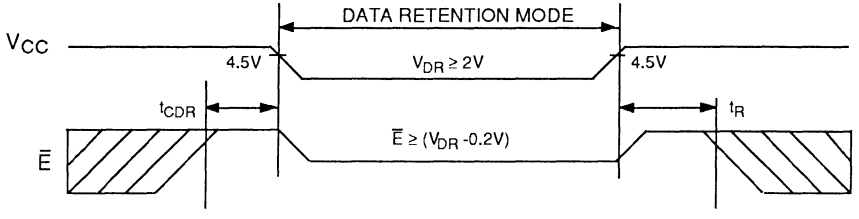
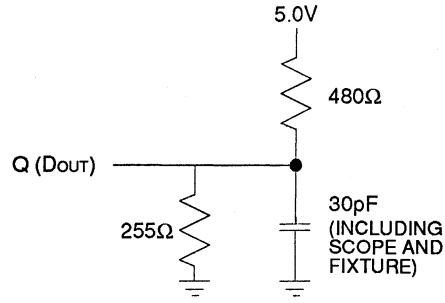


FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS1600 IMS1601L	25ns	PLASTIC DIP	IMS1600P-25	
	25ns	CERAMIC DIP	IMS1600S-25	
	25ns	CERAMIC LCC	IMS1600W-25	
	25ns	PLASTIC SOJ	IMS1600E-25	
	30ns	PLASTIC DIP	IMS1600P-30	
	30ns	CERAMIC DIP	IMS1600S-30	
	30ns	CERAMIC LCC	IMS1600W-30	
	30ns	PLASTIC SOJ	IMS1600E-30	
	35ns	PLASTIC DIP	IMS1600P-35	IMS1601LP35
	35ns	CERAMIC DIP	IMS1600S-35	IMS1601LS35
	35ns	CERAMIC LCC	IMS1600W-35	IMS1601LW35
	35ns	PLASTIC SOJ	IMS1600E-35	IMS1601LE35
	45ns	PLASTIC DIP	IMS1600P-45	IMS1601LP45
	45ns	CERAMIC DIP	IMS1600S-45	IMS1601LS45
	45ns	CERAMIC LCC	IMS1600W-45	IMS1601LW45
	45ns	PLASTIC SOJ	IMS1600E-45	IMS1601LE45
	55ns	PLASTIC DIP	IMS1600P-55	IMS1601LP55
	55ns	CERAMIC DIP	IMS1600S-55	IMS1601LS55
	55ns	CERAMIC LCC	IMS1600W-55	IMS1601LW55
	55ns	PLASTIC SOJ	IMS1600E-55	IMS1601LE55

IMS1620
CMOS
High Performance
16K x 4 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 4 Bit Organization
- 25, 30, 35, 45 and 55 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ

DESCRIPTION

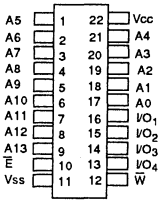
The INMOS IMS1620 is a high performance 16K x 4 CMOS Static RAM. The IMS1620 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1620 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1620 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

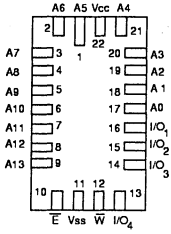
The IMS1624 is the functional equivalent of the IMS1620 with the addition of an Output Enable input.

The IMS1620M and IMS1620LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION

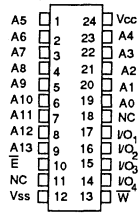


DIP



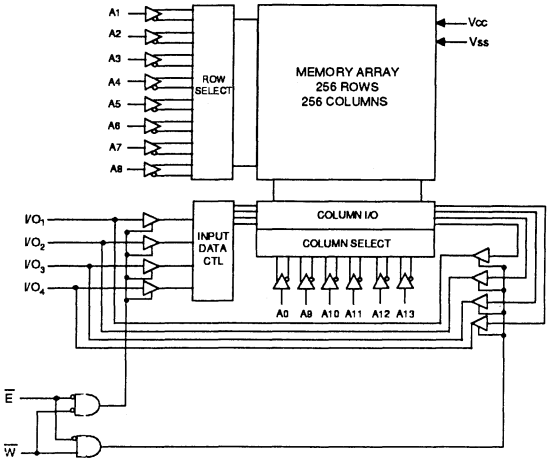
CHIP CARRIER

LOGIC SYMBOL



SOJ

BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	I/O	DATA IN/OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to Vcc+0.5
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		110 100	mA mA	t_{AVAV} = 25ns and 30ns t_{AVAV} = 35, 45 and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\bar{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\bar{E} \geq (V_{CC} - 0.2)$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		17	mA	$\bar{E} \geq (V_{CC} - 0.2)$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

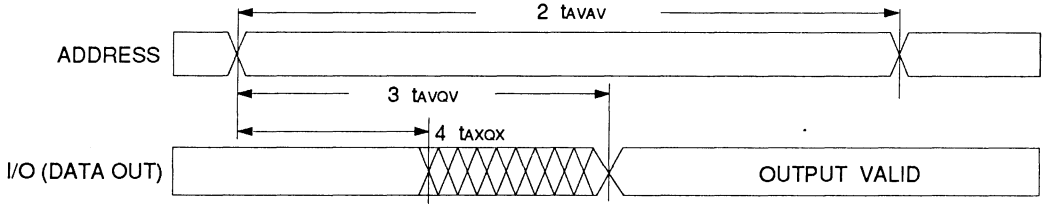
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

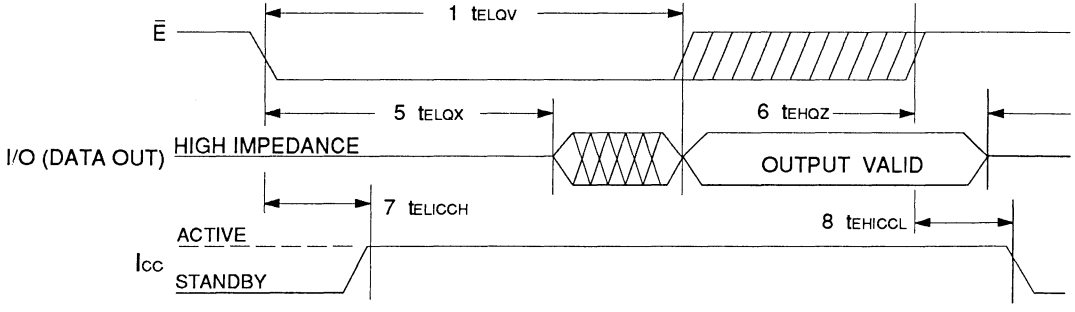
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1620-25 MIN	IMS 1620-25 MAX	IMS 1620-30 MIN	IMS 1620-30 MAX	IMS 1620-35 MIN	IMS 1620-35 MAX	IMS 1620-45 MIN	IMS 1620-45 MAX	IMS 1620-55 MIN	IMS 1620-55 MAX	UNITS	NOTES
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45		55	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		55		ns	c
3	tAVQV	tAA	Address Access Time		25		30		35		45		55	ns	d
4	tAXQX	tOH	O/P Hold After Address Change	5		5		5		5		5		ns	
5	tELQX	tLZ	Chip Enable to O/P Active	5		5		5		5		5		ns	j
6	tEHQZ	tHZ	Chip Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
7	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
8	tEHICCL	tPD	Chip Enable to Power Down		25		30		35		45		55	ns	j
		tT	Input Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



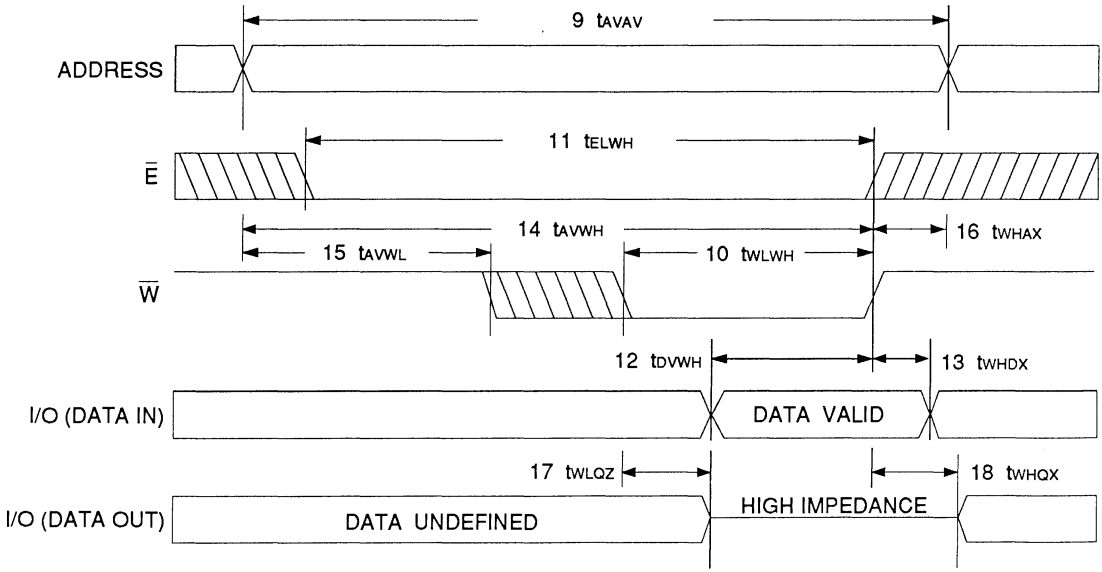
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ T_A ≤ 70°C) (V_{CC} = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1620-25 MIN	IMS 1620-25 MAX	IMS 1620-30 MIN	IMS 1620-30 MAX	IMS 1620-35 MIN	IMS 1620-35 MAX	IMS 1620-45 MIN	IMS 1620-45 MAX	IMS 1620-55 MIN	IMS 1620-55 MAX	UNITS	NOTES
9	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
10	tWLWH	tWP	Write Pulse Width	20		20		30		30		40		ns	
11	tELWH	tCW	Chip Enable to End of Write	20		20		30		30		40		ns	
12	tDVWH	tDW	Data Setup to End of Write	13		15		15		20		25		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
14	tAVWH	tAW	Address Setup End of Write	20		25		30		30		40		ns	
15	tAVWL	tAS	Address Setup to Start of Write	0		0		0		0		0		ns	
16	tWHAX	tWR	Address Hold after End of Write	5		5		5		0		0		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	20	0	20	0	25	ns	f,j
18	tWHQX	tOW	Write Enable to Output Disable	0		0		0		0		0		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



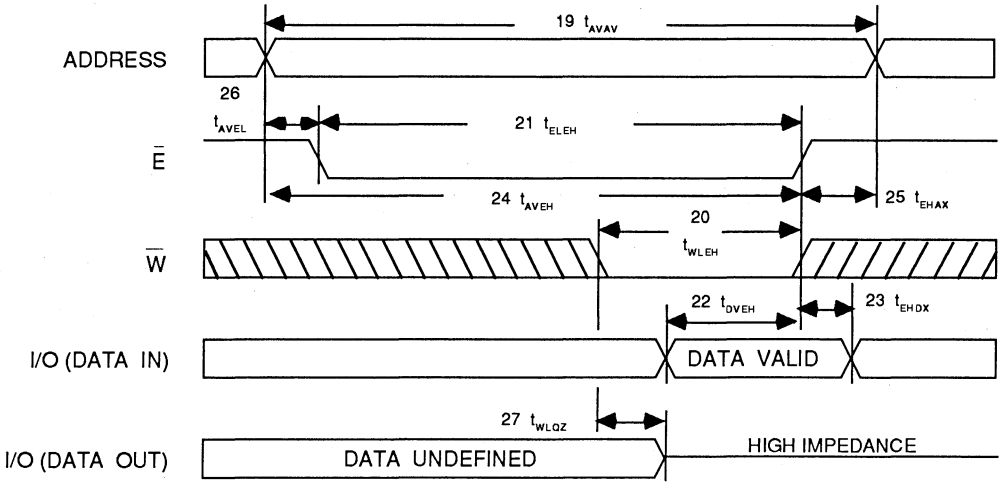
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL		PARAMETER	IMS 1620-25		IMS 1620-30		IMS 1620-35		IMS 1620-45		IMS 1620-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
19	tAVAV	tWC	Write Cycle Time	25		30		35		45		55		ns	
20	tWLEH	tWP	Write Pulse Width	20		20		30		30		40		ns	
21	tELEH	tCW	Chip Enable to End of Write	20		20		30		30		40		ns	
22	tDVEH	tDW	Data Setup to End of Write	13		15		15		20		25		ns	
23	tEHDX	tDH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVEH	tAW	Address Setup to End of Write	20		25		30		30		40		ns	
25	tEHAX	tWR	Address Setup to Start of Write	5		5		5		0		0		ns	
26	tAVEL	tAS	Address Hold after End of Write	0		0		0		0		0		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1620 has two control inputs, Chip Enable (/E) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1620 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1620. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

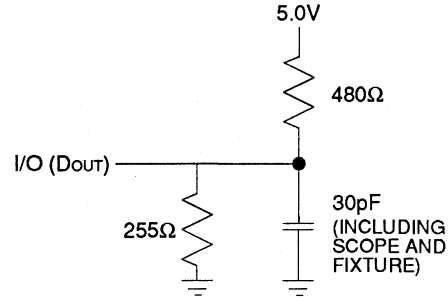
TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1620	25ns	PLASTIC DIP	IMS1620P-25
	25ns	CERAMIC DIP	IMS1620S-25
	25ns	CERAMIC LCC	IMS1620W-25
	25ns	PLASTIC SOJ	IMS1620E-25
	30ns	PLASTIC DIP	IMS1620P-30
	30ns	CERAMIC DIP	IMS1620S-30
	30ns	CERAMIC LCC	IMS1620W-30
	30ns	PLASTIC SOJ	IMS1620E-30
	35ns	PLASTIC DIP	IMS1620P-35
	35ns	CERAMIC DIP	IMS1620S-35
	35ns	CERAMIC LCC	IMS1620W-35
	35ns	PLASTIC SOJ	IMS1620E-35
	45ns	PLASTIC DIP	IMS1620P-45
	45ns	CERAMIC DIP	IMS1620S-45
	45ns	CERAMIC LCC	IMS1620W-45
	45ns	PLASTIC SOJ	IMS1620E-45
	55ns	PLASTIC DIP	IMS1620P-55
	55ns	CERAMIC DIP	IMS1620S-55
	55ns	CERAMIC LCC	IMS1620W-55
	55ns	PLASTIC SOJ	IMS1620E-55

IMS1624
CMOS
High Performance
16K x 4 Static RAM
with Output Enable

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- 16K x 4 Bit Organization with Output Enable
- 25, 30, 35, 45 and 55 nsec Address Access Times
- 25, 30, 35, 45 and 55 nsec Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 24-Pin, 300-mil DIP (JEDEC Std.)
- 28-Pin Ceramic LCC (JEDEC Std.)
- 24-Pin, 300-mil SOJ

DESCRIPTION

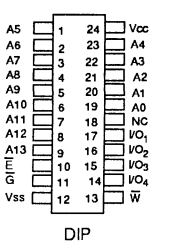
The INMOS IMS1624 is a high performance 16K x 4 CMOS Static RAM. The IMS1624 provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624 provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode. The IMS1624 also includes an Output Enable (/G) for fast access to data and enhanced bus contention control.

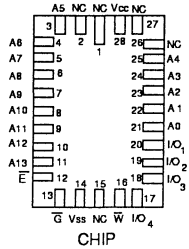
The IMS1624 is the functional equivalent of the IMS1620 with the addition of an Output Enable input.

The IMS1624M and IMS1624LM are MIL-STD-883 versions intended for military applications.

PIN CONFIGURATION

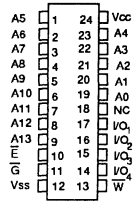


DIP



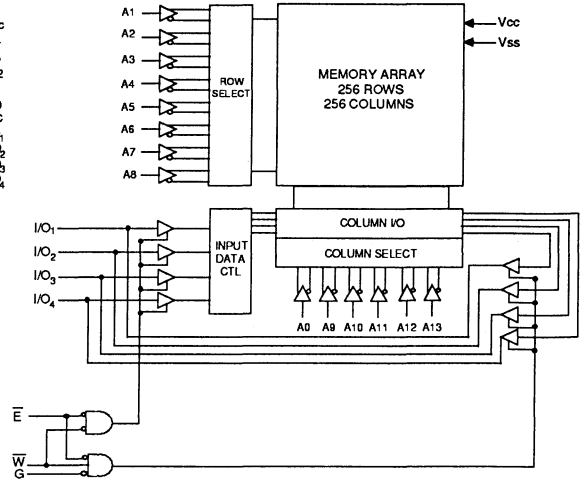
CHIP CARRIER

LOGIC SYMBOL



SOJ

BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13} ADDRESS INPUTS	I/O DATA IN/OUT
$\overline{W}$ WRITE ENABLE	Vcc POWER (+5V)
$\overline{E}$ CHIP ENABLE	Vss GROUND
$\overline{G}$ OUTPUT ENABLE	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to Vcc+0.5
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		110 100	mA mA	t_{AVAV} = 25ns and 30ns t_{AVAV} = 35, 45, and 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\bar{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\bar{E} \geq$ (Vcc - 0.2). All other inputs at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		17	mA	$\bar{E} \geq$ (Vcc - 0.2). Inputs cycling at $V_{IN} \leq 0.2$ or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

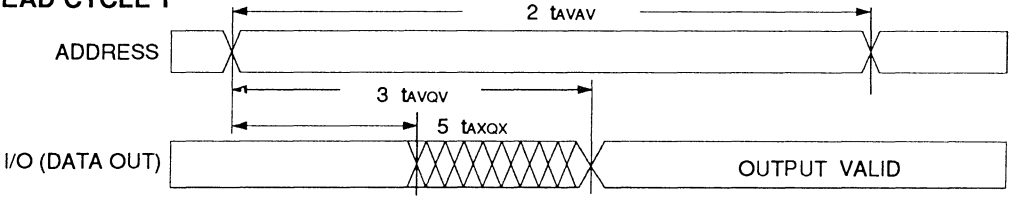
RECOMMENDED AC OPERATING CONDITIONS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

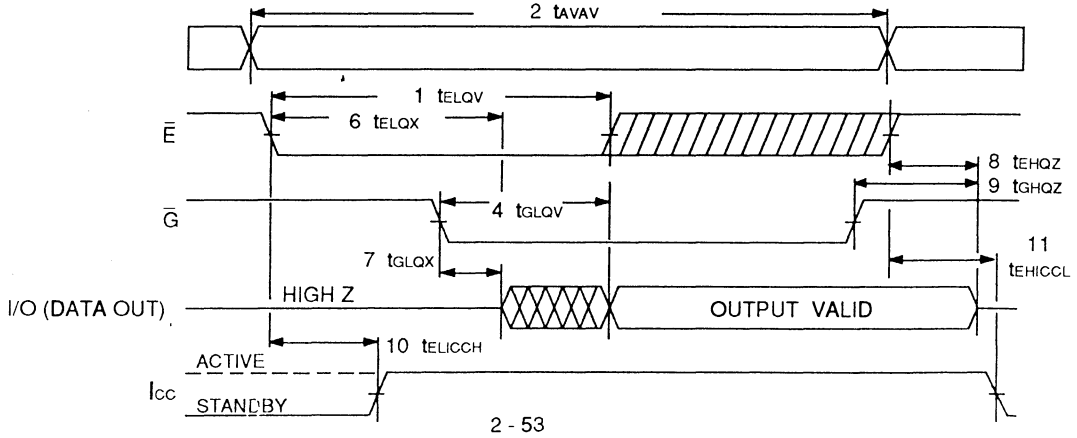
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
1	tELQV	tACS	Chip Enable Access Time		25		30		35		45		55	ns	
2	tAVAV	tRC	Read Cycle Time	25		30		35		45		55		ns	c
3	tAVQV	tAA	Address Access Time		25		30		35		45		55	ns	d
4	tGLQV	tTOE	O/P Enable Access Time		15		15		20		20		25	ns	
5	tAXQX	tOH	O/P Hold After Address Change	5		5		5		5		5		ns	j
6	tELQX	tLZ	O/P Enable to O/P Active	5		5		5		5		5		ns	j
7	tGLQX	tOLZ	O/P Enable to O/P Active	0		0		0		0		0		ns	j
8	tEHQZ	tHZ	Chip Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
9	tGHQZ	tOHZ	O/P Disable to Output Inactive	0	15	0	15	0	15	0	20	0	25	ns	f, j
10	tELICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
11	tEHICCL	tPD	Chip Disable to Power Down		25		30		35		45		55	ns	j
		tT	Input Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ and $\overline{G}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
12	tAVAV	t WC	Write Cycle Time	25		30		35		45		55		ns	
13	t WLWH	t WP	Write Pulse Width	20		20		30		30		40		ns	
14	t ELWH	t CW	Chip Enable to End of Write	20		20		30		30		40		ns	
15	t DVWH	t DW	Data Setup to End of Write	13		15		15		20		25		ns	
16	t WHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
17	t AVWH	t AW	Address Setup to End of Write	20		25		30		30		40		ns	
18	t AVWL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
19	t WHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
20	t WLQZ	t WZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,j
21	t WHQX	t OW	O/P Active after end of Write	0		0		0		0		0		ns	j

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g,h]

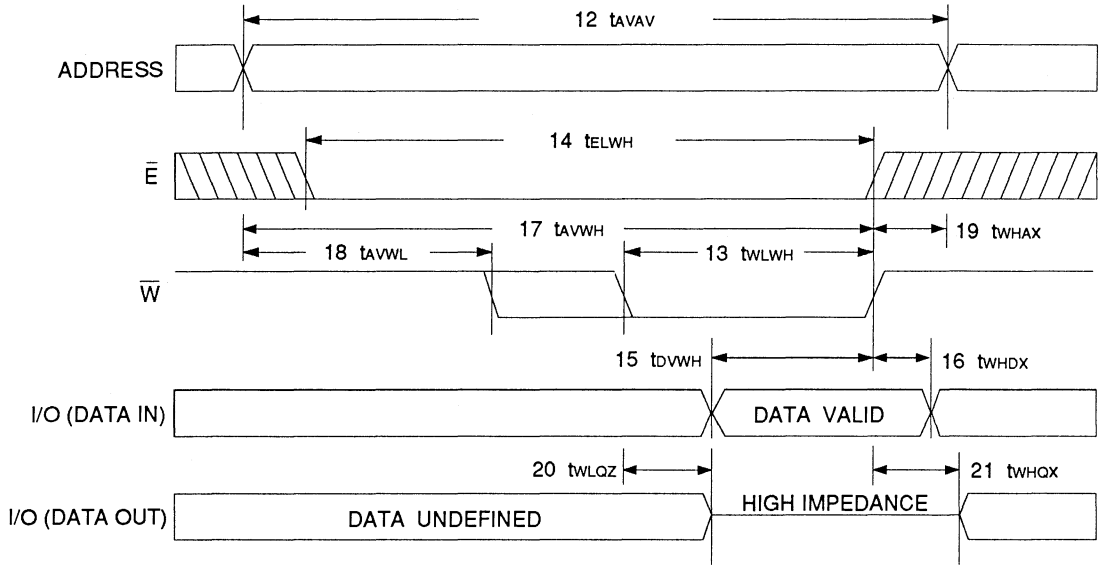
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
22	tAVAV	t WC	Write Cycle Time	25		30		35		45		55		ns	
23	t WLEH	t WP	Write Pulse Width	20		20		30		30		40		ns	
24	t ELEH	t CW	Chip Enable to End of Write	20		20		30		30		40		ns	
25	t DVEH	t DW	Data Setup to End of Write	13		15		15		20		25		ns	
26	t EHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
27	t AVEH	t AW	Address Setup to End of Write	20		25		30		30		40		ns	
28	t EHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
29	t AVEL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
30	t WLQZ	t WZ	Write Enable to Output Disable	0	15	0	15	0	15	0	20	0	25	ns	f,j

WRITE CYCLE 3: Fast Write, Outputs Disabled[g,h]

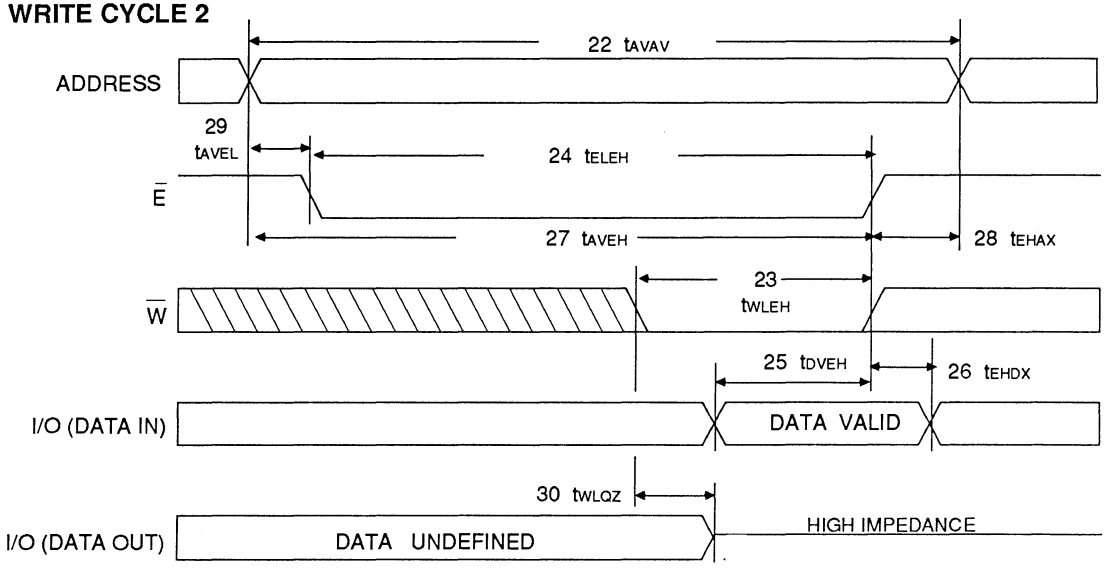
No	SYMBOL Standard	SYMBOL Alternate	PARAMETER	IMS 1624-25 MIN	IMS 1624-25 MAX	IMS 1624-30 MIN	IMS 1624-30 MAX	IMS 1624-35 MIN	IMS 1624-35 MAX	IMS 1624-45 MIN	IMS 1624-45 MAX	IMS 1624-55 MIN	IMS 1624-55 MAX	UNITS	NOTES
31	tAVAV	t WC	Write Cycle Time	18		20		20		25		30		ns	
32	t WLWH	t WP	Write Pulse Width	13		15		15		20		25		ns	
33	t DVWH	t DW	Data Setup to End of Write	18		20		20		25		30		ns	
34	t WHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
35	t AVWH	t AW	Address Setup to End of Write	12		15		15		20		25		ns	
36	t WHAX	t WR	Address Hold after End of Write	5		5		5		0		0		ns	
37	t AVWL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

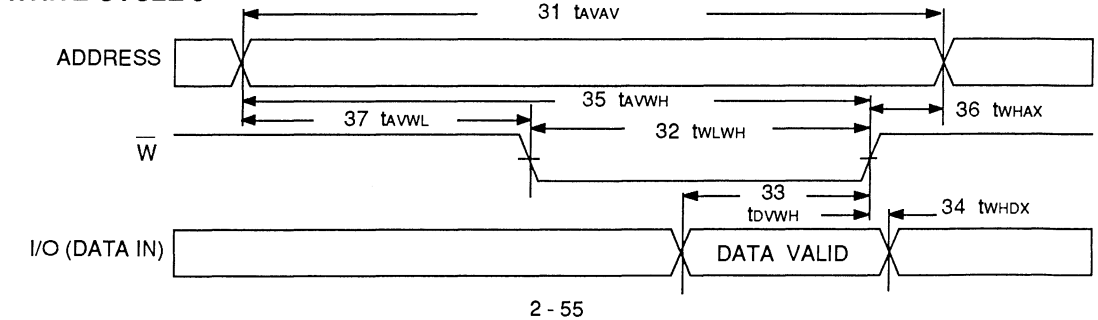
WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE 3



DEVICE OPERATION

The IMS1624 has three control inputs, Chip Enable (/E), Output Enable (/G) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W and /G inputs. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E and /G $\leq$ V_{IL} max. Read access time is measured from the latter of either /E or /G going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E and /G are low. The outputs remain active throughout READ CYCLE 1 and are valid at the specified address access time. The address inputs may change at access time and long as /E and /G remain low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated bythe latter of /E or /G going low. As long as address is stable when /E goes low, valid data is at the outputs at thelatter of specified Chip Enable Access or Output Enable Access times. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

Since /G controls the output buffers, /G is required to be low in order for the outputs to be active.

WRITE CYCLE

The write cycle of the IMS1624 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELQX} after the falling edge of /E if /G is already low (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLQZ}. To aviod bus contention, the /G input can be held high throughout the write operation.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active (if /G is low). The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

WRITE CYCLE 3 waveform shows a write cycle controlled by /W, with /G high and /E low throughout the cycle. As the outputs will not become active during this operation, maximum data bandwidth is provided by allowing very short write cycles and eliminating any bus contention considerations.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1624. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

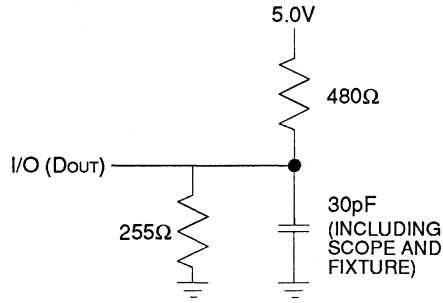
TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

FIGURE 1. OUTPUT LOAD



ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1624	25ns	PLASTIC DIP	IMS1624P-25
	25ns	CERAMIC DIP	IMS1624S-25
	25ns	CERAMIC LCC	IMS1624W-25
	25ns	PLASTIC SOJ	IMS1624E-25
	30ns	PLASTIC DIP	IMS1624P-30
	30ns	CERAMIC DIP	IMS1624S-30
	30ns	CERAMIC LCC	IMS1624W-30
	30ns	PLASTIC SOJ	IMS1624E-30
	35ns	PLASTIC DIP	IMS1624P-35
	35ns	CERAMIC DIP	IMS1624S-35
	35ns	CERAMIC LCC	IMS1624W-35
	35ns	PLASTIC SOJ	IMS1624E-35
	45ns	PLASTIC DIP	IMS1624P-45
	45ns	CERAMIC DIP	IMS1624S-45
	45ns	CERAMIC LCC	IMS1624W-45
	45ns	PLASTIC SOJ	IMS1624E-45
	55ns	PLASTIC DIP	IMS1624P-55
	55ns	CERAMIC DIP	IMS1624S-55
	55ns	CERAMIC LCC	IMS1624W-55
	55ns	PLASTIC SOJ	IMS1624E-55

IMS1630L
CMOS
High Performance
8K x 8 Static RAM

FEATURES

- INMOS' high performance CMOS
- Advanced Process - 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- 45, 55, 70, 100 and 120 ns Address Access Times
- 45, 55, 70, 100 and 120 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Standard 28 Pin 600-mil DIP, 28-Lead SOIC and Skinny DIP Package
- Battery Backup Operation - 2V Data Retention

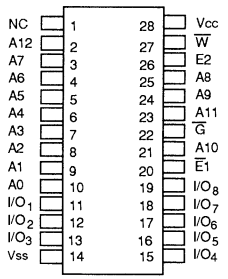
DESCRIPTION

The INMOS IMS1630L is a high performance 8Kx8 CMOS Static RAM.

The IMS1630L features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. The IMS1630L provides two Chip Enable functions ($\overline{E1}$, E2) to place the device into a reduced power standby mode.

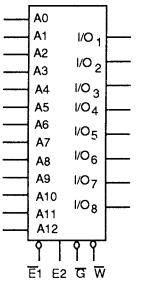
In the low power battery backup data retention mode, the IMS1630L consumes typically 10µA at 2 volts supply.

PIN CONFIGURATION

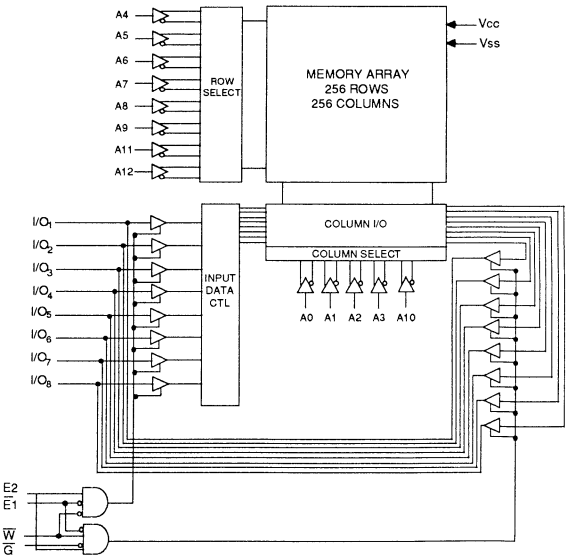


DIP and SOIC

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{12}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vcc	GROUND
I/O1-I/O8	DATA IN/OUT		
$\overline{E1}$, E2	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

IMS1630L

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (V_{CC}+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

*V_{IL} min = -3.0 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		90	mA	t_{AVAV} = t_{AVAV} (min)
I_{CC2}	V_{CC} Power Supply Current (Standby,Stable TTL Input Levels)		20	mA	$\overline{E}1 \geq V_{IH}$ or $E2 \leq V_{IL}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		8	mA	$\overline{E}1 \geq (V_{CC} - 0.2V)$ or $E2 \leq 0.2V$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\overline{E}1 \geq (V_{CC} - 0.2V)$ or $E2 \leq 0.2V$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC} = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC} = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

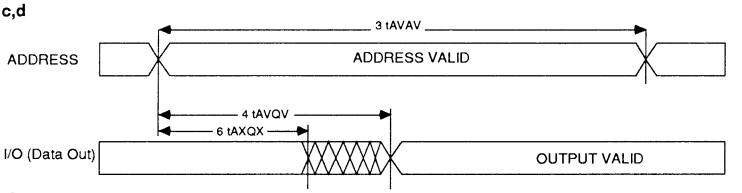
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

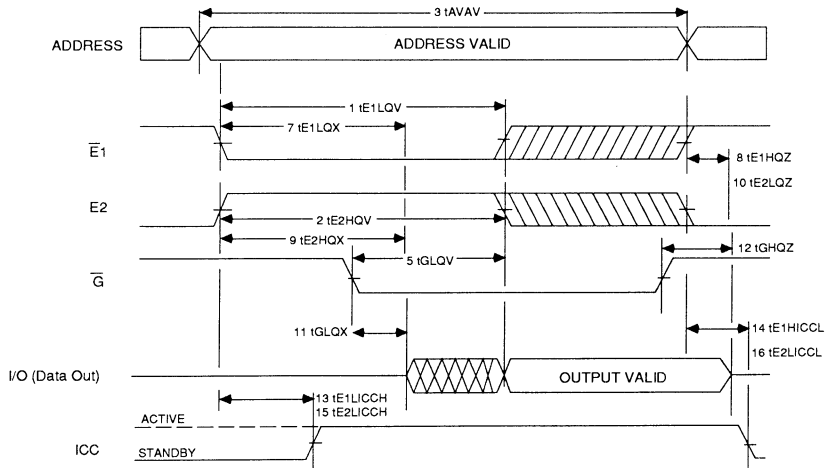
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
1	t E1LQV	t ACS	Chip Enable Access Time		45		55		70		100		120	ns	
2	t E2HQV	t ACS	Chip Enable Access Time		45		55		70		100		120	ns	
3	tAVAV	t RC	Read Cycle Time	45		55		70		100		120		ns	c
4	tAVQV	t AA	Address Access Time		45		55		70		100		120	ns	d
5	tGLQV	t OE	O/P Enable to Data Valid		20		20		35		40		50	ns	
6	tAXQX	t OH	O/P Hold After Addr's Ch'ge	5		5		10		10		10		ns	
7	t E1LQZ	t LZ	Chip Enable to O/P Active	5		5		10		10		10		ns	
8	tE1HQZ	t HZ	Chip Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
9	t E2HQZ	t LZ	Chip Enable to O/P Active	5		5		10		10		10		ns	
10	tE2LQZ	t HZ	Chip Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
11	t GLQX	t LZ	O/P Enable to O/P Active	5		5		5		5		5		ns	
12	t GHQZ	t HZ	O/P Disable to O/P Inactive	0	20	0	25	0	25	0	35	0	40	ns	f, j
13	t E1HICCH	t PU	Chip Enable to Power Up	0		0		0		0		0		ns	j
14	t E1LICCL	t PD	Chip Enable to Power Down		20		20		20		25		30	ns	j
15	t E2HICCH	tPU	Chip Enable to Power Up	0		0		0		0		0		ns	j
16	t E2LICCL	tPD	Chip Disable to Power Down		20		20		20		25		30	ns	j
17		tT	I/P Rise and Fall Times		50		50		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}1$ low, $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

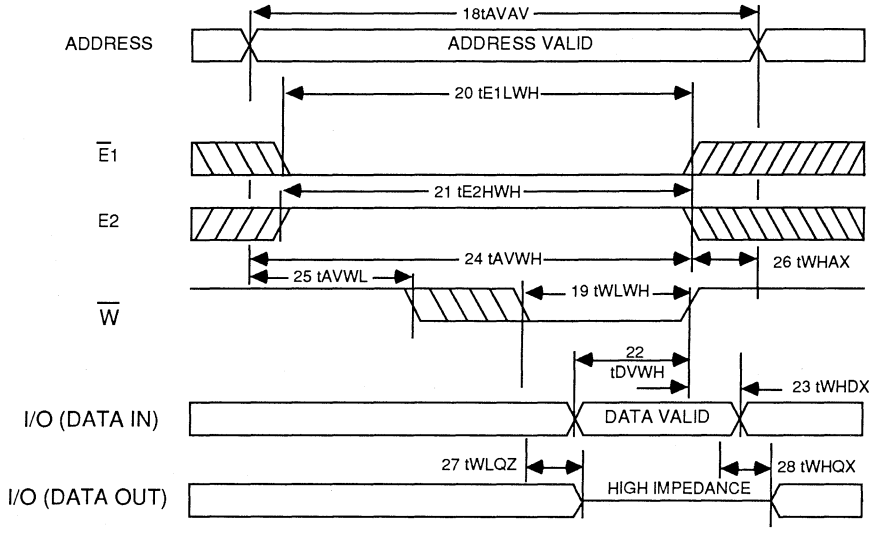
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
18	tAVAV	t WC	Write Cycle Time	45		55		70		100		120		ns	
19	tWLWH	t WP	Write Pulse Width	35		40		40		60		70		ns	
20	tE1LWH	t CW	Chip Enable 1 to End of Write	35		40		40		60		70		ns	
21	tE2HWH	t CW	Chip Enable 2 to End of Write	35		40		40		60		70		ns	
22	tDVWH	t DW	Data Setup to End of Write	20		20		20		40		40		ns	
23	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
24	tAVWH	t AW	Address Setup to End of Write	35		40		40		80		85		ns	
25	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
26	tWHAX	t WR	Address Hold after End of Write	0		0		0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	20	0	20	0	20	0	35	0	40	ns	f,j
28	tWHQX	t OW	Output Active After End of Write	5		5		5		5		5		ns	i,j

WRITE CYCLE 2: $\overline{E}1$ OR E2 CONTROLLED[g,h]

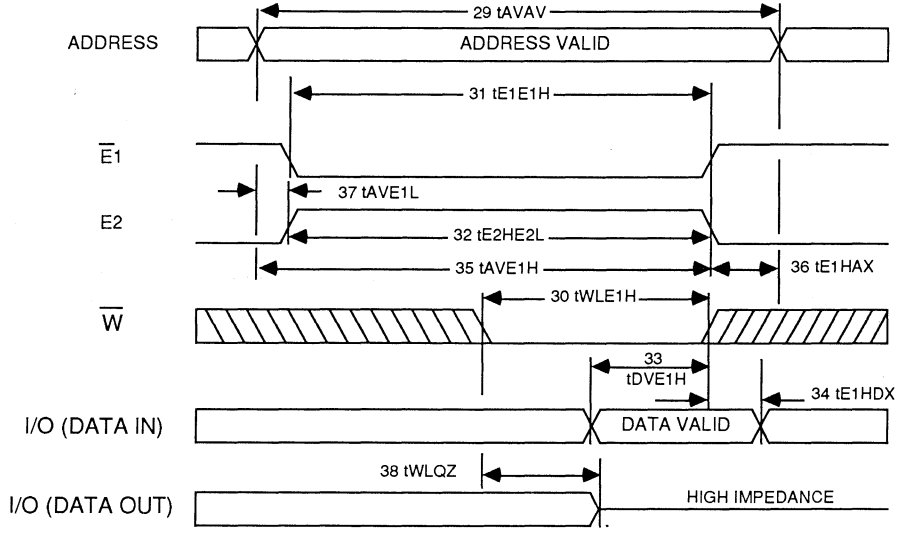
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630L-45 MIN	IMS 1630L-45 MAX	IMS 1630L-55 MIN	IMS 1630L-55 MAX	IMS 1630L-70 MIN	IMS 1630L-70 MAX	IMS 1630L-100 MIN	IMS 1630L-100 MAX	IMS 1630L-120 MIN	IMS 1630L-120 MAX	UNITS	NOTES
29	tAVAV	t WC	Write Cycle Time	45		55		70		100		120		ns	
30	tWLE1H	t WP	Write Pulse Width	35		40		40		60		70		ns	
31	tE1LE1H	t CW	Chip Enable 1 to End of Write	35		40		40		60		70		ns	
32	tE2HE2L	t CW	Chip Enable 2 to End of Write	35		40		40		60		70		ns	
33	tDVE1H	t DW	Data Setup to End of Write	20		20		20		40		40		ns	
34	tE1HDX	t DH	Data Hold after End of Write	0		0		0		0		0		ns	
35	tAVE1H	t AW	Address Setup to End of Write	35		40		40		80		85		ns	
36	tE1HAX	t WR	Address Hold after End of Write	0		0		0		0		0		ns	
37	tAVE1L	t AS	Address Setup to Start of Write	0		0		0		0		0		ns	
38	tWLQZ	t WZ	Write Enable to Output Disable	0	20	0	20	0	20	0	30	0	35	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}1$, or $\overline{W}$ must be $\geq V_{IH}$ or E2 must be $\leq V_{IL}$ during address transitions.
Note i: If $\overline{W}$ is low when the later of $\overline{E}1$ goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



WRITE CYCLE 2



DEVICE OPERATION

The IMS1630L has four control inputs, Chip Enable1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$) and Output Enable ($\overline{G}$). There are also13 address inputs (A0 -A12) and eight Data I/O lines (I/O 1 to I/O 8). The Enable inputs control device selection as well as active and standby modes. The $\overline{W}$ input controls the mode of operation (Read or Write). The $\overline{G}$ input controls only the state of the eight output drivers.

With both $\overline{E1}$ low and E2 high, the device is selected and the 13 address inputs are decoded to select one 8-bit word out of 8K words. Read and Write operations on the memory cells are controlled by the $\overline{W}$ input. With either $\overline{E1}$ high or E2 low, the device is deselected, the outputs disabled and the power consumption is reduced to less than one-fourth of the active mode power. $\overline{G}$ serves only to control the operation of the output drivers. When $\overline{G}$ is high, the output drivers are in a high impedance state, independant of the $\overline{E1}$, E2 and $\overline{W}$ inputs.

READ CYCLE

A read cycle is defined as $W \geq V_{IH}$ min with $\overline{E1} \leq V_{IL}$ max, $E2 \geq V_{IH}$ min and $\overline{G} \leq V_{IL}$ max. Read access time is measured from the later of either $\overline{E1}$ going low, E2 going high, valid address, or $\overline{G}$ going low.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E1}$ is low and E2 is high (with $\overline{G}$ low). The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of tAXQX. As long as $\overline{E1}$ remains low and E2 is high, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by the later of $\overline{E1}$ going low, E2 going high or $\overline{G}$ going low. As long as address is stable when the later of $\overline{E1}$ goes low or E2 goes high, valid data is at the output at the later of tE1LQV, tE2HQV or tGLQV. If address is not valid when the later of $\overline{E1}$ goes low or E2 goes high, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

The $\overline{G}$ signal controls the output buffer. $\overline{G}$ is required to be low (along with $\overline{E1}$ low and E2 high) in order for I/O1 - I/O 8 to be active.

WRITE CYCLE

The write cycle of the IMS1630L is initiated by the later of $\overline{E1}$ or $\overline{W}$ to transition from a high to a low or E2 transitioning from low to high. The $\overline{G}$ control will remove bus contention if held high throughout the duration of the write cycle. If $\overline{G}$ is low during a $\overline{W}$ controlled write cycle (Write Cycle 1), the output buffer will be turned on by the later of tE1LQX after the falling edge of $\overline{E1}$ or tE2HQX after the rising edge of E2. The output buffer is then turned off within tWLQZ of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore the recommended mode of operation is to keep $\overline{G}$ high during the write cycle. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

For any write cycle, tAVWL, tAVE1L, or tAVE2H must be met, depending on whether $\overline{E1}$, E2 or $\overline{W}$ is the last to transition. After either $\overline{W}$ or $\overline{E1}$ goes high or E2 goes low to terminate the write cycle, addresses may change. If address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways. The fidelity of the $\overline{W}$ control signal is very important. Excessive ringing on high to low transitions may cause signals to rise above V_{IL} max, violating the minimum $\overline{W}$ pulse width specification - tWLWH.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E1}$ is low and E2 is high, the outputs remain in a high impedance state (unless $\overline{G}$ is low). If $\overline{G}$ is low when $\overline{W}$ goes high at the end of a write cycle the data read from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by the later $\overline{E1}$ going high or E2 going low. Data set-up and hold times are referenced to the later of the rising edge of $\overline{E1}$ or the falling edge of E2. With either $\overline{E1}$ high or E2 low the outputs remain in the high impedance state.

When using WRITE CYCLE 1 proper management of the $\overline{G}$ control signal will avoid bus contention. If $\overline{G}$ is low when $\overline{W}$ goes high (with $\overline{E1}$ low and E2 high) the output buffers will be active tWHQX after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If input data from the previous cycle is still valid after the address changes, contention may result. Contention may also result if the device is selected ($\overline{E1}$ low, E2 high, $\overline{G}$ low) before $\overline{W}$ goes low and input data is valid early in the cycle. The recommended mode of operation is to keep $\overline{G}$ high except when reading data from the device, thus avoiding bus contention.

TTL VS. CMOS INPUTLEVELS

The INMOS 1630L is fully compatible with TTL input levels. The input circuitry of the IMS1630L is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1630L consumes less power when CMOS levels are used instead of TTL levels. The lower CMOS Icc specifications (Icc3 and Icc4) may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1630L. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 µF and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilising a wideband oscilloscope and probe.

DATA RETENTION (L version only) ($0°C \le T_A \le 70°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (Vcc -0.2V)$ $\overline{E} \ge (Vcc -0.2V)$
I_{CCDR1}	Data Retention Current		15	350	µA	V_{CC} = 3.0 volts
I_{CCDR2}	Data Retention Current		10	200	µA	V_{CC} = 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Typical data retention parameters at 25 °C

Note j: Parameter guaranteed but not tested

Note k: Supply recovery rate should not exceed 100mV per10µs from V_{DR} to V_{CC} min

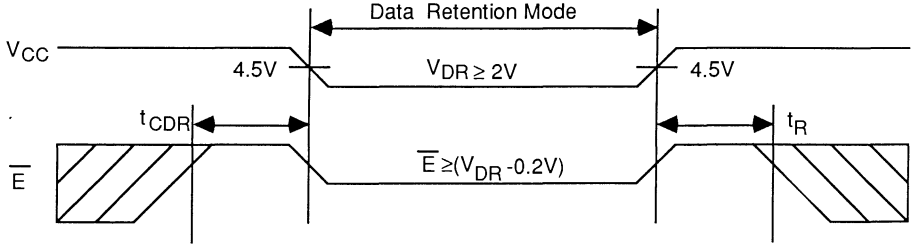
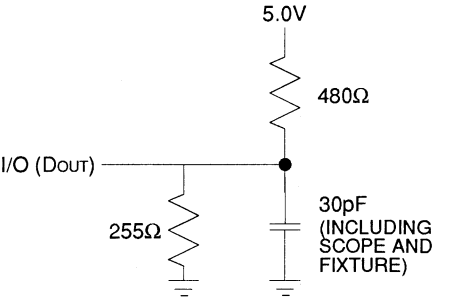


FIGURE 1. OUTPUT LOAD



$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	I/O	MODE
H	X	X	X	HI-Z	Standby (Isb)
X	L	X	X	HI-Z	Standby (Isb)
L	H	H	H	HI-Z	Output disable
L	H	H	L	DOUT	Read
L	H	L	X	DIN	Write

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1630	45ns	PDIP	IMS1630LP45
	45ns	SOIC	IMS1630LH45
	45ns	Skinny DIP	IMS1630LP45Z
	55ns	PDIP	IMS1630LP55
	55ns	SOIC	IMS1630LH55
	55ns	Skinny DIP	IMS1630LP55Z
	70ns	PDIP	IMS1630LP70
	70ns	SOIC	IMS1630LH70
	70ns	Skinny DIP	IMS1630LP70Z
	100ns	PDIP	IMS1630LP10
	100ns	SOIC	IMS1630LH10
	100ns	Skinny DIP	IMS1630LP10Z
	120ns	PDIP	IMS1630LP12
	120ns	SOIC	IMS1630LH12
	120ns	Skinny DIP	IMS1630LP12Z

IMS 1605:	**64K x 1**
IMS 1625:	**16K x 4**
IMS 1629:	**16K x 4 with Output Enable**
IMS 1626/7:	**16K x 4 with Separate I/Os**
IMS 1635:	**8K x 8**
IMS 1695:	**8K x 9**

IMS16X5 series High Performance Memory Products

Advance Information

FEATURES

- INMOS' Very High Speed Double Metal CMOS
- Advanced Process-1.2 Micron Design Rules
- 64K Bit Devices
- 15, 20 and 25 ns Address Access Times
- 15, 20 and 25 ns Chip Enable Access Times
- Fully TTL Compatible
- Single +5V ± 10% Operation
- Battery Backup Operation - 2V Data Retention, 10µA typical at 25°C
- Packages include: DIP, LCC and SOJ
- Military Versions Available

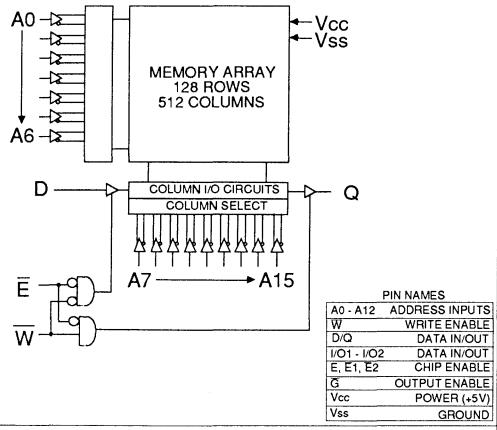
DESCRIPTION

The INMOS IMS16X5 series are high speed advanced 64K double layer metal CMOS Static RAMs.

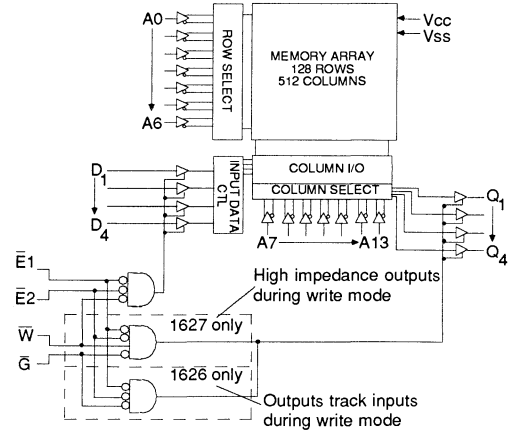
The range features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. A chip enable function ($\overline{E}$) that can be used to place the device into a low-power standby mode is available on all organisations. The 8K x 8 organisations provide an additional Chip Enable for reduced low-power standby mode. Output Enable ($\overline{G}$) is an enhancement on organisations requiring fast access to data and enhanced bus contention control.

Military versions of the 16X5 are also available.

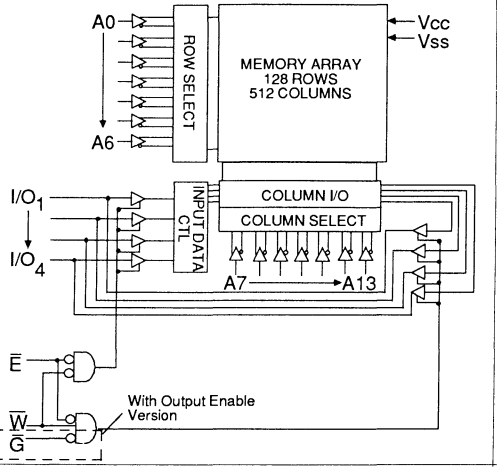
64K x 1



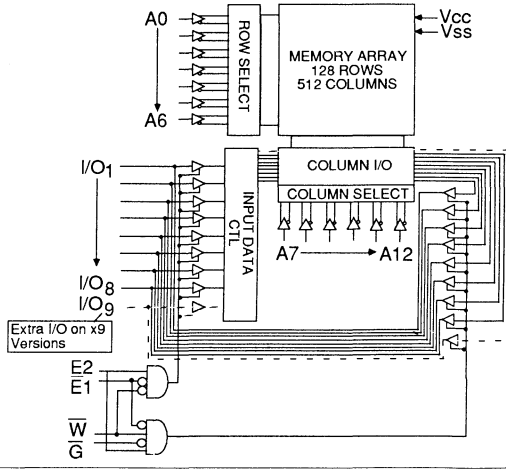
16K x 4 (Separate Inputs and Outputs)



16K x 4 (Without and with Output Enable)



8K x 8 / 8K x 9



2.1 Electrical specifications

2.1.1 Absolute maximum ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{SS}	Value on relative pin	−2.0	7.0	V
	Voltage on I/O	−1.0	V_{CC} +0.5	V
T_A	Temperature under bias	−55	125	°C
	Storage temperature	−65	150	°C
	Power dissipation		1	W
	DC output current		25	mA

(One output at a time, one second duration).

2.1.2 DC operating conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic '1' Voltage	2.0		V_{CC} + 0.5	V	All inputs
V_{IL}	Input Logic '0' Voltage	–0.5*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

*V_{IL}min. = −3.0V for pulse width <10ns, note b

2.1.3 DC electrical characteristics ($0°C \leq T_A \leq 70°C$)($V_{CC} = 5.0V \pm 10\%$)[a]

For suffixes refer to section 2.1.7.

Symbol	Parameter	Min	Max	Units	Notes
I_{CC1}	Average V_{CC} Power Supply Current		100	mA	$t_{AVAV} = t_{AVAV}$(min).
I_{CC2}	V_{CC} Power Supply Current (Standby, Stable TTL Input Levels)		40	mA	$\overline{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$.
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		2	mA	$\overline{E}_1 \geq (V_{CC} - 0.2V)$ or $E_2 \leq 0.2V$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V$.
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		25	mA	$\overline{E}_1 \geq (V_{CC} - 0.2V)$ or $E_2 \leq 0.2V$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V$.
I_{ILK}	Input Leakage Current (any input)		±1	μA	V_{CC} = max. $V_{IN} = V_{SS}$ to V_{CC}.
I_{OLK}	Off State Output Leakage Current		±5	μA	V_{CC} = max. $V_{IN} = V_{SS}$ to V_{CC}.
V_{OH}	Output Logic '1' Voltage	2.4		V	$I_{OH} = -4mA$.
V_{OL}	Output Logic '0' Voltage		0.4	V	$I_{OL} = 8mA$.

[1]Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.1.4 AC test condition

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	5ns
Input and output timing reference levels	1.5V
Output load	see figure 2.1

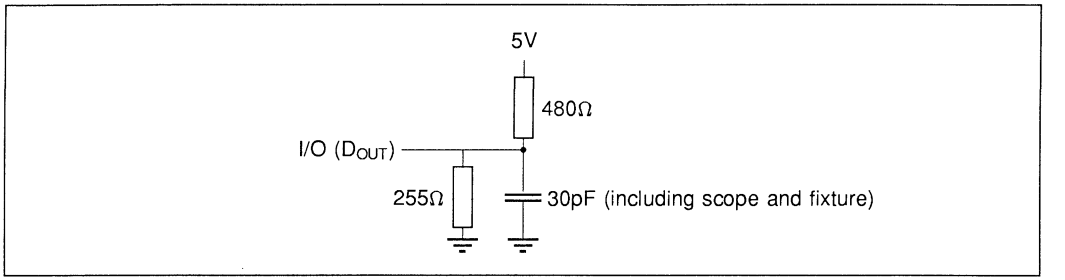


Figure 2.1 Output load

2.1.5 Capacitance[b]

Symbol	Parameter	Min	Max	Units	Conditions
C_{IN}	Input capacitance		5	pF	ΔV = 0 to 3.0V
C_{OUT}	Output capacitance		7	pF	ΔV = 0 to 3.0V

2.1.6 Recommended AC operating conditions ($0°C \leq T_A \leq 70°C$)($V_{CC} = 5.0V \pm 10\%$)

Read cycle[g]

No.	Symbol		Parameter	16X5-15		16X5-20		16X5-25		Units	Notes*
	Stand.	Alt.		min	max	min	max	min	max		
1	t_{E1LQV}	t_{ACS}	Chip Enable Access Time		15		20		25	ns	
2	t_{E2HQV}	t_{ACS}	Chip Enable Access Time		15		20		25	ns	
3	t_{AVAV}	t_{RC}	Read Cycle Time	15		20		25		ns	c
4	t_{AVQV}	t_{AA}	Address Access Time		15		20		25	ns	d
5	t_{GLQV}	t_{OE}	O/P Enable to Data Valid		8		10		10	ns	
6	t_{AXQX}	t_{OH}	O/P Hold After Add's Ch'ge	3		3		3		ns	
7	t_{E1LQX}[1]	t_{LZ}	Chip Enable to O/P Active	8		8		10		ns	
8	t_{E1HQZ}	t_{HZ}	Chip Disable to O/P inactive		8		10		10	ns	f,j
9	t_{E2HQZ}	t_{LZ}	Chip Enable to O/P Active	8		10		10		ns	
10	t_{E2LQZ}	t_{HZ}	Chip Disable to O/P Inactive		8		10		10	ns	f,j
11	t_{GLQX}	t_{LZ}	O/P Enable to O/P Active	3		3		3		ns	
12	t_{GHQZ}	t_{HZ}	O/P Disable to O/P Inactive		8		10		10	ns	f,j
13	$t_{E1LICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
14	$t_{E1LICCL}$	t_{PD}	Chip Disable to Power Down		15		20		25	ns	j
15	$t_{E2HICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
16	$t_{E2LICCL}$	t_{PD}	Chip Disable to Power down		15		20		25	ns	j
17		t_T	I/P Rise and Fall Times		50		50		50	ns	e,j

* Refer to section 2.1.7.
[1] T_{ELQX} is always greater than T_{EHQZ}

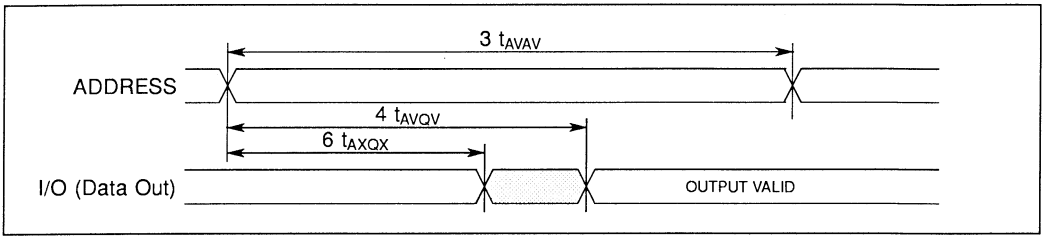


Figure 2.2 Read cycle 1[c,d]

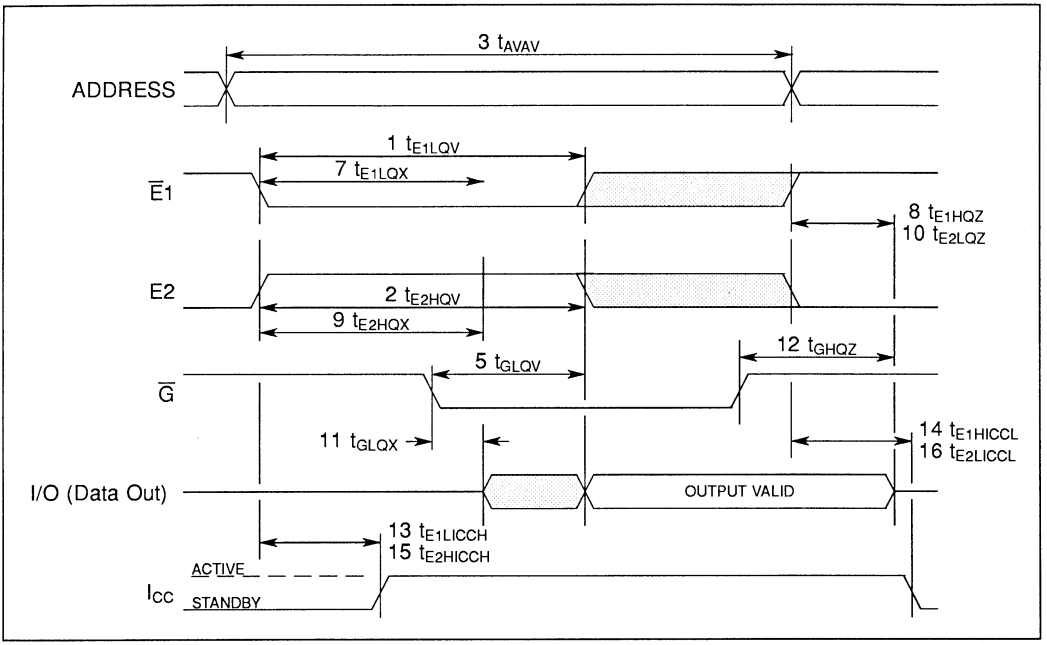


Figure 2.3 Read cycle 2[c]

Write cycle 1: $\overline{W}$ controlled[g,h]

No.	Symbol		Parameter	16X5-15		16X5-20		16X5-25		Units	Notes*
	Stand.	Alt.		min	max	min	max	min	max		
18	t_{AVAV}	t_{WC}	Write Cycle Time	15		20		25		ns	
19	t_{WLWH}	t_{WP}	Write Pulse Width	12		15		20		ns	
20	t_{E1LWH}	t_{CW}	Chip Enable 1 to End of Write	12		15		20		ns	
21	t_{E2HWH}	t_{CW}	Chip Enable 2 to End of Write	12		15		20		ns	
22	t_{DVWH}	t_{DW}	Data Setup to End of Write	10		12		15		ns	
23	t_{WHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
24	t_{AVWH}	t_{AW}	Address Setup to End of Write	15		15		20		ns	
25	t_{AVWL}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
26	t_{WHAX}	t_{WR}	Add's Hold After End of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	8	0	10	0	10	ns	f,j
28	t_{WHQX}	t_{OW}	Output Active after End of Write	0		0		0		ns	i,j

Write cycle 2: $\overline{E}1$ or E2 controlled[g,h]

No.	Symbol		Parameter	16X5-15		16X5-20		16X5-25		Units	Notes*
	Stand.	Alt.		min	max	min	max	min	max		
29	t_{AVAV}	t_{WC}	Write Cycle Time	15		20		25		ns	
30	t_{WLWE1H}	t_{WP}	Write Pulse Width	12		15		20		ns	
31	t_{E1LE1H}	t_{CW}	Chip Enable 1 to End of Write	12		15		20		ns	
32	t_{E2HE2L}	t_{CW}	Chip Enable 2 to End of Write	12		15		20		ns	
33	t_{DVE1H}	t_{DW}	Data Setup to End of Write	10		12		15		ns	
34	t_{E1HDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
35	t_{AVE1H}	t_{AW}	Address Setup to End of Write	15		15		20		ns	
36	t_{E1HAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns	
37	t_{AVE1L}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
38	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	8	0	10	0	10	ns	f,j

* Refer to section 2.1.7.

2.1.7 Notes

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.
Note b: This parameter is sampled and not 100% tested.
Note c: For Read Cycle 1 and 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continually selected, $\overline{E}1$ low $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max. and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}1$ or $\overline{W}$ must be $\geq V_{IH}$ or E2 must be $\leq V_{IL}$ during address transitions.
Note I: If $\overline{W}$ is low when the later of $\overline{E}1$ goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per 10μs from V_{DR} to V_{CC} min.

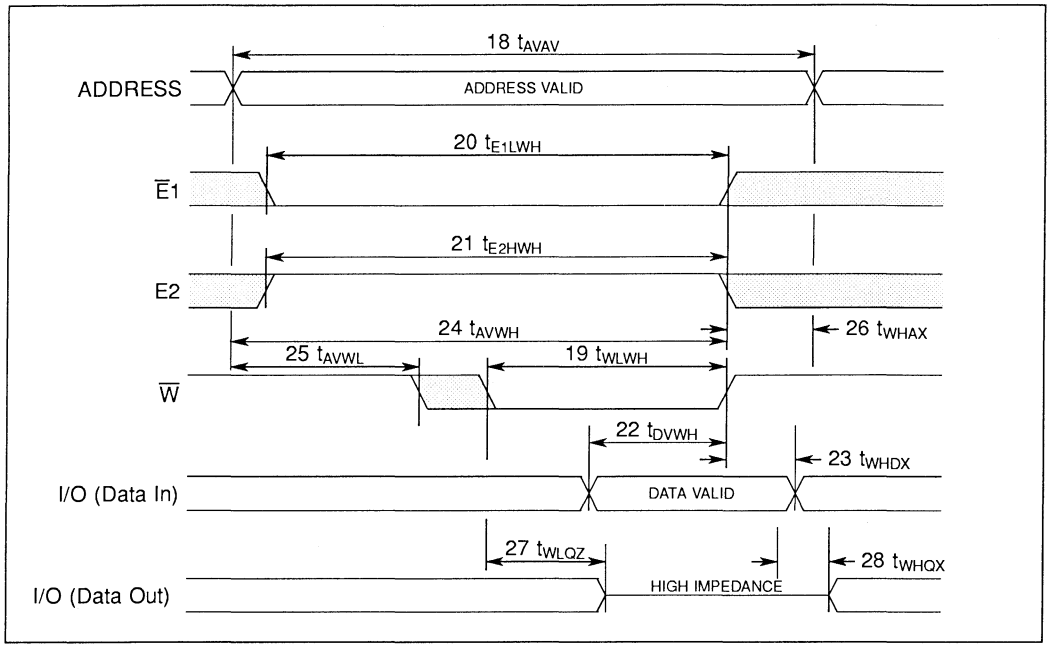


Figure 2.4 WRITE CYCLE 1

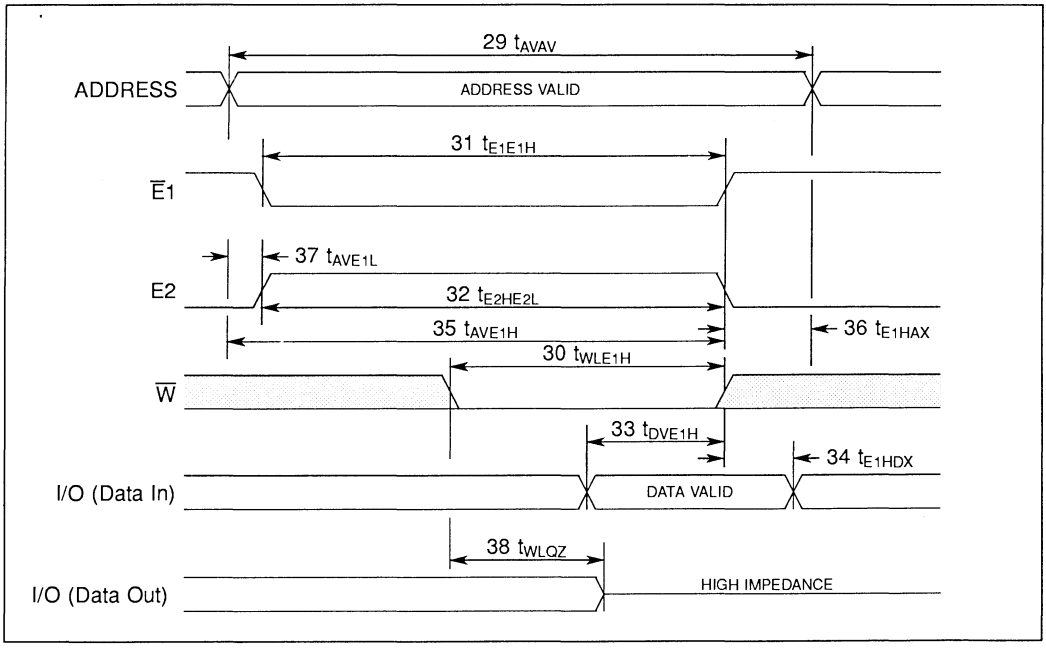


Figure 2.5 WRITE CYCLE 2

2.1.8 Power distribution

Recommended power distribution schemes combine proper power trace layout and placement of decoupling capacitors to maintain the wide operating margins of the IMS 16X5 series. The impedance in the decoupling path from the V_{CC} power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance/reactance of the decoupling capacitor.

Current transients associated with the operation of high speed memories have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as near the memory as possible, with the shortest lead lengths practical. The high frequency decoupling capacitor should have a minimum value of 0.1μF and be placed between the rows of memory devices in the array. A larger tantalum capacitor for low frquency current transients should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

2.1.9 Termination

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the line, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended series termination technique uses no DC current and a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The termination resistor should be placed as close to the driver package as possible. The line should be kept short by placing the driver–termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimise reflections, but generally a series resistor in the 10 to 33Ω range will be required. Because the characteristic impedance of each layout will be different, it is necessary to select the proper value of this resistor by trial and error. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilizing a wideband oscilloscope and probe.

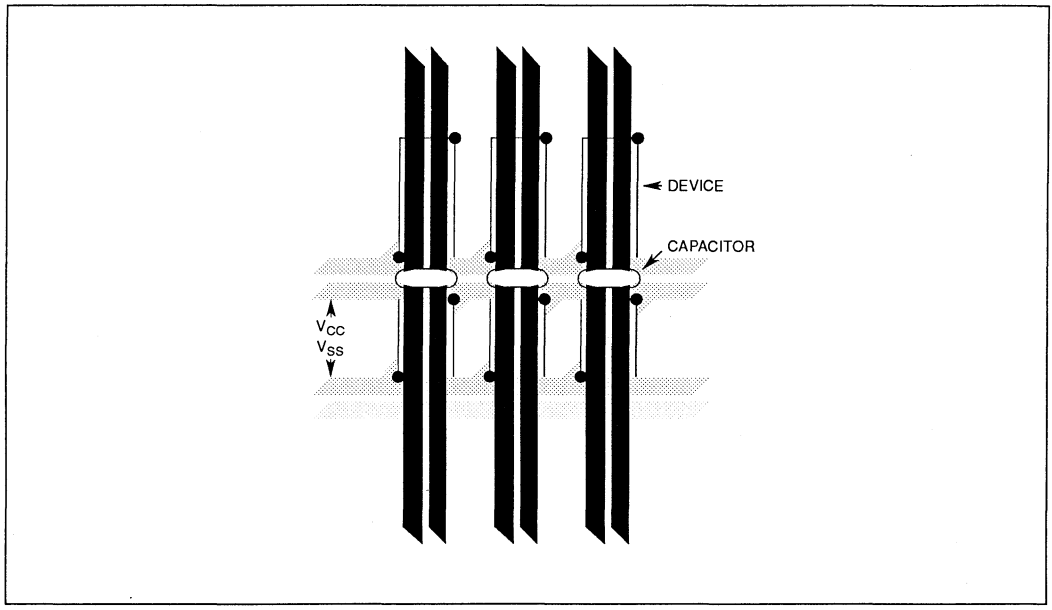


Figure 2.6 Grid showing decoupling capacitors

2.1.10 Data retention (low power versions only)($0°C \leq T_A \leq 70°C$)

Symbol	Parameter	Min	Typ(25°C)	Max	Units	Notes*
V_{DR}	Data Retention Voltage	2.0			V	$V_{IN} \leq 0.2V$ or $\geq (V_{CC}-0.2V)\overline{E} \geq (V_{CC} - 0.2V)$
I_{CCDR1}	Data Retention Current		15	100	μA	$V_{CC} = 3.0V$
I_{CCDR2}	Data Retention Current		10	70	μA	$V_{CC} = 2.0V$
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Refer to section 2.1.7.

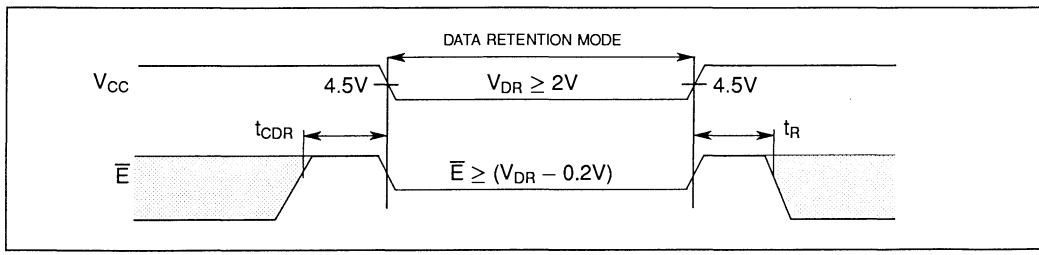


Figure 2.7 Data retention

2.2 Packaging information

2.2.1 Pin-outs and packages

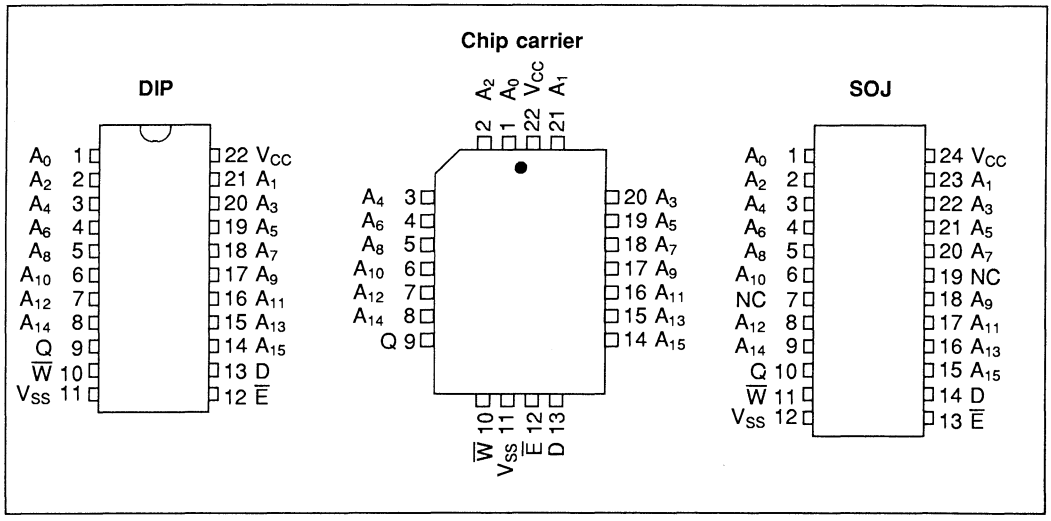


Figure 2.8 64K x 1 pin configuration

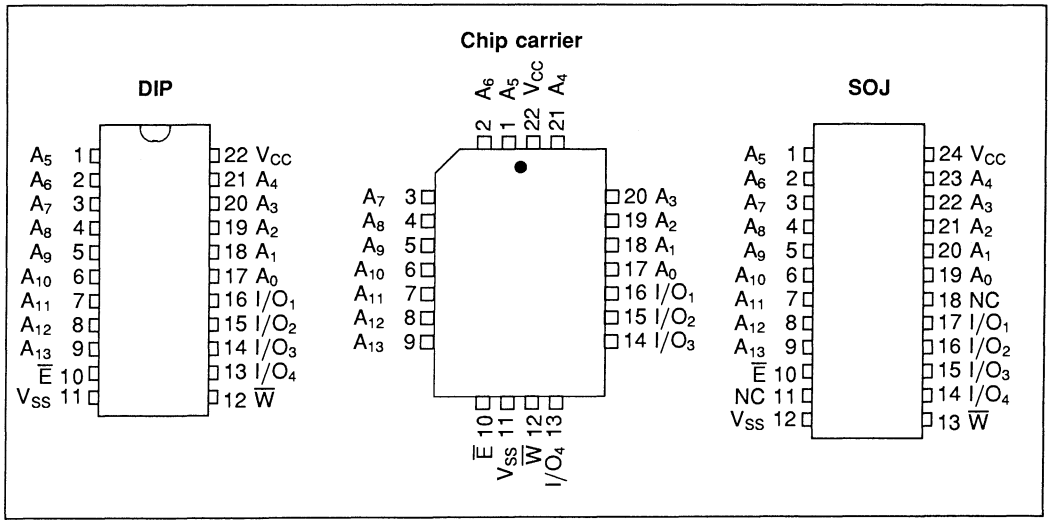


Figure 2.9 16K x 4 pin configuration

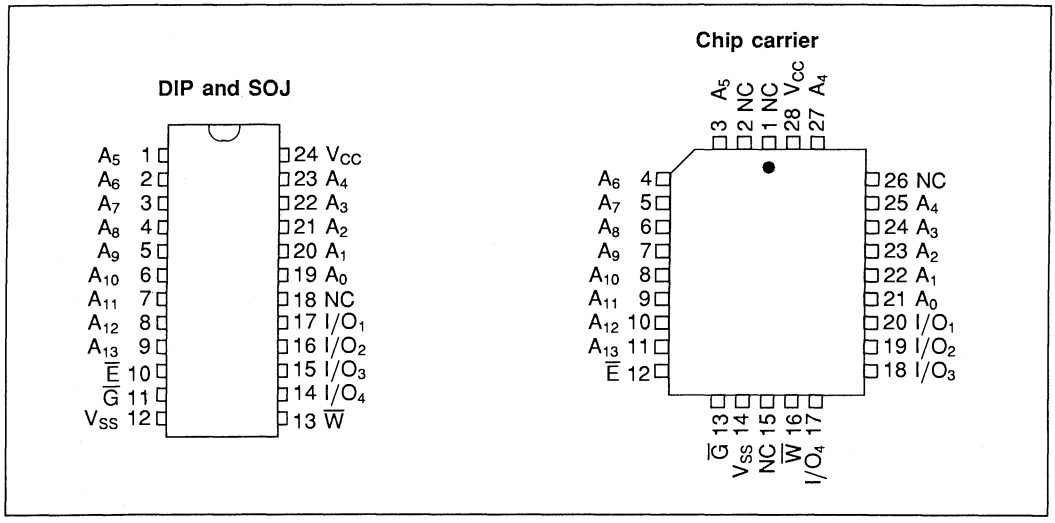


Figure 2.10 16K x 4 (with output enable) pin configuration

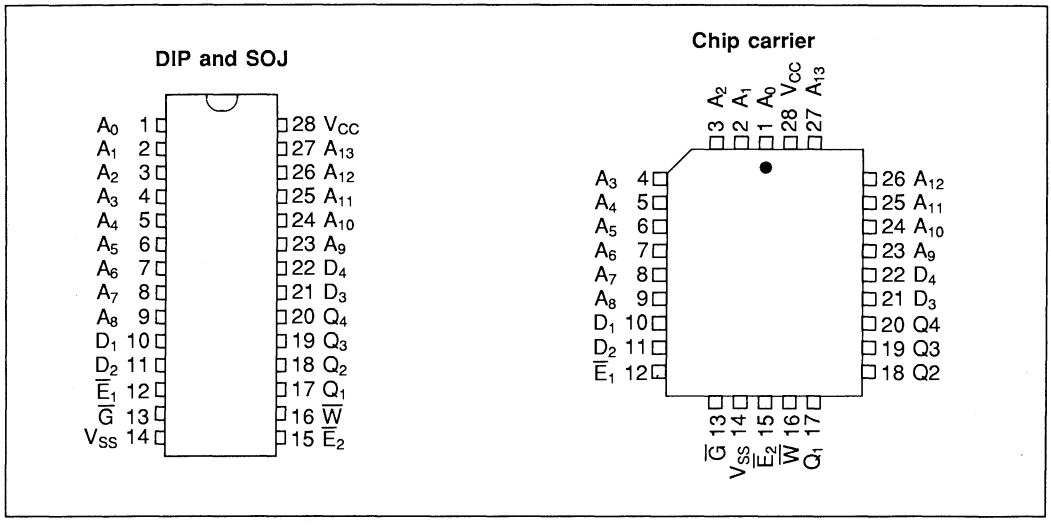


Figure 2.11 16K x 4 (with separate Inputs and Outputs) pin configuration

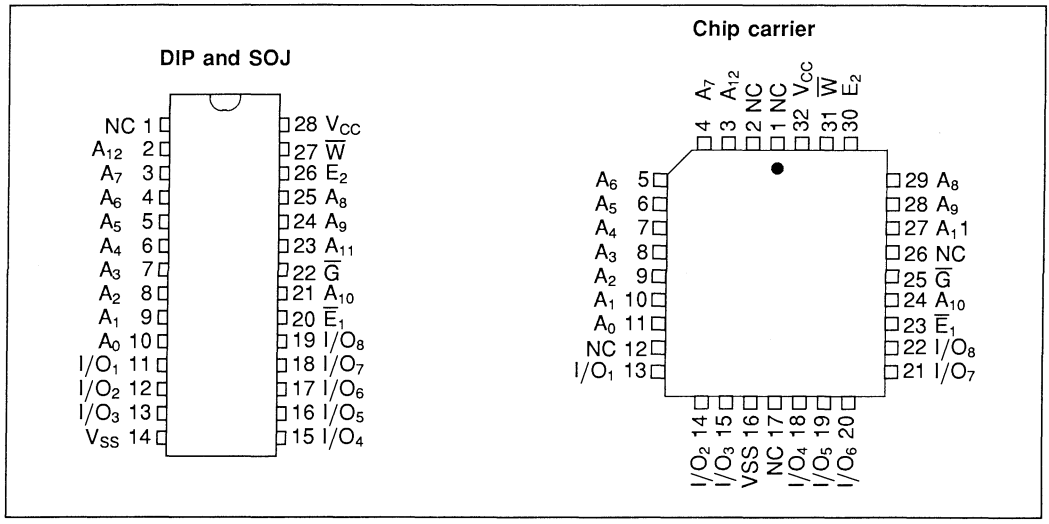


Figure 2.12 8K x 8 pin configuration

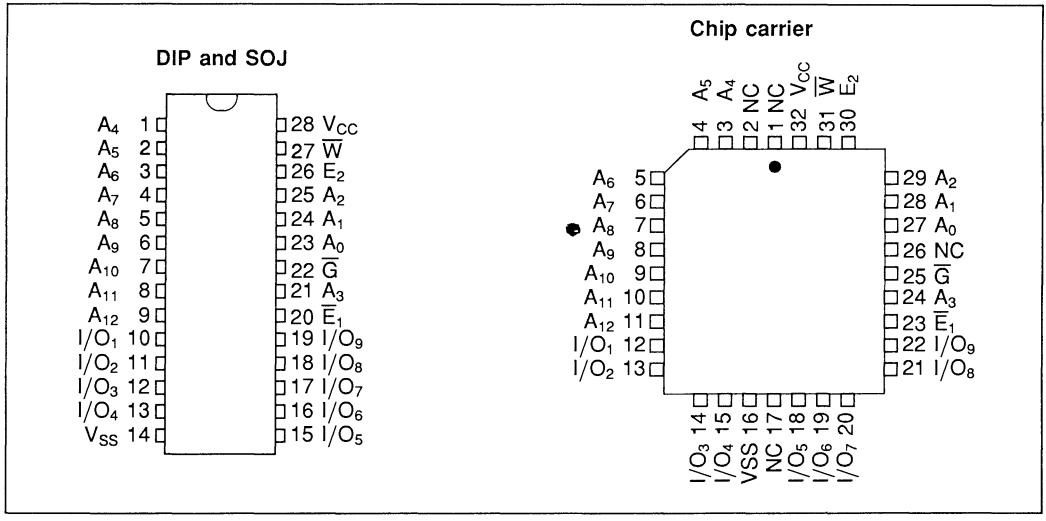


Figure 2.13 8K x 9 pin configuration

2.3 Ordering information

Device	Speed	Part Number
IMS1605	15ns	IMS1605x–15
	20ns	IMS1605x–20
	25ns	IMS1605x–25
IMS1625	15ns	IMS1625x–15
	20ns	IMS1625x–20
	25ns	IMS1625x–25
IMS1629	15ns	IMS1629x–15
	20ns	IMS1629x–20
	25ns	IMS1629x–25
IMS1626	15ns	IMS1626x–15
	20ns	IMS1626x–20
	25ns	IMS1626x–25
IMS1627	15ns	IMS1627x–15
	20ns	IMS1627x–20
	25ns	IMS1627x–25
IMS1635	15ns	IMS1635x–15
	20ns	IMS1635x–20
	25ns	IMS1635x–25
IMS1695	15ns	IMS1695x–15
	20ns	IMS1695x–20
	25ns	IMS1695x–25

Where x refers to packages P, S, E, or W. See also Appendix D.

IMS1800
CMOS
High Performance
256K x 1 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 256K x 1 Bit Organization
- 25, 30, 35 and 45 ns Address Access Times
- 25, 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Outputs
- Three-state Output
- 24 Pin 300-mil DIP, SOJ and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

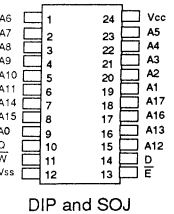
DESCRIPTION

The INMOS IMS1800 is a high performance 256Kx1 CMOS Static RAM. The IMS1800 provides maximum density and speed enhancements with the additional benefits of lower power and superior reliability.

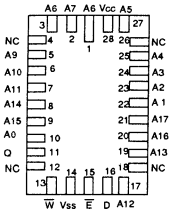
The IMS1800 features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1800 provides a Chip Enable function (E) that can be used to place the device into a low power standby mode.

The IMS1800E is an extended temperature version pending military qualification of the IMS1800M.

PIN CONFIGURATION

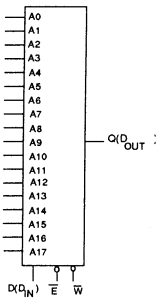


DIP and SOJ

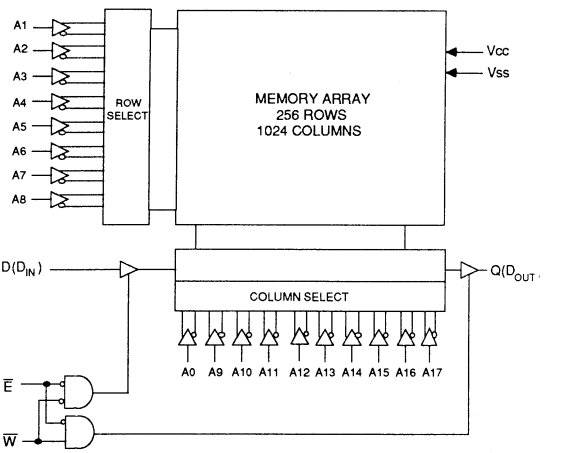


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{17}	ADDRESS INPUTS	Q	DATA OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to 6.0V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-0.5 *		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	

*V_{IL} min = -3.0V for pulse width <10ns, note b

DC ELECTRICAL CHARACTERISTICS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		120	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$E \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		10	mA	$E \geq (V_{CC} - 0.2V)$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	$E \geq (V_{CC} - 0.2V)$. Inputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

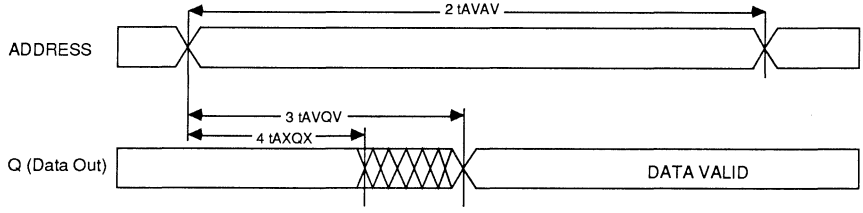
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ TA ≤ 70°C) (VCC = 5.0V ±10%)

READ CYCLE[g]

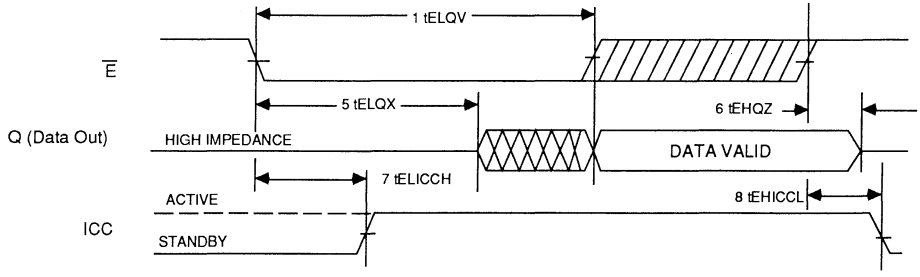
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1800-25 MIN	IMS 1800-25 MAX	IMS 1800-30 MIN	IMS 1800-30 MAX	IMS 1800-35 MIN	IMS 1800-35 MAX	IMS 1800-45 MIN	IMS 1800-45 MAX	UNITS	NOTES
1	t ELQV	t ACS	Chip Enable Access Time		25		30		35		45	ns	
2	t AVAV	t RC	Read Cycle Time	25		30		35		45		ns	c
3	t AVQV	t AA	Address Access Time		25		30		35		45	ns	d
4	t AXQX	t OH	O/P Hold After Addr's Ch'ge	3		3		3		3		ns	
5	t ELQX	t LZ	Chip Enable to O/P Active	3		3		3		3		ns	
6	t EHQZ	t HZ	Chip Disable to O/P Inactive	0	20	0	20	0	20	0	20	ns	f,j
7	t ELICCH	t PU	Chip Enable to Power Up	0		0		0		0		ns	j
8	t ELICCL	t PD	Chip Enable to Power Down		30		30		30		30	ns	j
		t T	Input Rise and Fall Times		50		50		50		50	ns	e,j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



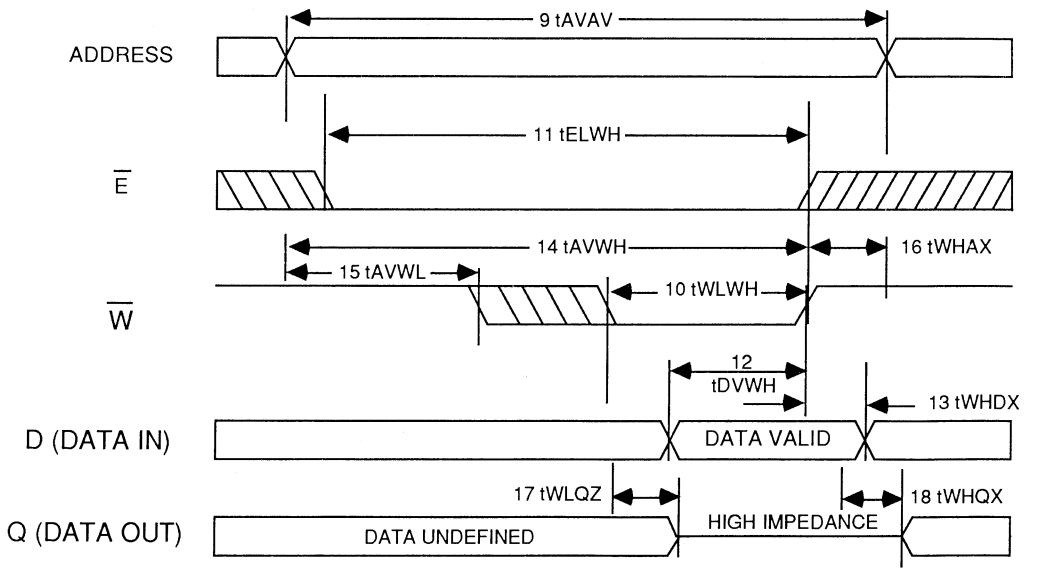
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1800-25 MIN	IMS 1800-25 MAX	IMS 1800-30 MIN	IMS 1800-30 MAX	IMS 1800-35 MIN	IMS 1800-35 MAX	IMS 1800-45 MIN	IMS 1800-45 MAX	UNITS	NOTES
9	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
10	t WLWH	t WP	Write Pulse Width	20		25		30		40		ns	
11	tELWH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
12	tDVWH	t DW	Data Setup to End of Write	10		12		15		20		ns	
13	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
14	tAVWH	t AW	Address Setup to End of Write	20		25		30		40		ns	
15	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
16	tWHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
17	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	20	0	20	ns	f,j
18	tWHQX	t OW	Output Active After End of Write	5		5		5		5		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and W must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$, or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2: $\overline{E}$1 OR E2 CONTROLLED[g,h]



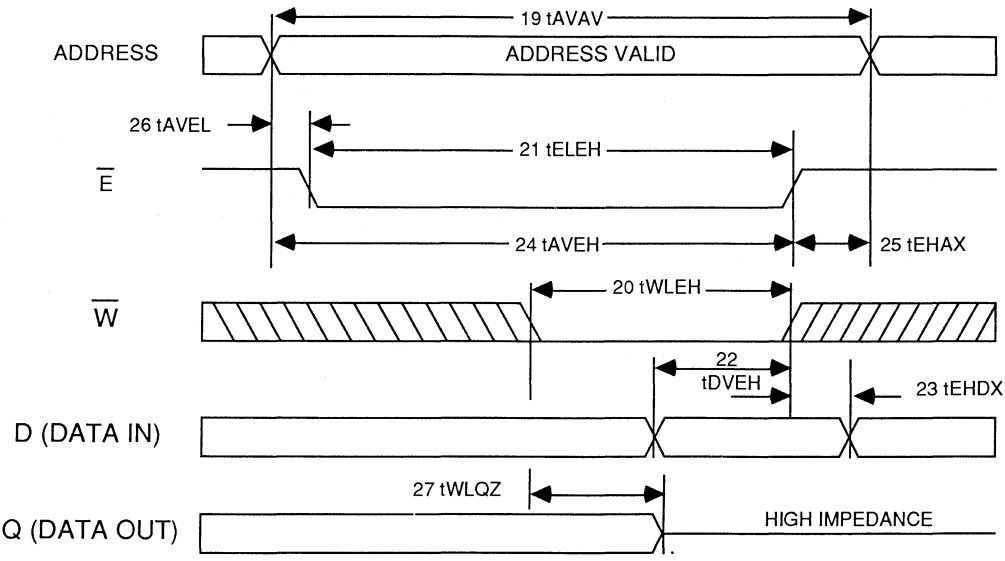
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1800-25 MIN	IMS 1800-25 MAX	IMS 1800-30 MIN	IMS 1800-30 MAX	IMS 1800-35 MIN	IMS 1800-35 MAX	IMS 1800-45 MIN	IMS 1800-45 MAX	UNITS	NOTES
19	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
20	tWLEH	t WP	Write Pulse Width	20		25		30		40		ns	
21	tELEH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
22	tDVEH	t DW	Data Setup to End of Write	10		12		15		20		ns	
23	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
24	tAVEH	t AW	Address Setup to End of Write	20		25		30		40		ns	
25	tEHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
26	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1800 has two control inputs, Chip Enable (/E) and Write Enable (/W), 18 address inputs (A0 -A17), a Data In (D) and a Data Out (Q). The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 18 address inputs are decoded to select one bit out of 256 Kbits. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1800 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1800, that the fundemental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1800. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1800	25ns	Plastic DIP	IMS1800P-25
	25ns	Ceramic DIP	IMS1800S-25
	25ns	SOJ	IMS1800E-25
	25ns	Ceramic LCC	IMS1800W-25
	25ns	Ceramic LCC	IMS1800N-25
	30ns	Plastic DIP	IMS1800P-30
	30ns	Ceramic DIP	IMS1800S-30
	30ns	SOJ	IMS1800E-30
	30ns	Ceramic LCC	IMS1800W-30
	30ns	Ceramic LCC	IMS1800N-30
	35ns	Plastic DIP	IMS1800P-35
	35ns	Ceramic DIP	IMS1800S-35
	35ns	SOJ	IMS1800E-35
	35ns	Ceramic LCC	IMS1800W-35
	35ns	Ceramic LCC	IMS1800N-35
	45ns	Plastic DIP	IMS1800P-45
	45ns	Ceramic DIP	IMS1800S-45
	45ns	SOJ	IMS1800E-45
	45ns	Ceramic LCC	IMS1800W-45
	45ns	Ceramic LCC	IMS1800N-45

IMS1820
CMOS
High Performance
64K x 4 Static RAM

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 64K x 4 Bit Organization
- 25, 30, 35 and 45 ns Address Access Times
- 25, 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Outputs
- Three-state Outputs
- 24 Pin 300-mil DIP, SOJ and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

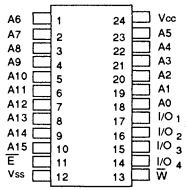
DESCRIPTION

The INMOS IMS1820 is a high performance 64Kx4 CMOS Static RAM. The IMS1820 allows speed enhancements to existing 64K x 4 applications with the additional benefit of reduced power consumption .

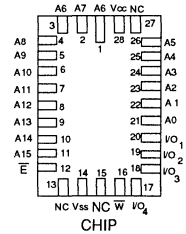
The IMS1820 features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1820 provides a Chip Enable function (/E) that can be used to place the device into a low power standby mode.

The IMS1820E is an extended temperature version pending military qualification of the IMS1820M.

PIN CONFIGURATION

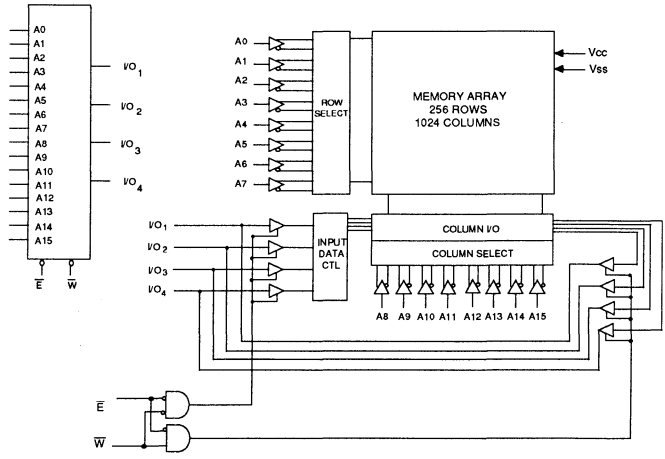


DIP and SOJ



CHIP CARRIER

BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Vcc	POWER (+5V)
W	WRITE ENABLE	Vss	GROUND
I/O-I/O	DATA IN/OUT		
E	CHIP ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5V)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC} + 0.5*	V	All inputs
V_{IL}	Input Logic "0" Voltage	-0.5		0.8	V	All inputs
T_A	Ambient Operating Temperature	0		70	°C	400 linear ft/min air flow

* V_{IL} min = -3.0V for pulse width < 10ns, note b

DC ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

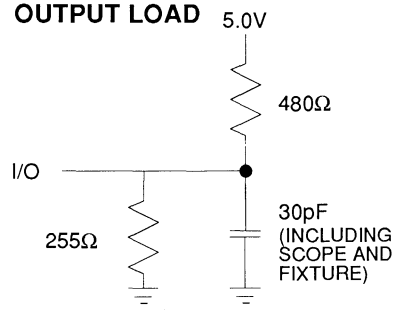
SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		120	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	V_{CC} Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\overline{E1} \ge V_{IH}$ or $E2 \le V_{IL}$. All other inputs at $V_{IN} \le V_{IL}$ or $\ge V_{IH}$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		10	mA	$\overline{E1} \ge (V_{CC} - 0.2V)$ or $E2 \le 0.2V$. All other inputs at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		15	mA	$\overline{E1} \ge (V_{CC} - 0.2V)$ or $E2 \le 0.2V$. Inputs cycling at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC} = max V_{IN} = Vss to V_{CC}
I_{OLK}	Off State Output Leakage Current		±10	µA	V_{CC} = max V_{IN} = Vss to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the outputs unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load ..... See Figure 1

FIGURE 1. OUTPUT LOAD



CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

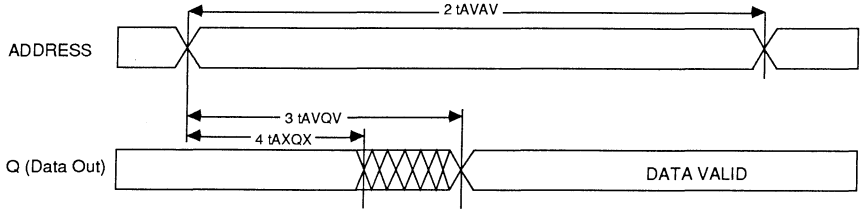
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

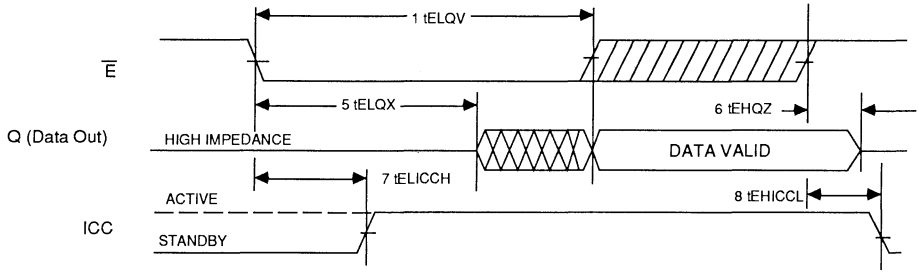
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
1	t ELQV	t ACS	Chip Enable Access Time		25		30		35		45	ns	
2	t AVAV	t RC	Read Cycle Time	25		30		35		45		ns	c
3	t AVQV	t AA	Address Access Time		25		30		35		45	ns	d
4	t AXQX	t OH	O/P Hold After Addr's Ch'ge	3		3		3		3		ns	
5	t ELQX	t LZ	Chip Enable to O/P Active	3		3		3		3		ns	
6	t EHQZ	t HZ	Chip Disable to O/P Inactive	0	12	0	15	0	15	0	20	ns	f,j
7	t ELICCH	t PU	Chip Enable to Power Up	0		0		0		0		ns	j
8	t EHICCL	tPD	Chip Enable to Power Down		30		30		30		30	ns	j
		t T	Input Rise and Fall Times		50		50		50		50	ns	e,j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



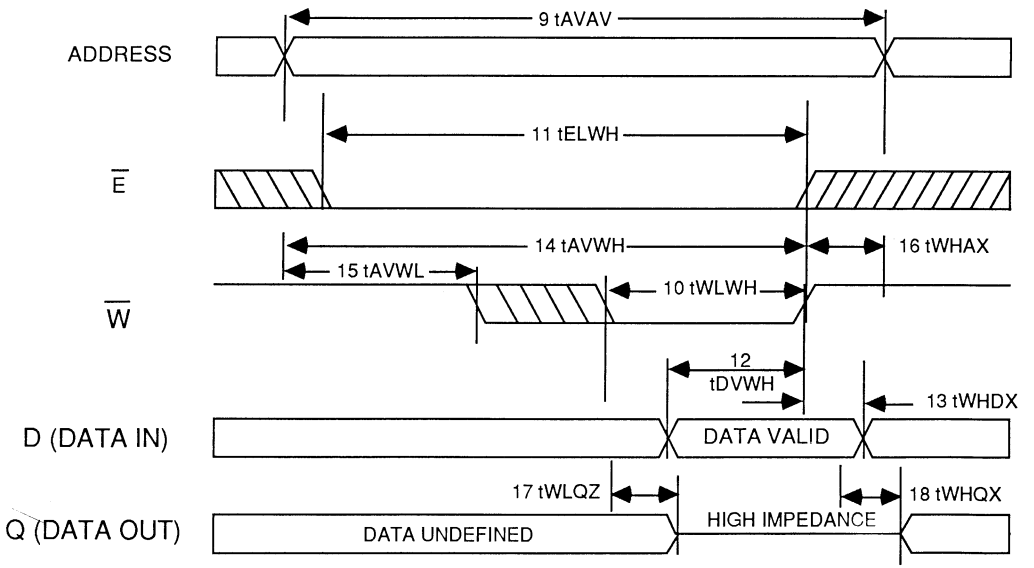
RECOMMENDED AC OPERATING CONDITIONS ($0°C \leq T_A \leq 70°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
9	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
10	t WLWH	t WP	Write Pulse Width	20		25		30		40		ns	
11	tELWH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
12	tDVWH	t DW	Data Setup to End of Write	10		12		15		20		ns	
13	tWHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
14	tAVWH	t AW	Address Setup to End of Write	20		25		30		40		ns	
15	tAVWL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
16	tWHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
17	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f,j
18	tWHQX	t OW	Output Active After End of Write	5		5		5		5		ns	i

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$, or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



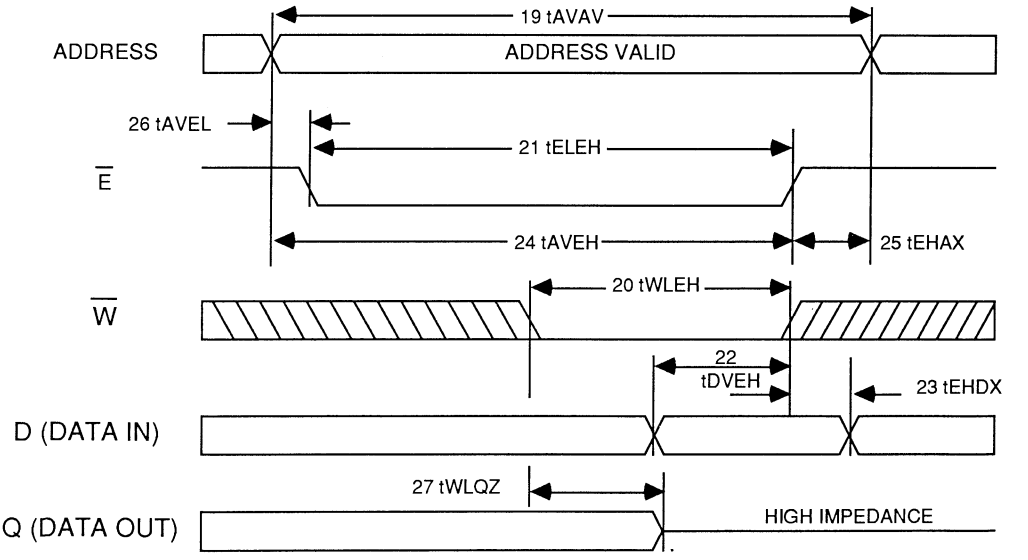
RECOMMENDED AC OPERATING CONDITIONS (0°C ≤ Ta ≤ 70°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1820-25 MIN	IMS 1820-25 MAX	IMS 1820-30 MIN	IMS 1820-30 MAX	IMS 1820-35 MIN	IMS 1820-35 MAX	IMS 1820-45 MIN	IMS 1820-45 MAX	UNITS	NOTES
19	tAVAV	t WC	Write Cycle Time	25		30		35		45		ns	
20	tWLEH	t WP	Write Pulse Width	20		25		30		40		ns	
21	tELEH	t CW	Chip Enable to End of Write	20		25		30		40		ns	
22	tDVEH	t DW	Data Setup to End of Write	10		12		15		20		ns	
23	tEHDX	t DH	Data Hold after End of Write	0		0		0		0		ns	
24	tAVEH	t AW	Address Setup to End of Write	20		25		30		40		ns	
25	tEHAX	t WR	Address Hold after End of Write	2		2		0		0		ns	
26	tAVEL	t AS	Address Setup to Start of Write	0		0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	10	0	10	0	15	0	20	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1820 has two control inputs, Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), and four data I/O lines.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one 4 bit word out of 64K words. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq V_{IH}$ min with /E $\leq V_{IL}$ max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1820 is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and $\overline{Q}$ connected together in a common I/O configuration. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1820, that the fundemental rules in regard to memory board layout be followed to ensure proper system operation.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1820. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS1820	25ns	Plastic DIP	IMS1820P-25
	25ns	Ceramic DIP	IMS1820S-25
	25ns	SOJ	IMS1820E-25
	25ns	Ceramic LCC	IMS1820W-25
	25ns	Ceramic LCC	IMS1820N-25
	30ns	Plastic DIP	IMS1820P-30
	30ns	Ceramic DIP	IMS1820S-30
	30ns	SOJ	IMS1820E-30
	30ns	Ceramic LCC	IMS1820W-30
	30ns	Ceramic LCC	IMS1820N-30
	35ns	Plastic DIP	IMS1820P-35
	35ns	Ceramic DIP	IMS1820S-35
	35ns	SOJ	IMS1820E-35
	35ns	Ceramic LCC	IMS1820W-35
	35ns	Ceramic LCC	IMS1820N-35
	45ns	Plastic DIP	IMS1820P-45
	45ns	Ceramic DIP	IMS1820S-45
	45ns	SOJ	IMS1820E-45
	45ns	Ceramic LCC	IMS1820W-45
	45ns	Ceramic LCC	IMS1820N-45

military RAMs

IMS1203M
CMOS
High Performance
4K x 1 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to + 125° C)
- 4K x 1 Bit Organization
- 25, 35, and 45 nsec Access Times
- Single +5V ± 10% Operation
- Power Down Function
- Fully TTL Compatible
- Separate Data Input and Output
- Three-state Output
- Standard Military Drawing version available (refer to page B-7)
- 18-Pin, 300-mil DIP (JEDEC Std.) and FP

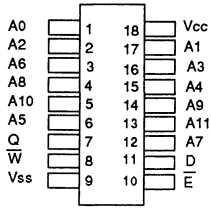
DESCRIPTION

The INMOS IMS1203M is a high speed CMOS 4Kx1 static RAM processed in full compliance to MIL-STD-883C. The IMS1203M provides performance enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1203M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1203M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

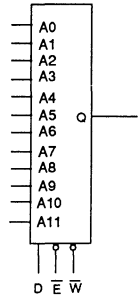
The IMS1203M is a VLSI static RAM intended for military temperature applications that demand superior performance and reliability.

PIN CONFIGURATION

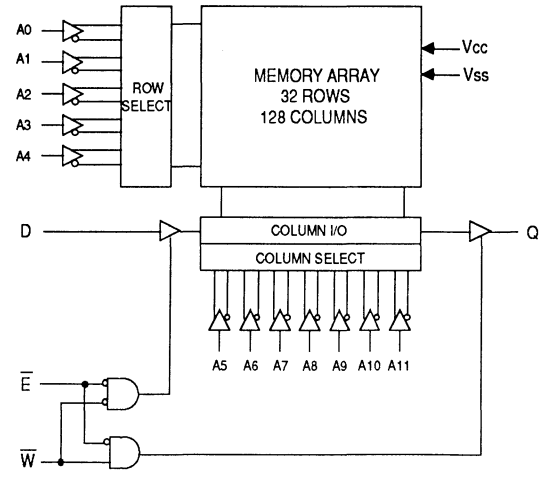


DIP &
FLAT PACK

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss	GROUND
D	DATA INPUT		
$\overline{E}$	CHIP ENABLE		
Q	DATA OUTPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (V_{CC}+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC}+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3.0 V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		80	mA	$t_{AVAV} = t_{AVAV}$(min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	$\overline{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\overline{E} \geq$ (Vcc - 0.2). All other inputs at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\overline{E} \geq$ (Vcc - 0.2) . Inputs cycling at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 12mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

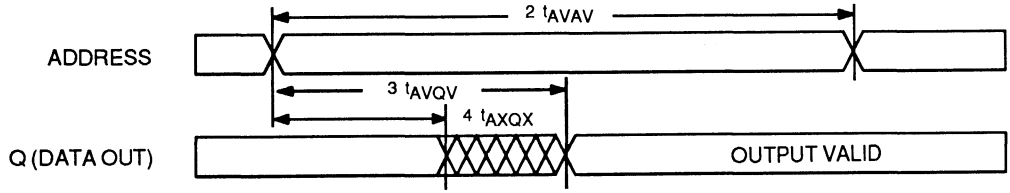
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

READ CYCLE[g]

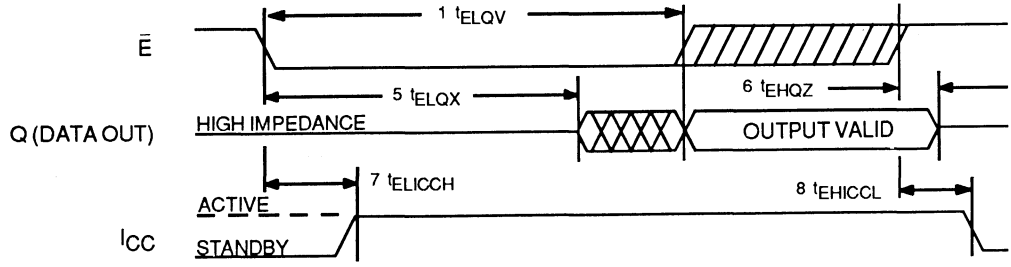
NO.	SYMBOL		PARAMETER	1203M-25		1203M-35		1203M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



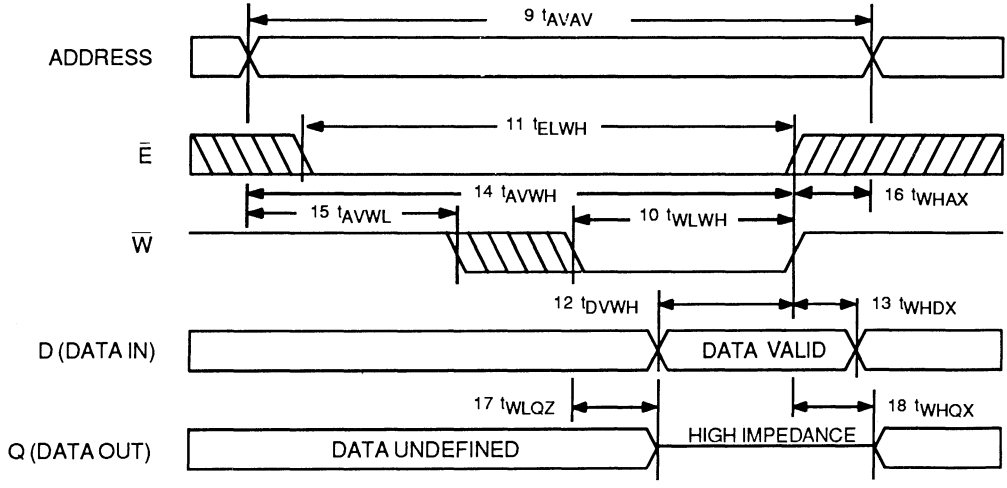
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1203M-25		IMS1203M-35		IMS1203M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0		ns	i, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



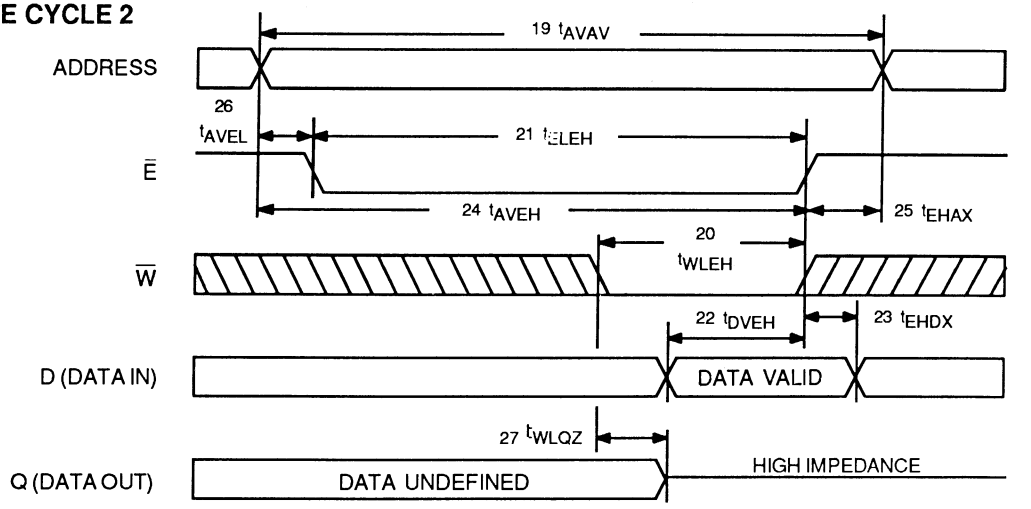
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1203M-25		IMS1203M-35		IMS1203M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	25		35		45		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1203M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs (A_0-A_{11}), a Data In (D) and a Data Out (Q). The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one bit out of 4K bits. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1203M is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to low. In the case of $\overline{W}$ falling last, the output buffer will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1203M, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

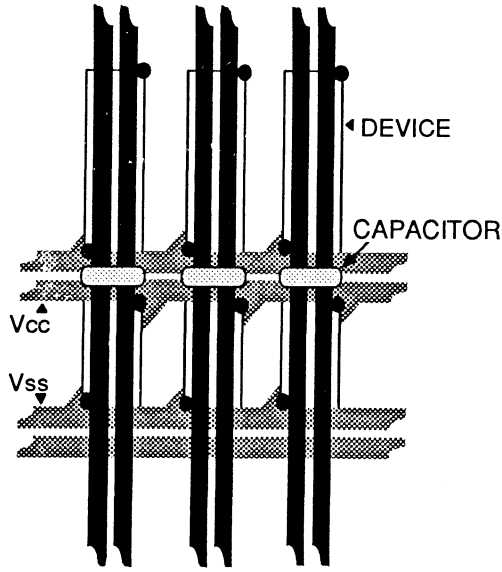
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1203M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

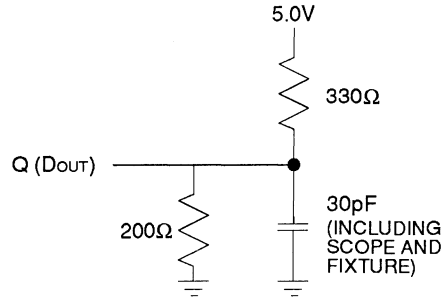
Since the current transients associated with the operation of the high speed IMS1203M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1203M	25ns	CERAMIC DIP	IMS1203S-25M
	25ns	FLAT PACK	IMS1203A-25M
	35ns	CERAMIC DIP	IMS1203S-35M
	35ns	FLAT PACK	IMS1203A-35M
	45ns	CERAMIC DIP	IMS1203S-45M
	45ns	FLAT PACK	IMS1203A-45M

IMS1223M
CMOS
High Performance
1K x 4 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to + 125° C)
- 1K x 4 Bit Organization
- 25, 35, and 45 nsec Access Times
- Fully TTL Compatible
- Single +5V ± 10% Operation
- Power Down Function
- Common Data Input and Output
- Three-state Output
- Standard Military Drawing version available (refer to page B-7)
- 18-Pin, 300-mil DIP (JEDEC Std.) and FP

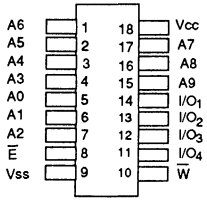
DESCRIPTION

The INMOS IMS1223M is a high speed CMOS 1Kx4 static RAM processed in full compliance to MIL-STD-883C. The IMS1223M provides performance enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1223M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1223M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

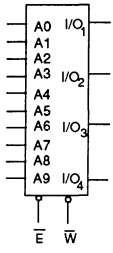
The IMS1223M is a VLSI static RAM intended for military temperature applications that demand superior performance and reliability.

PIN CONFIGURATION

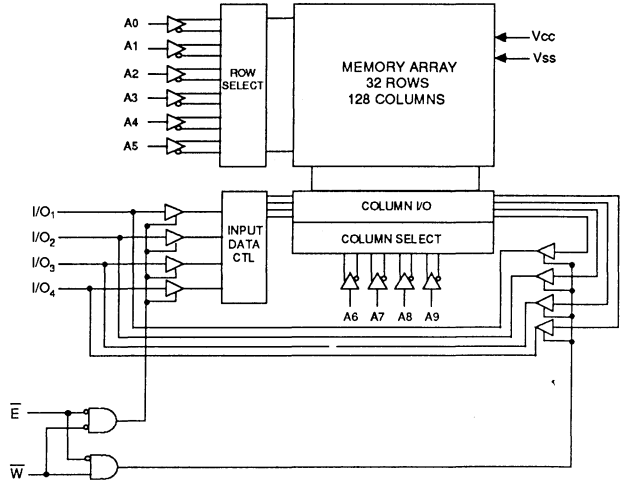


DIP &
FLAT PACK

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_9	ADDRESS INPUTS	Vcc	POWER
W̄	WRITE ENABLE	Vss	GROUND
Ē	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		110	mA	$t_{AVAV} = t_{AVAV}$(min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	E ≥ V_{IH} . All other inputs at $V_{IN} \leq V_{IL}$ or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	E ≥ (Vcc - 0.2) . All other inputs at $V_{IN} \leq$ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	E ≥ (Vcc - 0.2) . Inputs cycling at $V_{IN} \leq$ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	4	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

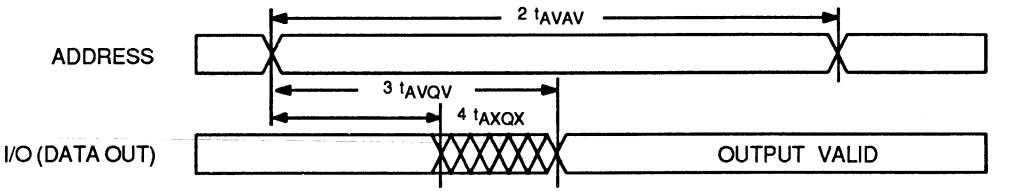
RECOMMENDED AC OPERATING CONDITIONS $-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

READ CYCLE[g]

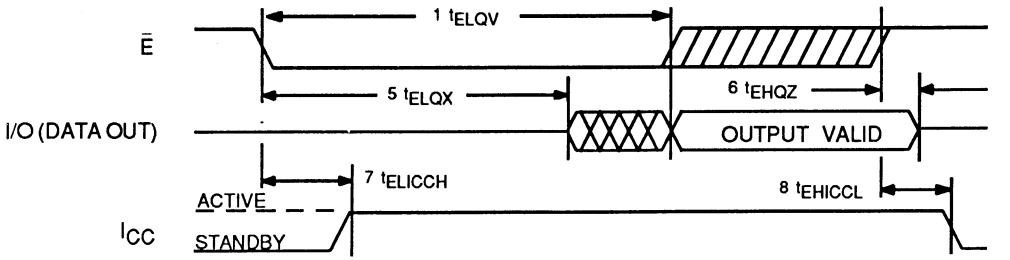
NO.	SYMBOL		PARAMETER	1223M-25		1223M-35		1223M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		25		35		45	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	25		35		45		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		25		35		45	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Disable to Power Down		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLES 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



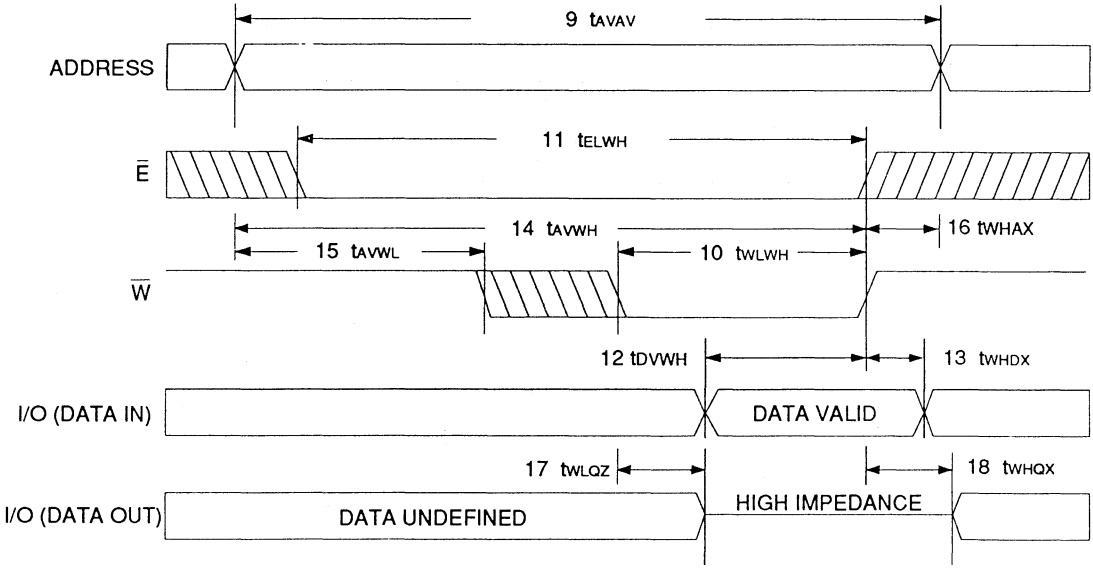
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ±10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

NO.	SYMBOL		PARAMETER	1223M-25		1223M-35		1223M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	20		30		40		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	15		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
12	t_{DVWH}	t_{DW}	Data Setup to End of Write	15		20		25		ns	
13	t_{WHDX}	t_{DH}	Data Hold after End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Setup to End of Write	20		30		40		ns	
15	t_{AVWL}	t_{AS}	Address Setup to Start of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold after End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active after End of Write	5		5		5		ns	i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



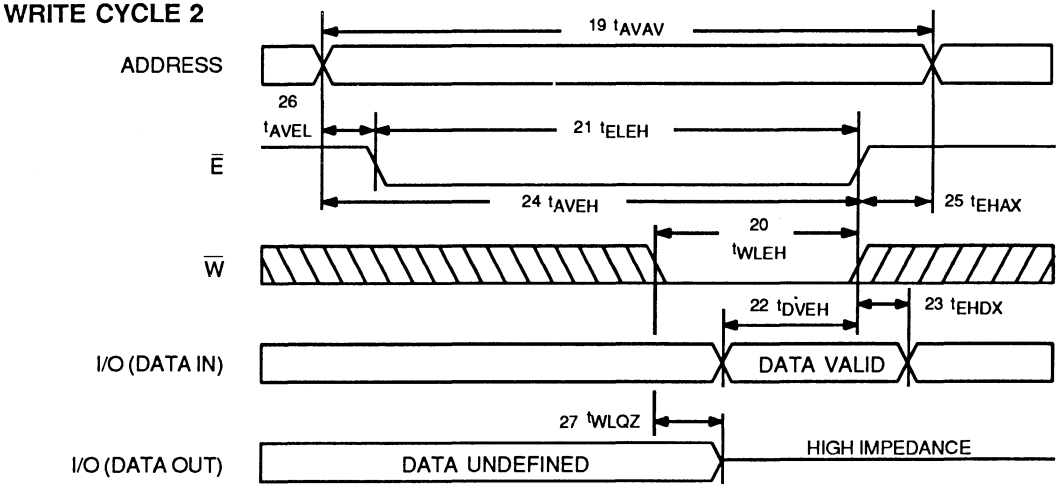
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	1223M-25		1223M-35		1223M-45		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	20		30		40		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	15		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		30		40		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	10		15		15		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	20		30		40		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	20	ns	f, j

Note f: Measured ± 200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1223M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), ten address inputs (A_0-A_9), and four Data I/O lines. The $\overline{E}$ input controls device selection as well as active and standby modes. With $\overline{E}$ low, the device is selected and the ten address inputs are decoded to select one four-bit word out of 1K words. Read and Write operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The outputs remain active throughout READ CYCLE 1 and are valid at the specified address access time. The address inputs may change at access time and as long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable when $\overline{E}$ goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when $\overline{E}$ goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1223M is initiated by the latter of $\overline{E}$ or $\overline{W}$ to transition from a high to a low. In the case of $\overline{W}$ falling last, the output buffers will be turned on t_{ELQX} after the falling edge of $\overline{E}$ (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common I/O configurations. To avoid bus contention, input data should not become active on the I/O bus until t_{WLQZ}.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high at the end of the cycle with $\overline{E}$ active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high the outputs remain in the high impedance state.

APPLICATION

It is imperative when designing with any very high speed memory, such as the IMS1223M, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

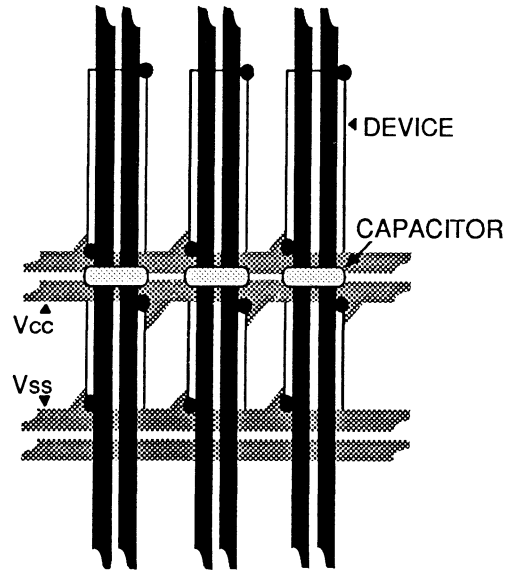
Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1223M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

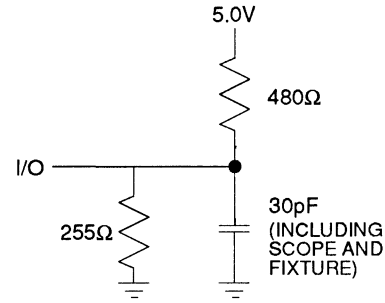
Since the current transients associated with the operation of the high speed IMS1223M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	Din	Write

Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1223M	25ns	CERAMIC DIP	IMS1223S-25M
	25ns	FLAT PACK	IMS1223A-25M
	35ns	CERAMIC DIP	IMS1223S-35M
	35ns	FLAT PACK	IMS1223A-35M
	45ns	CERAMIC DIP	IMS1223S-45M
	45ns	FLAT PACK	IMS1223A-45M

IMS1400M

High Performance 16K Static RAM MIL-STD-883C

FEATURES

- Full Military Temperature Operating Range (-55°C to +125°C)
- MIL-STD-883C Processing
- 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

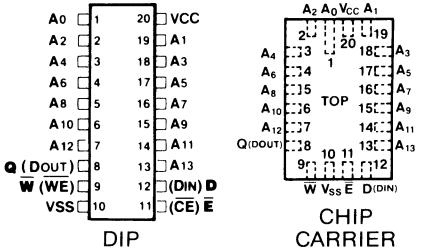
DESCRIPTION

The INMOS IMS1400M is a high performance 16Kx1 Static RAM processed in full compliance to MIL-STD-883C with access times as fast as 45nsec and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary NMOS technology.

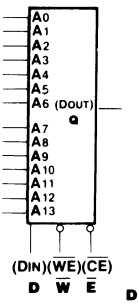
The IMS1400M features fully static operation requiring no external clocks or timing strobes with equal access and cycle times. Additionally, the IMS1400M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode reducing consumption to less than 165mW.

The IMS1400M is a high speed VLSI RAM intended for military applications which demand superior performance and reliability.

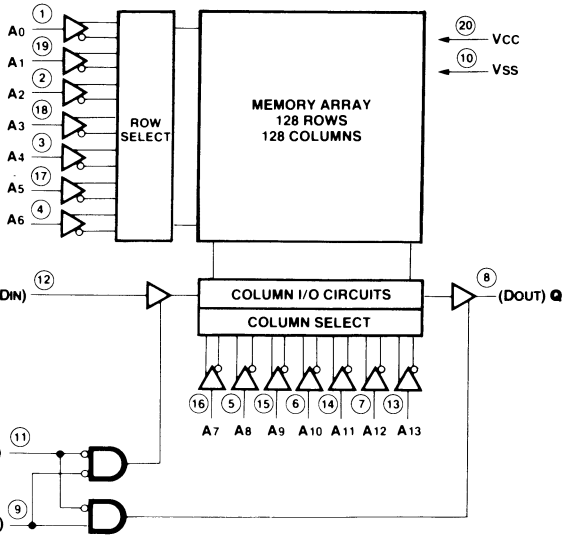
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A0 - A13 ADDRESS INPUTS	VCC POWER(+5V)
W (WE) WRITE ENABLE	VSS GROUND
E (CE) CHIP ENABLE	
D (DIN) DATA INPUT	
Q (DOUT) DATA OUTPUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −65°C to 135°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 16mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

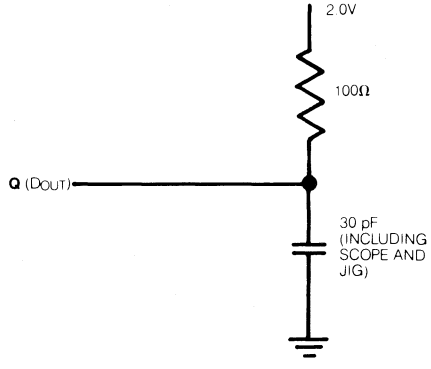
Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



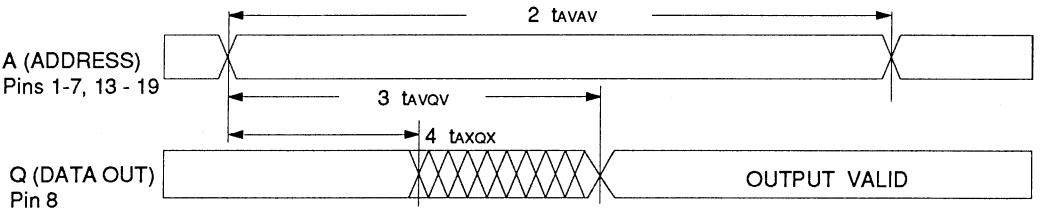
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

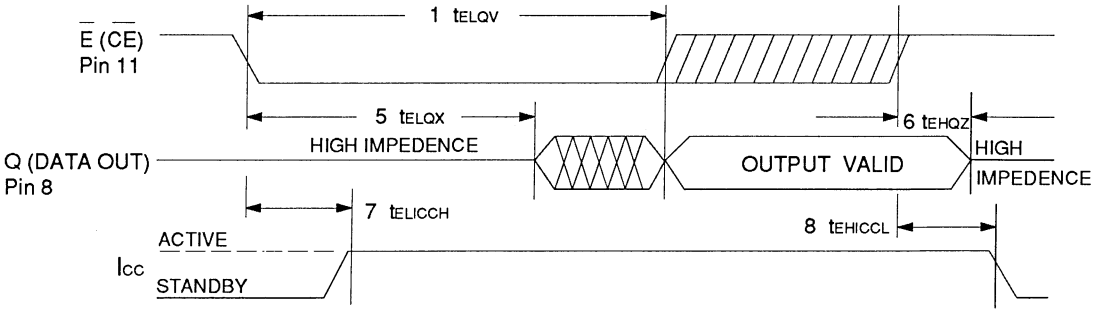
NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	40		50		65		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		40		50		65	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		0		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	3		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Disable	0	25	0	30	0	40	ns	f
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down	0	45	0	55	0	70	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2 [c]



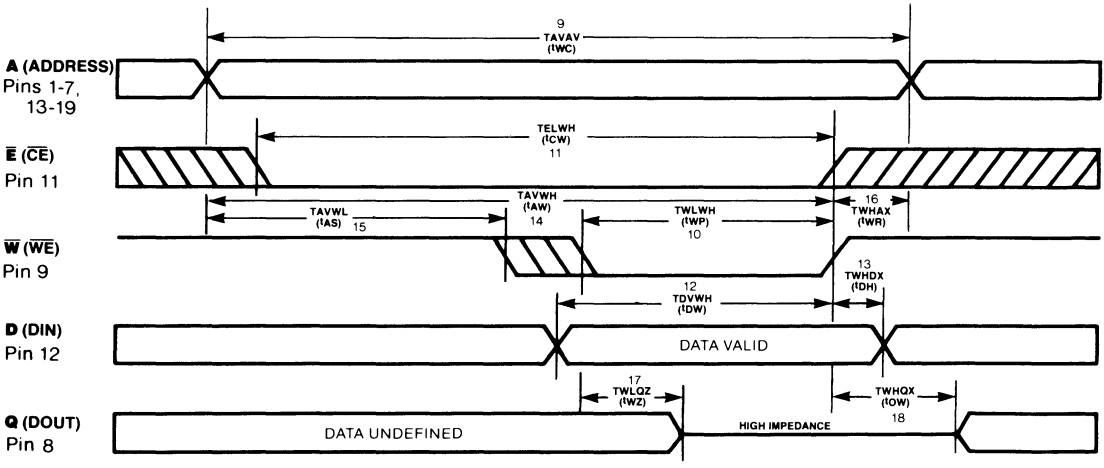
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		25		30		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		8		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	8		8		8		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0	25	0	30	0	40	ns	g, j

Note f: Measured ±200mV from steady state output voltage.
Note g: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



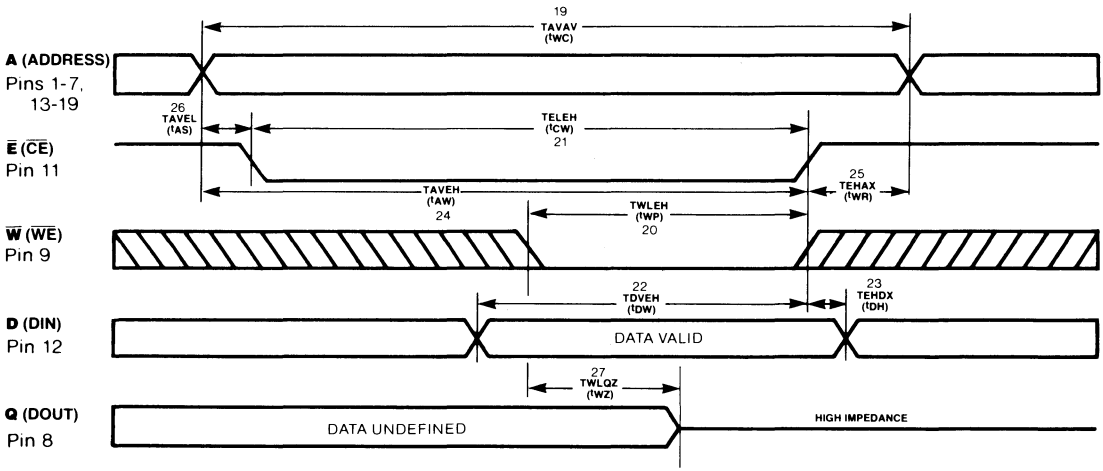
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL		PARAMETER	1400M-45		1400M-55		1400M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	40		50		65		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		60		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		20		23		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	5		5		10		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		50		55		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		10		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	−5		−5		−5		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	28	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transition.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1400M has two control inputs: Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), 14 address inputs, a data in (D_{IN}) and a data out (D_{OUT}).

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the 14 address inputs are decoded to select one memory cell out of 16,385. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than ¼ of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout a READ CYCLE 1 and is valid at the specified address access time. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the input (D_{IN}) is written into the selected cell, and the output (D_{OUT}) is in high impedance.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, D_{OUT} becomes active.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, D_{OUT} remains in the high impedance state.

APPLICATION

To ensure proper operation of the extended temperature IMS1400M in a system environment, it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see Figure 2). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

Also, to prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry.

TERMINATION

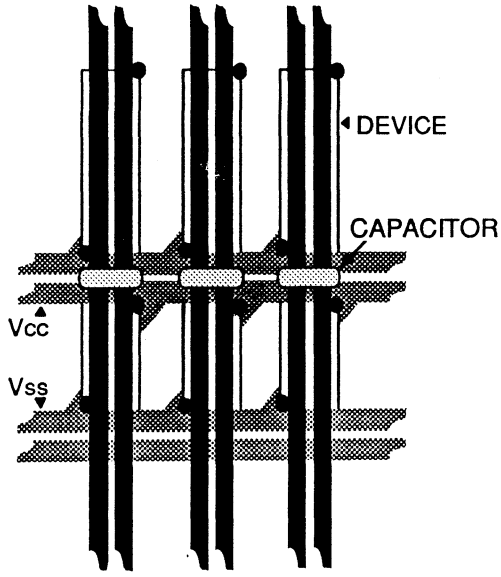
Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

The use of proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are some of the most important, yet basic rules to be followed.

The rules are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1400M	45ns	CERAMIC DIP	IMS1400S-45M
	45ns	CERAMIC LCC	IMS1400N-45M
	55ns	CERAMIC DIP	IMS1400S-55M
	55ns	CERAMIC LCC	IMS1400N-55M
	70ns	CERAMIC DIP	IMS1400S-70M
	70ns	CERAMIC LCC	IMS1400N-70M

IMS1403M
IMS1403LM

CMOS
High Performance
16K x 1 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to +125° C)
- 16K x 1 Bit Organization
- 35, 45, 55 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Single +5V ± 10% Operation
- Power Down Function
- Pin Compatible with IMS1400M
- Standard Military Drawing version available
- 20-Pin, 300-mil DIP & LCC (JEDEC Std.)
- Battery Backup Operation - 2V Data Retention (L version only)

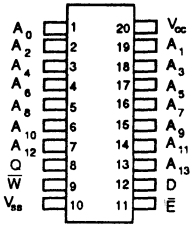
DESCRIPTION

The INMOS IMS1403M is a high speed 16K x 1 CMOS static RAM processed in full compliance to MIL-STD-883C. The IMS1403M provides maximum density and performance enhancements with the additional CMOS benefits of lower power and superior reliability.

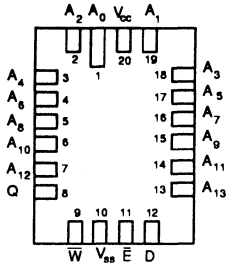
The IMS1403M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1403LM is a low power version offering battery backup data retention operating from a 2 volt supply.

PIN CONFIGURATION

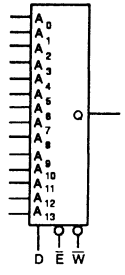


DIP



CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM

PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	V_{CC}	POWER
$\overline{E}$	CHIP ENABLE	V_{SS}	GROUND
D	DATA INPUT		

November 1988

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS}.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+.5)V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

* V_{IL} Min = -3.0V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$) [a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current		75	mA	$t_{AVAV} = t_{AVAV}$ (min)
I_{CC2}	V_{CC} Power Supply Current (Standby,Stable TTL Input Levels)		15	mA	$\overline{E} \ge V_{IH}$ All other inputs at $V_{IN} \le V_{IL}$ or $\ge V_{IH}$
I_{CC3}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		5	mA	$\overline{E} \ge (V_{CC} - 0.2)$ All other inputs at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{CC4}	V_{CC} Power Supply Current (Standby, Cycling CMOS Input Levels)		10	mA	$\overline{E} \ge (V_{CC} - 0.2)$ Inputs cycling at $V_{IN} \le 0.2$ or $\ge (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±5	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current		±10	µA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 16mA

Note a: I_{CC} is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels.....V_{SS} to 3V
Input Rise and Fall Times.....5ns
Input and Output Timing Reference Levels.....1.5V
Output Load.....See Figure 1

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	$\Delta V = 0$ to 3V
C_{OUT}	Output Capacitance	4	pF	$\Delta V = 0$ to 3V

Note b: This parameter is sampled and not 100% tested.

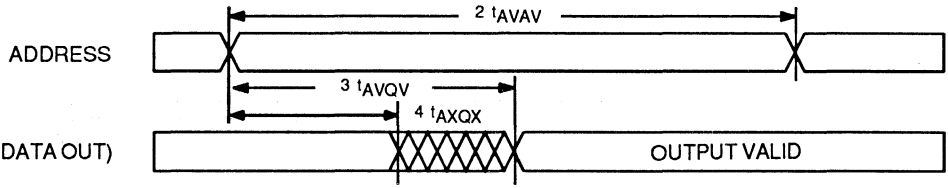
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

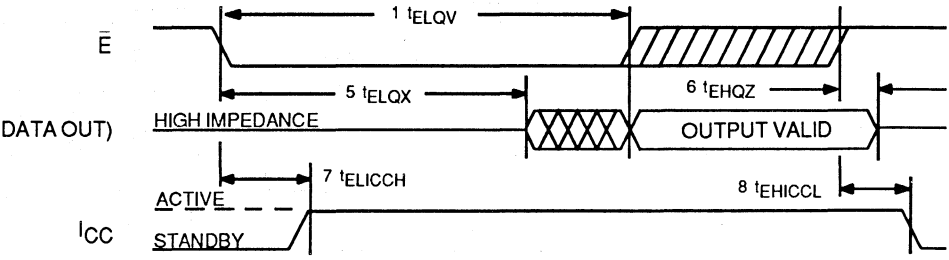
NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read CycleTime	35		40		50		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		35		40		50	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	20	0	25	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		30		30		30	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



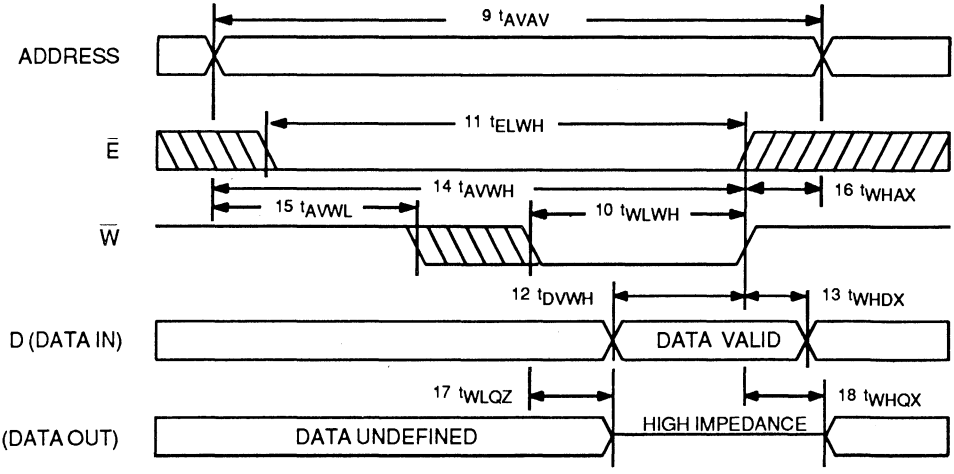
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	30		40		50		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	20		20		25		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	30		35		45		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	30		35		45		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	0		0		0			i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



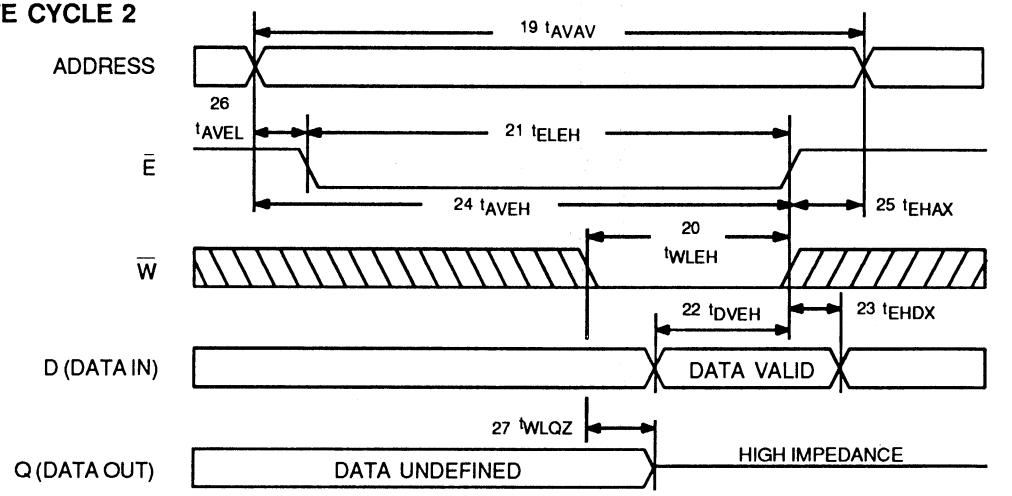
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 2: $\bar{E}$ CONTROLLED [g, h]

NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	30		40		50		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		20		25		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	30		35		45		ns	
22	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		15		20		ns	
23	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
24	t_{AVEH}	t_{AW}	Address Set-up to End of Write	30		35		45		ns	
25	t_{EHAX}	t_{WR}	Address Hold After End of Write	0		0		0		ns	
26	t_{AVEL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	20	0	25	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\bar{E}$ and $\bar{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\bar{E}$ or $\bar{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\bar{W}$ is low when $\bar{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1403M has two control inputs, Chip Enable (/E) and Write Enable (/W), 14 address inputs (A0 -A13), a Data In (D) and a Data Out (Q). The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the14 address inputs are decoded to select one bit out of 16K bits. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq V_{IH}$ min with /E $\leq V_{IL}$ max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1403M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval, it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. Contention can be avoided in a carefully designed system. During a write cycle, data on the input is written into the selected cells and the output is floating.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

APPLICATION

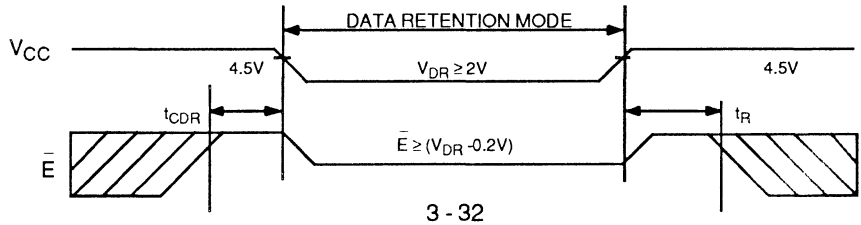
It is imperative when designing with any very high speed memory, such as the IMS1403M, that the fundamental rules in regard to memory board layout be followed to ensure proper system operation.

DATA RETENTION (L version only) (-55°C $\leq T_A \leq$ 125°C)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$ $\bar{E} \geq (V_{CC} - 0.2V)$
I_{CCDR1}	Data Retention Current		3	400	µA	V_{CC} = 3.0 volts
I_{CCDR2}	Data Retention Current		2	250	µA	V_{CC} = 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC} = Read Cycle Time)

*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION



POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1403M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1403M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

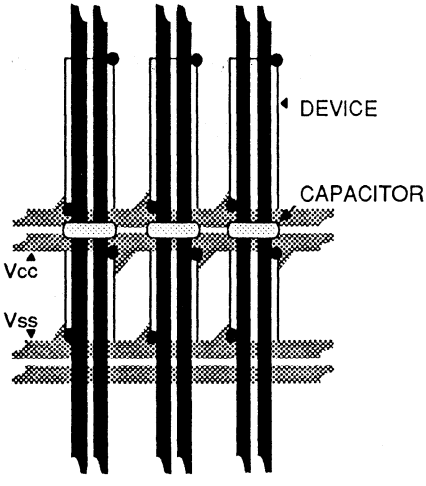
The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

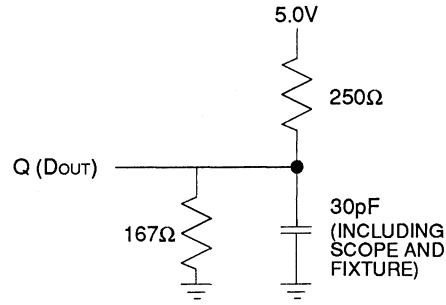
The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1403M IMS 1403LM	35ns	CERAMIC DIP	IMS1403S-35M	IMS1403LS35M
	35ns	CERAMIC LCC	IMS1403N-35M	IMS1403LN35M
	45ns	CERAMIC DIP	IMS1403S-45M	IMS1403LS45M
	45ns	CERAMIC LCC	IMS1403N-45M	IMS1403LN45M
	55ns	CERAMIC DIP	IMS1403S-55M	IMS1403LS55M
	55ns	CERAMIC LCC	IMS1403N-55M	IMS1403LN55M

IMS1420M
High Performance 4Kx4 Static RAM MIL-STD-883C

FEATURES

- Full Military Temperature Operating Range (-55° C to + 125° C)
- MIL-STD-883C Processing
- 4Kx4 Bit Organisation
- 55 and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Input and Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 20-Pin, 300-mil DIP (JEDEC Std.)
- 20-Pin Ceramic LCC (JEDEC Std.)

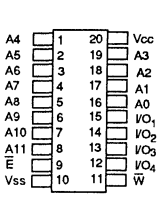
DESCRIPTION

The INMOS IMS1420M is a high performance 4Kx4 Static RAM processed in full compliance to MIL-STD-883C with access times of 55ns and 70ns and a maximum power consumption of 660mW. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary NMOS technology.

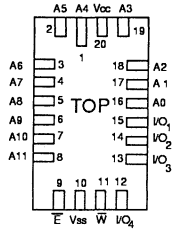
The IMS1420M features fully static operation requiring no external clocks or timing strobes with equal access and cycle times. Additionally, the IMS1420M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode reducing consumption to less than 165mW.

The IMS1420M is a high speed VLSI RAM intended for military applications which demand high performance and reliability.

PIN CONFIGURATION

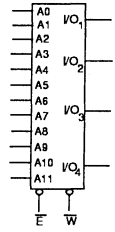


DIP

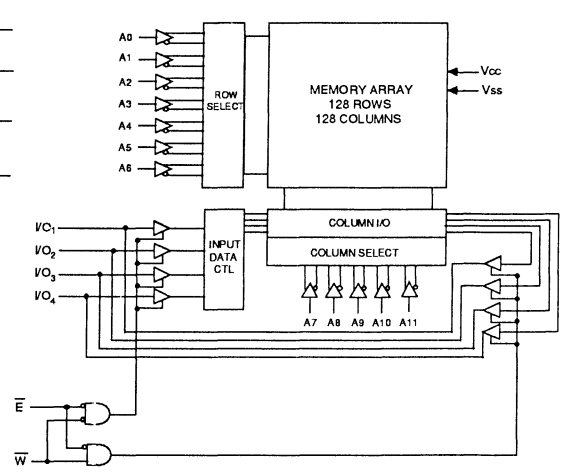


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss GROUND
$\overline{E}$	CHIP ENABLE	
I/O	DATA IN/OUT	

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V_{SS} . . . . . −3.5 to 7.0V
Temperature Under Bias . . . . . −65°C to 135°C
Storage Temperature (Ambient) . . . . . −65°C to 150°C
Power Dissipation 1W
DC Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.4		6.0	V	All Inputs
V_{IL}	Input Logic "0" Voltage	−2.0		0.8	V	All Inputs
T_A	Ambient Operating Temperature	−55		125	°C	400 Linear ft/min transverse air flow

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average V_{CC} Power Supply Current AC		120	mA	$t_C = t_C$ min
I_{CC2}	V_{CC} Power Supply Current (Standby)		30	mA	$\overline{E} \geq V_{IH}$ min
I_{IN}	Input Leakage Current (Any Input)	−10	10	μA	V_{CC} = max $V_{IN} = V_{SS}$ to V_{CC}
I_{OLK}	Off State Output Leakage Current	−50	50	μA	V_{CC} = max $V_{OUT} = V_{SS}$ to V_{CC}
V_{OH}	Output Logic "1" Voltage $I_{OUT} = -4mA$	2.4		V	
V_{OL}	Output Logic "0" Voltage $I_{OUT} = 8mA$		0.4	V	

AC TEST CONDITIONS[a]

Input Pulse Levels . . . . . V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . . See Figure 1

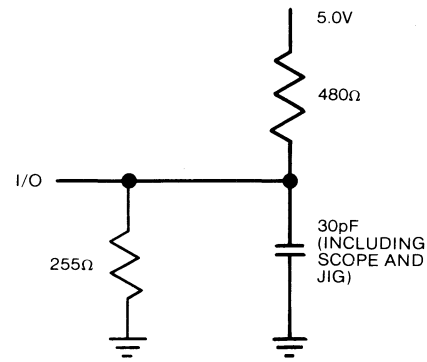
Note a: Operation to specifications guaranteed 2ms after V_{CC} applied.

CAPACITANCE[b] ($T_A = 25°C$, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNIT	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
$C_{\overline{E}}$	$\overline{E}$ Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

FIGURE 1. OUTPUT LOAD



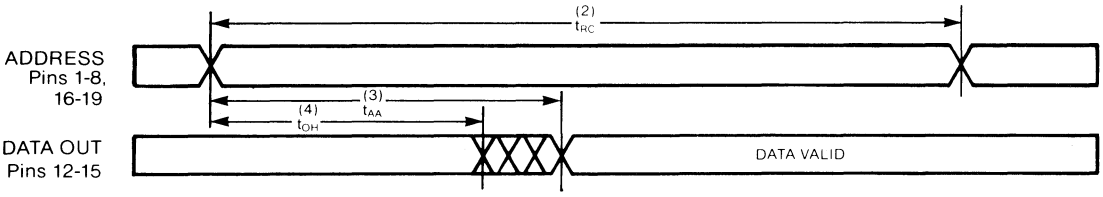
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE

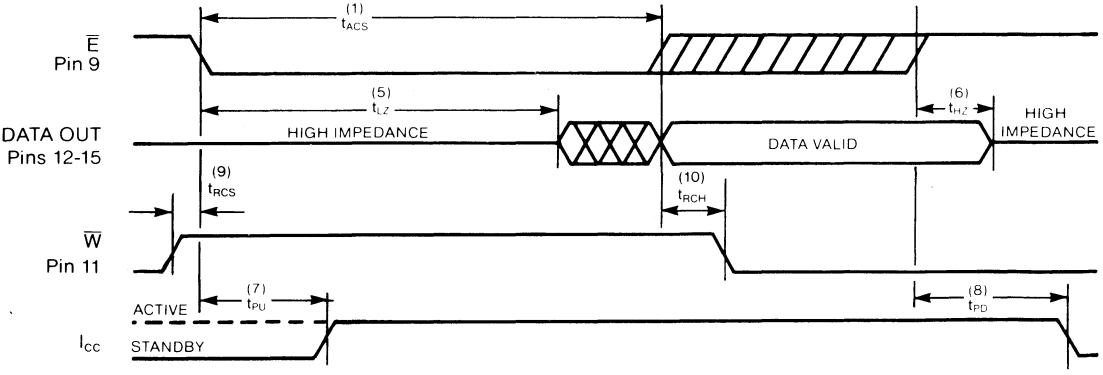
NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
1	t_{ACS}	Chip Enable Access Time		55		70	ns	
2	t_{RC}	Read Cycle Time	55		70		ns	c
3	t_{AA}	Address Access Time		55		70	ns	d
4	t_{OH}	Output Hold After Address Change	3		3		ns	j
5	t_{LZ}	Chip Enable to Output Active	15		15		ns	j
6	t_{HZ}	Chip Disable to Output Disable		25		30	ns	f
7	t_{PU}	Chip Enable to Power Up	0		0		ns	j
8	t_{PD}	Chip Disable to Power Down	0	55	0	70	ns	j
9	t_{RCS}	Read Command Set-up Time	−5		−5		ns	
10	t_{RCH}	Read Command Hold Time	−5		−5		ns	
	t_T	Input Rise and Fall Times		50		50	ns	e

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



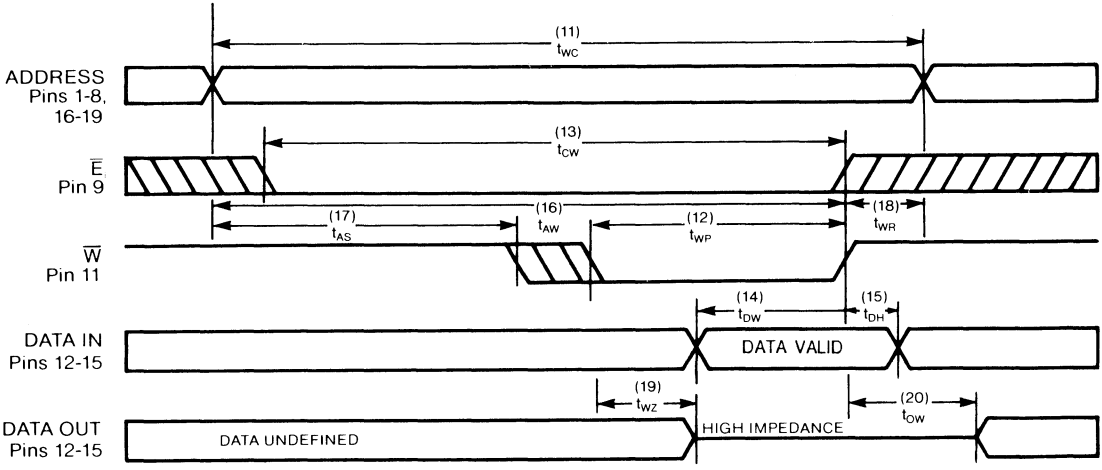
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
11	t_{WC}	Write Cycle Time	55		70		ns	
12	t_{WP}	Write Pulse Width	45		65		ns	
13	t_{CW}	Chip Enable to End of Write	45		65		ns	
14	t_{DW}	Data Set-up to End of Write	25		30		ns	
15	t_{DH}	Data Hold After End of Write	3		5		ns	
16	t_{AW}	Address Set-up to End of Write	45		65		ns	
17	t_{AS}	Address Set-up to Beginning of Write	0		0		ns	
18	t_{WR}	Address Hold After End of Write	5		5		ns	
19	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f
20	t_{OW}	Output Active After End of Write	0		0		ns	g

Note f: Measured ± 200mV from steady state output voltage.
Note g: If $\overline{E}$ goes high with $\overline{W}$ low, Output remains in HIGH impedance state.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 1



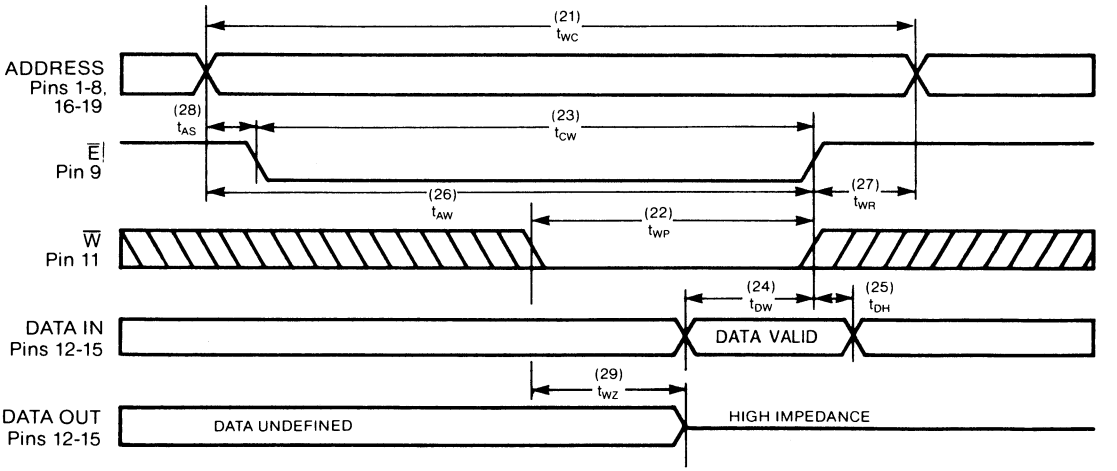
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC}$ = 5.0V ± 10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[h]

NO.	SYMBOL	PARAMETER	IMS1420M-55		IMS1420M-70		UNITS	NOTES
			MIN	MAX	MIN	MAX		
21	t_{WC}	Write Cycle Time	55		70		ns	
22	t_{WP}	Write Pulse Width	45		65		ns	
23	t_{CW}	Chip Enable to End of Write	45		65		ns	
24	t_{DW}	Data Set-up to End of Write	25		30		ns	
25	t_{DH}	Data Hold After End of Write	5		5		ns	
26	t_{AW}	Address Set-up to End of Write	40		60		ns	
27	t_{WR}	Address Hold After End of Write	5		5		ns	
28	t_{AS}	Address Set-up to Beginning of Write	−5		−5		ns	
29	t_{WZ}	Write Enable to Output Disable	0	25	0	30	ns	f

Note f: Measured ± 200mV from steady state output voltage.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1420M has two control inputs, Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$), twelve address inputs, and four Data I/O lines.

When V_{CC} is first applied to pin 20, a circuit associated with the $\overline{E}$ input forces the device into the lower power standby mode regardless of the state of the $\overline{E}$ input. After V_{CC} is applied for 2ms the $\overline{E}$ input controls device selection as well as active and standby modes.

With $\overline{E}$ low, the device is selected and the twelve address inputs are decoded to select one 4-bit word out of 4096. READ and WRITE operations on the memory cell are controlled by $\overline{W}$ input. With $\overline{E}$ high, the device is deselected, the output is disabled, and the power consumption is reduced to less than one-third of the active mode power.

READ CYCLE

A read cycle is defined as $\overline{W} \geq V_{IH}$ min with $\overline{E} \leq V_{IL}$ max. Read access time is measured from either $\overline{E}$ going low or from valid address.

The READ CYCLE 1 waveform on page 3 shows a read access that is initiated by a change in the address inputs while $\overline{E}$ is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of 3ns. As long as $\overline{E}$ remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform on page 3 shows a read access that is initiated by $\overline{E}$ going low. As long as address is stable within 5ns after $\overline{E}$ goes low, valid data is at the output at the specified Chip Enable access time. If address is not valid within 5ns after $\overline{E}$ goes low, the timing is as specified in the READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

A write cycle is initiated by the latter of $\overline{W}$ or $\overline{E}$ going low, and terminated by $\overline{W}$ (WRITE CYCLE 1) or $\overline{E}$ (WRITE CYCLE 2) going high. During the write cycle, data on the inputs is written into the selected cells, and the outputs are floating.

If a write cycle is initiated by $\overline{W}$ going low, the address must be stable for the WRITE CYCLE 1 set-up time. If a write cycle is initiated by $\overline{E}$ going low, the address need not be stable until a maximum of 5ns after $\overline{E}$ goes low. The address must be held stable for the entire write cycle. After $\overline{W}$ or $\overline{E}$ goes high to terminate the write cycle, addresses may change. If these address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways.

WRITE CYCLE 1 waveform on page 4 shows a write cycle terminated by $\overline{W}$ going high. D_{IN} set-up and hold times are referenced to the rising edge of $\overline{W}$. With $\overline{W}$ high, the outputs become active. When $\overline{W}$ goes high at the end of a write cycle and the outputs of the memory go active, the data from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform on page 5 shows a write cycle terminated by $\overline{E}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{E}$. With $\overline{E}$ high, the outputs remain in the high impedance state.

APPLICATION

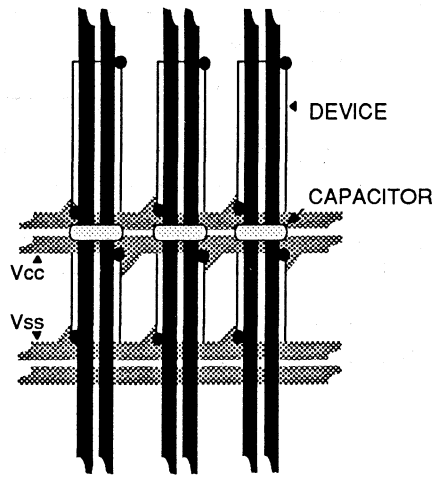
Fundamental rules in regard to memory board layout should be followed to ensure maximum benefit from the features offered by the IMS1420M Static RAM.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1420M. The impedance in the decoupling path from the power pin (20) through the decoupling capacitor, to the ground pin (10) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1420M are high frequency, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor acts as a low impedance power supply located near the memory device. The high frequency decoupling capacitor should have a value of 0.1μF, and be placed between the rows of memory devices in the array (see drawing). A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

The ground grid of the memory array should extend to the TTL driver periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs, are some of the most important, yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1420M	55ns	CERAMIC DIP	IMS1420S-55M
	55ns	CERAMIC LCC	IMS1420N-55M
	70ns	CERAMIC DIP	IMS1420S-70M
	70ns	CERAMIC LCC	IMS1420N-70M

IMS1423M
CMOS
High Performance
4K x 4 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55° C to + 125° C)
- 4K x 4 Bit Organization
- 35, 45, and 55 nsec Access Times
- Single +5V ± 10% Operation
- Power Down Function for Low Standby Power
- Fully TTL Compatible
- Common Data Input and Output
- Three-state Output
- Standard Military Drawing version available (refer to page B-7)
- 20-Pin DIP, LCC (JEDEC Std.) and FP
- Pin Compatible with IMS1420M

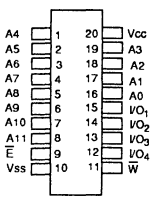
DESCRIPTION

The INMOS IMS1423M is a high speed 4K x 4 CMOS static RAM processed in full compliance to MIL-STD-883C. The IMS1423M provides maximum density and performance enhancements to existing 16K applications.

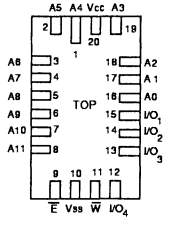
The IMS1423M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1423M is a VLSI static RAM intended for military applications that demand high performance and superior reliability.

PIN CONFIGURATION

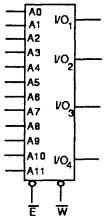


DIP and FLAT PACK

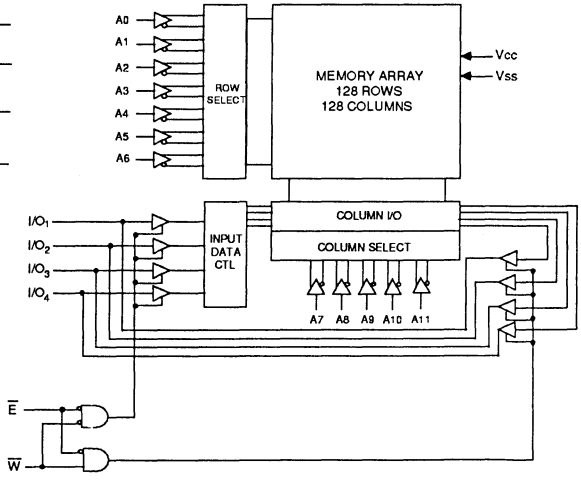


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{11}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5)V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		130 120 110	mA mA mA	t_{AVAV} = 35ns t_{AVAV} = 45ns t_{AVAV} = 55ns
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		20	mA	$\overline{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		8	mA	$\overline{E} \geq (V_{CC} - 0.2)$. All other inputs at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		15 14 13	mA mA mA	t_{AVAV} = 35ns t_{AVAV} = 45ns t_{AVAV} = 55ns $\overline{E} \geq (V_{CC} - 0.2)$. all other iInputs cycling at $V_{IN} \leq 0.2$ or $\geq (V_{CC} - 0.2V)$
I_{ILK}	Input Leakage Current (Any Input)		±10	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±50	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V
C_E	/E Capacitance	6	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

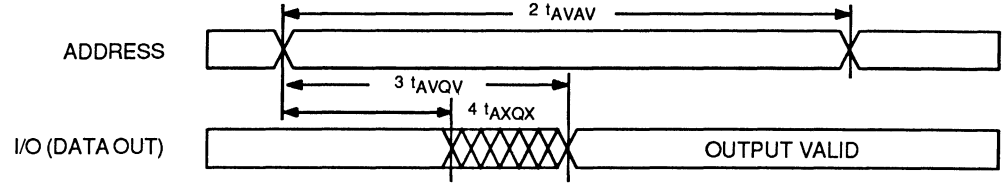
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

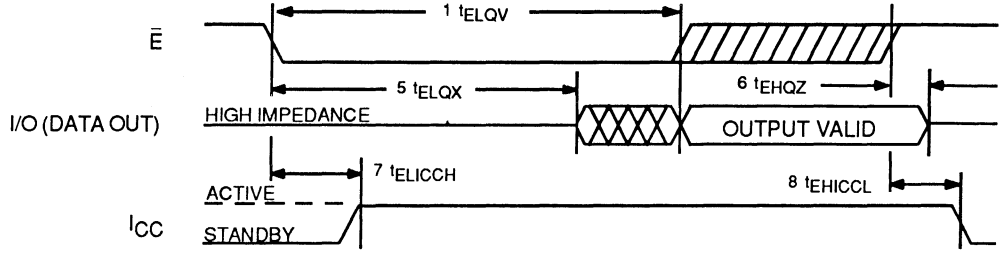
NO.	SYMBOL		PARAMETER	IMS1423M-35		IMS1423M-45		IMS1423M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		35		45		55	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	35		45		55		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		35		45		55	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	3		3		3		ns	j
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	20	0	20	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		35		45		55	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1 [c, d]



READ CYCLE 2 [c]



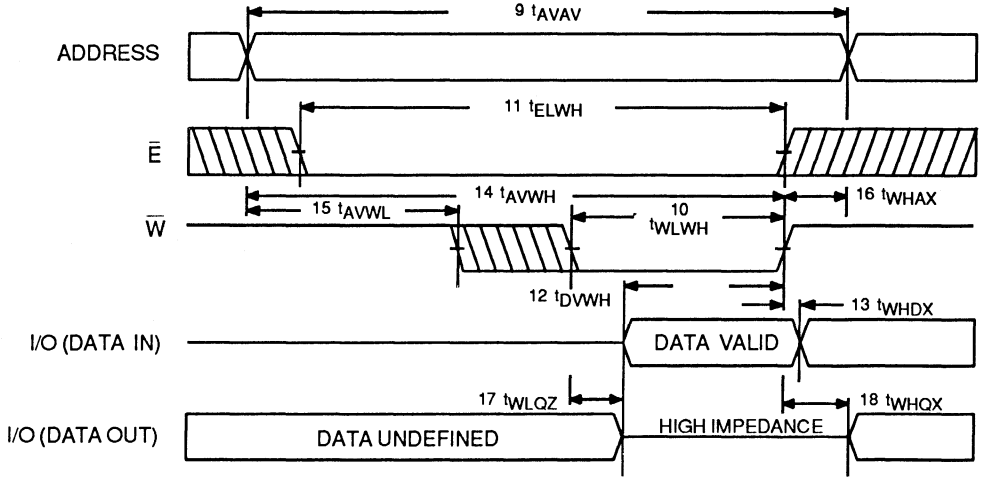
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1403M-35		IMS1403M-45		IMS1403M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	t_{AVAV}	t_{WC}	Write Cycle Time	35		45		55		ns	
10	t_{WLWH}	t_{WP}	Write Pulse Width	30		40		50		ns	
11	t_{ELWH}	t_{CW}	Chip Enable to End of Write	30		40		50		ns	
12	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
13	t_{WHDX}	t_{DH}	Data Hold After End of Write	3		3		3		ns	
14	t_{AVWH}	t_{AW}	Address Set-up to End of Write	30		40		50		ns	
15	t_{AVWL}	t_{AS}	Address Set-up to Beginning of Write	0		0		0		ns	
16	t_{WHAX}	t_{WR}	Address Hold After End of Write	5		5		5		ns	
17	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	15	0	20	0	25	ns	f, j
18	t_{WHQX}	t_{OW}	Output Active After End of Write	5		5		5			i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



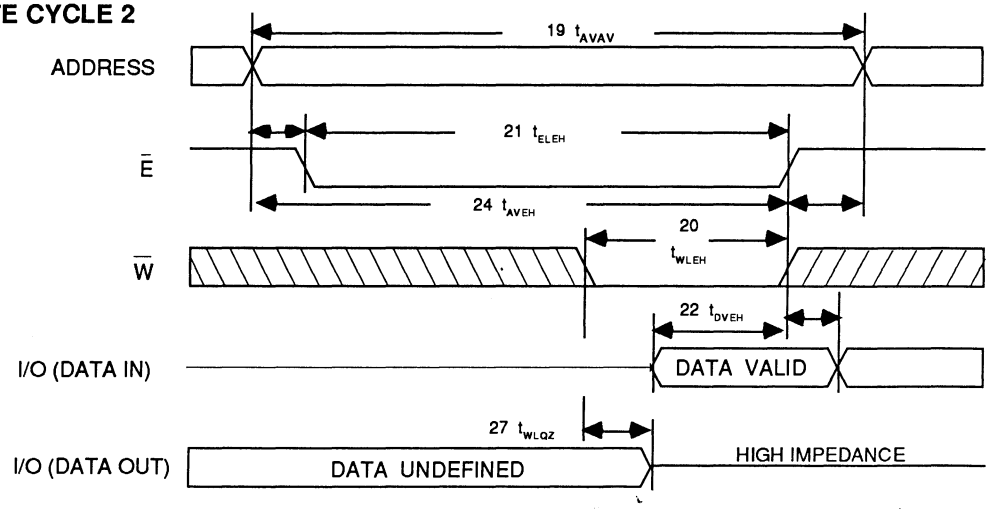
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ TA ≤ 125°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

No	SYMBOL		PARAMETER	IMS 1423M-35		IMS 1423M-45		IMS 1423M-55		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	tAVAV	tWC	Write Cycle Time	35		45		55		ns	
20	tWLEH	tWP	Write Pulse Width	30		40		50		ns	
21	tELEH	tCW	Chip Enable to End of Write	30		40		50		ns	
22	tDVEH	tDW	Data Setup to End of Write	15		20		25		ns	
23	tEHDX	tDH	Data Hold after End of Write	3		3		3		ns	
24	tAVEH	tAW	Address Setup to End of Write	30		40		50		ns	
25	tEHAX	tWR	Address Hold After End of Write	5		5		5		ns	
26	tAVEL	tAS	Address Setup to Beginning of Write	3		3		3		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f,j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between VIH to VIL or VIL to VIH in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ VIH during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1423M has two control inputs, Chip Enable (/E) and Write Enable (/W), 12 address inputs (A0 -A11), and four Data I/O lines. The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 12 address inputs are decoded to select one four-bit word out of 4K words. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq V_{IH}$ min with /E $\leq V_{IL}$ max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1423M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of /W. During this interval, it is possible to have bus contention between devices with common I/O configurations. To avoid bus contention, input data should not be active until t_{WLQZ}.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the outputs of the memory become active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1423M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Since the current transients associated with the operation of the high speed IMS1423M have very high frequency components, the line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad, and be placed between each row of devices in the array (see drawing). A larger tantalum capacitor, with a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

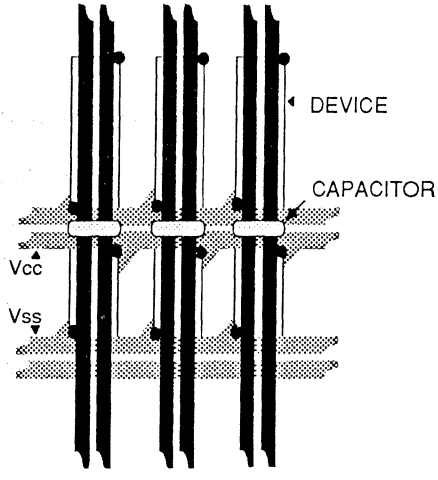
The ground grid of the memory array should extend to the TTL periphery circuit. This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

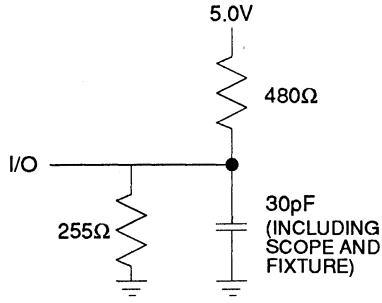
The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.



V_{CC}, V_{SS} GRID SHOWING DECOUPLING CAPACITORS

FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	Din	Write

Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 1423M	35ns	CERAMIC DIP	IMS1423S-35M
	35ns	CERAMIC LCC	IMS1423N-35M
	35ns	FLAT PACK	IMS1423Y-35M
	45ns	CERAMIC DIP	IMS1423S-45M
	45ns	CERAMIC LCC	IMS1423N-45M
	45ns	FLAT PACK	IMS1423Y-45M
	55ns	CERAMIC DIP	IMS1423S-55M
	55ns	CERAMIC LCC	IMS1423N-55M
	55ns	FLAT PACK	IMS1423Y-55M

IMS1600M
IMS1601LM
CMOS
High Performance
64K x 1 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Full Military Temperature Operating Range (-55°C to +125°C)
- MIL-STD-883C Processing
- 45, 55, and 70 nsec Access Times
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- Standard Military Drawing version available (refer to page B-7)
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- Battery Backup Operation - 2V Data Retention (L version only)

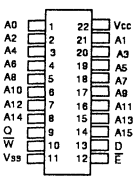
DESCRIPTION

The INMOS IMS1600M is a high performance 64Kx1 CMOS Static RAM processed in full compliance to MIL-STD-883C and guaranteed to operate over the full military temperature range. The IMS1600M provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

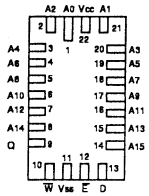
The IMS1600M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

The IMS1601LM is a low power version offering battery backup data retention operating from a 2 volt supply.

PIN CONFIGURATION

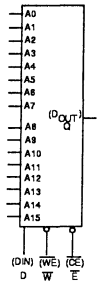


DIP

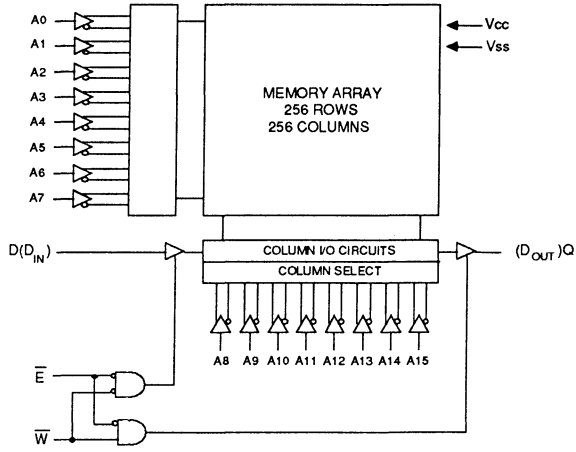


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Q	DATA OUTPUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on Q.....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3 V for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		70	mA	$t_{AVAV} = t_{AVAV}$(min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		25	mA	$\overline{E} \geq V_{IH}$. All other inputs at $V_{IN} \leq V_{IL}$ or $\geq V_{IH}$
	IMS1601L version		20		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		14	mA	$\overline{E} \geq$ (Vcc - 0.2) . All other inputs at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
	IMS1601L version		9		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		19	mA	$\overline{E} \geq$ (Vcc - 0.2) . Inputs cycling at $V_{IN} \leq$ 0.2 or $\geq$ (Vcc - 0.2V)
	IMS1601L version		15		
I_{ILK}	Input Leakage Current (Any Input)		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE (T_A=25°C, f=1.0MHZ)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

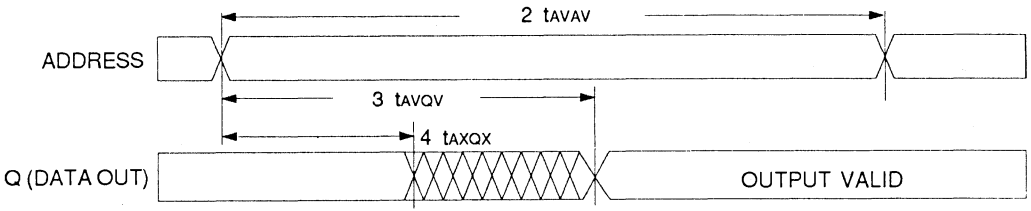
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE [g]

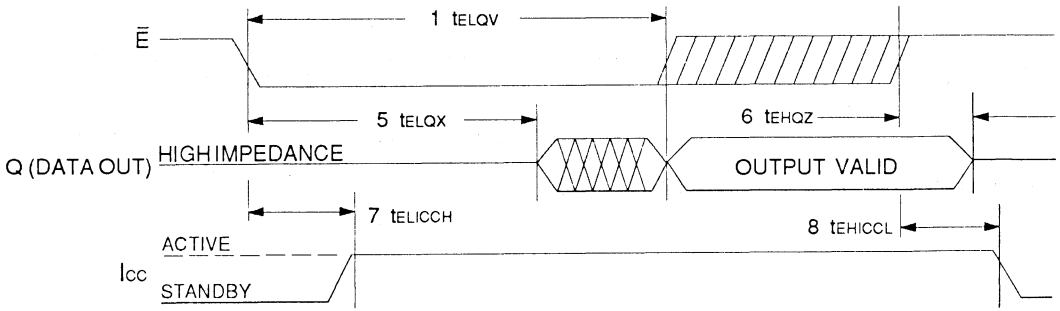
NO.	SYMBOL		PARAMETER	IMS1600M-45		IMS1600M-55		IMS1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	25	0	30	0	30	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		45		55		70	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



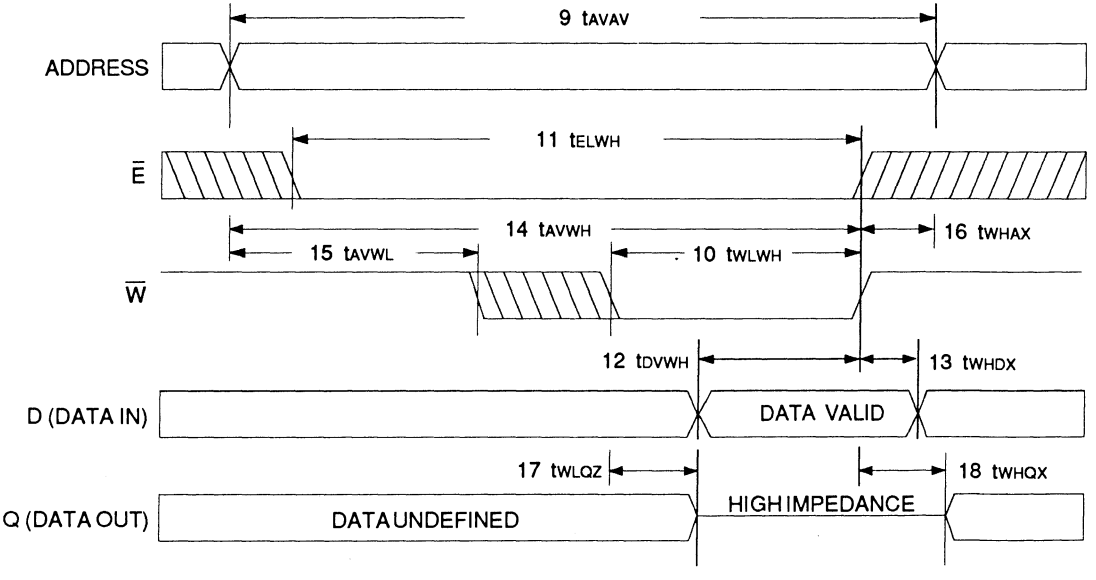
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1600M-45		IMS1600M-55		IMS1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	tAVAV	tWC	Write Cycle Time	45		55		70		ns	
10	tWLWH	tWP	Write Pulse Width	20		25		30		ns	
11	tELWH	tCW	Chip Enable to End of Write	20		30		35		ns	
12	tDVWH	tDW	Data Setup to End of Write	20		20		30		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		5		5		ns	
14	tAVWH	tAW	Address Setup to End of Write	27		32		37		ns	
15	tAVWL	tAS	Address Setup to Start of Write	7		7		7		ns	
16	tWHAX	tWR	Address Hold after End of Write	5		5		5		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	20	0	25	0	30	ns	f, j
18	tWHQX	tOW	Output Active after End of Write	0		0		0		ns	i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



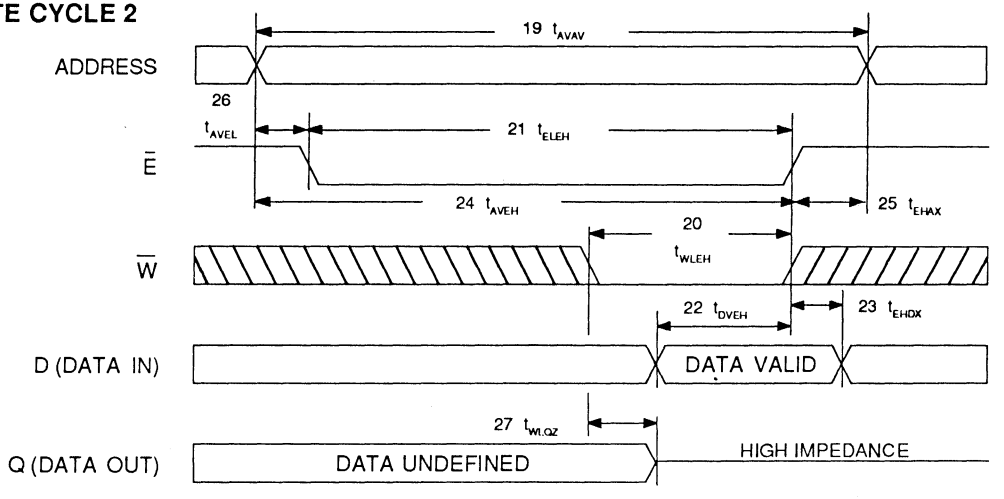
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ T_A ≤ +125°C) (V_{CC} = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1600M-45		IMS1600M-55		IMS1600M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
20	t_{WLEH}	t_{WP}	Write Pulse Width	20		25		30		ns	
21	t_{ELEH}	t_{CW}	Chip Enable to End of Write	20		25		30		ns	
22	t_{DVEH}	t_{DW}	Data Setup to End of Write	20		20		30		ns	
23	t_{EHDX}	t_{DH}	Data Hold after End of Write	5		5		5		ns	
24	t_{AVEH}	t_{AW}	Address Setup to End of Write	23		28		33		ns	
25	t_{EHAX}	t_{WR}	Address Hold after End of Write	5		5		5		ns	
26	t_{AVEL}	t_{AS}	Address Setup to Start of Write	3		3		3		ns	
27	t_{WLQZ}	t_{WZ}	Write Enable to Output Disable	0	20	0	25	0	30	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the output remains in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1600M has two control inputs, a Chip Enable (/E) and Write Enable (/W), 16 address inputs (A0 -A15), a data in (D) and a data out (Q).

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 16 address inputs are decoded to select one memory cell out of 65,536. Read and Write operations on the memory cell are controlled by the /W input. With /E high, the device is deselected, the output is disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the output at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1600M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffer will be turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffer is then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with D and Q connected together in a common I/O configuration. To aviod bus contention input data should not be active until t_{WLQZ}.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the output remains in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1600M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

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Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

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Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) (-55°C ≤ T_A ≤ 125°C)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		8	1200	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		5	800	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION

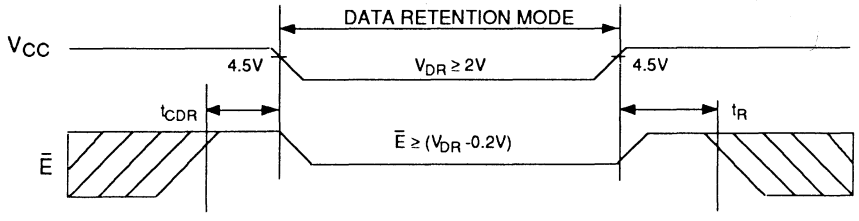
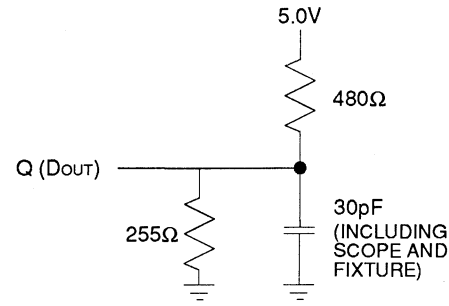


FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1600M IMS1600LM	45ns	CERAMIC DIP	IMS1600S-45M	IMS1601LS45M
	45ns	CERAMIC LCC	IMS1600N-45M	IMS1601LN45M
	55ns	CERAMIC DIP	IMS1600S-55M	IMS1601LS55M
	55ns	CERAMIC LCC	IMS1600N-55M	IMS1601LN55M
	70ns	CERAMIC DIP	IMS1600S-70M	IMS1601LS70M
	70ns	CERAMIC LCC	IMS1600N-70M	IMS1601LN70M

IMS1620M
IMS1620LM
CMOS
High Performance
16K x 4 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Full Military Temperature Operating Range (-55°C to + 125°C)
- MIL-STD-883C Processing
- 16K x 4 Bit Organization
- 45, 55 and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 22-Pin, 300-mil DIP (JEDEC Std.)
- 22-Pin Ceramic LCC (JEDEC Std.)
- Battery Backup Operation - 2V Data Retention (L version only)

DESCRIPTION

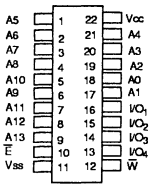
The INMOS IMS1620M is a high performance 16Kx4 CMOS Static RAM processed in full compliance to MIL-STD-883C and guaranteed to operate over the full military temperature range. The IMS1620M provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1620M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1620M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode.

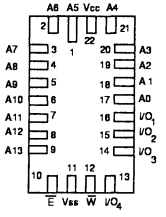
The IMS1620LM is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1624M is the functional equivalent of the IMS1620M with an added Output Enable function.

PIN CONFIGURATION

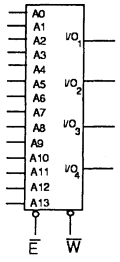


DIP

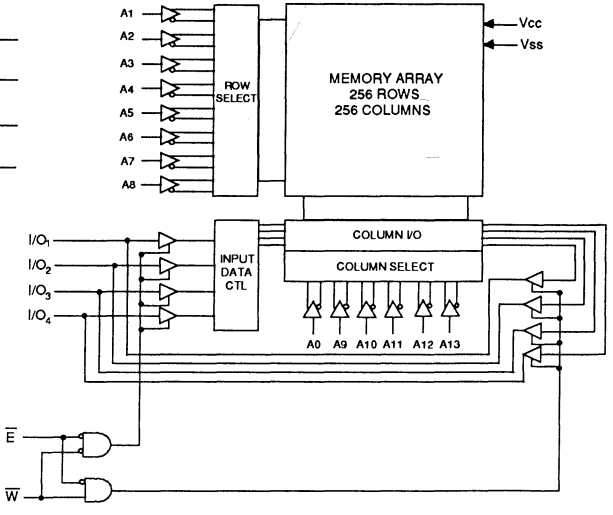


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13} ADDRESS INPUTS	I/O DATA IN/OUT
$\overline{W}$ WRITE ENABLE	Vcc POWER
$\overline{E}$ CHIP ENABLE	Vss GROUND

IMS1620/IMS1620LM

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O Pins (13-16).....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

(One output at a time, one second duration)

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	0	25	70	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		100	mA	t_{AVAV} = t_{AVAV} (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\overline{E}$ ≥ V_{IH}. All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
	IMS1620L version		20		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		19	mA	$\overline{E}$ ≥ (Vcc - 0.2). All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1620L version		8		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		20	mA	$\overline{E}$ ≥ (Vcc - 0.2). Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1620L version		8		
I_{ILK}	Input Leakage Current (Any Input)		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

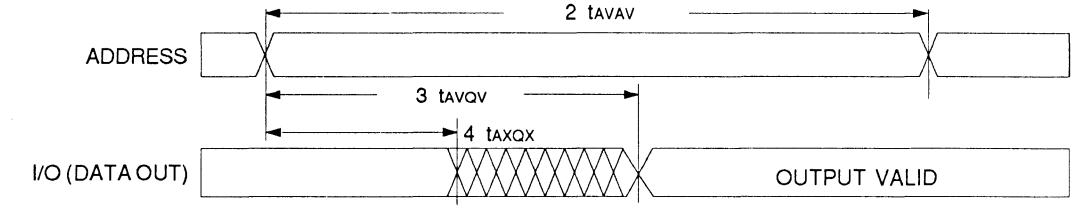
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

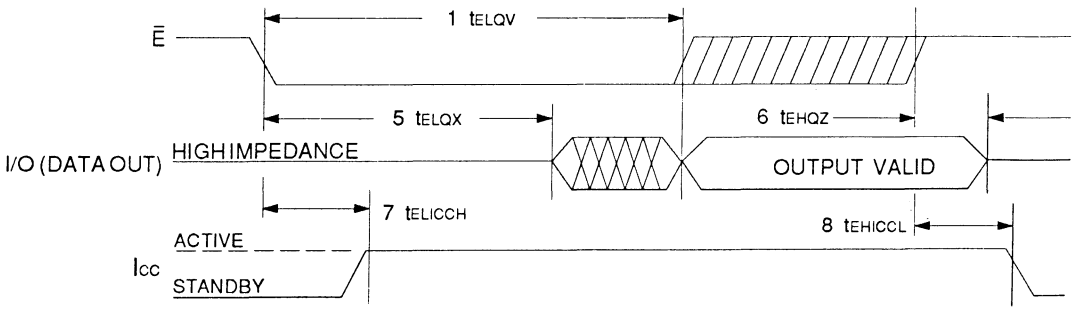
NO.	SYMBOL		PARAMETER	IMS1620M-45		IMS1620M-55		IMS1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	d
4	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
5	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
6	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	25	ns	f, j
7	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
8	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		45		55		70	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



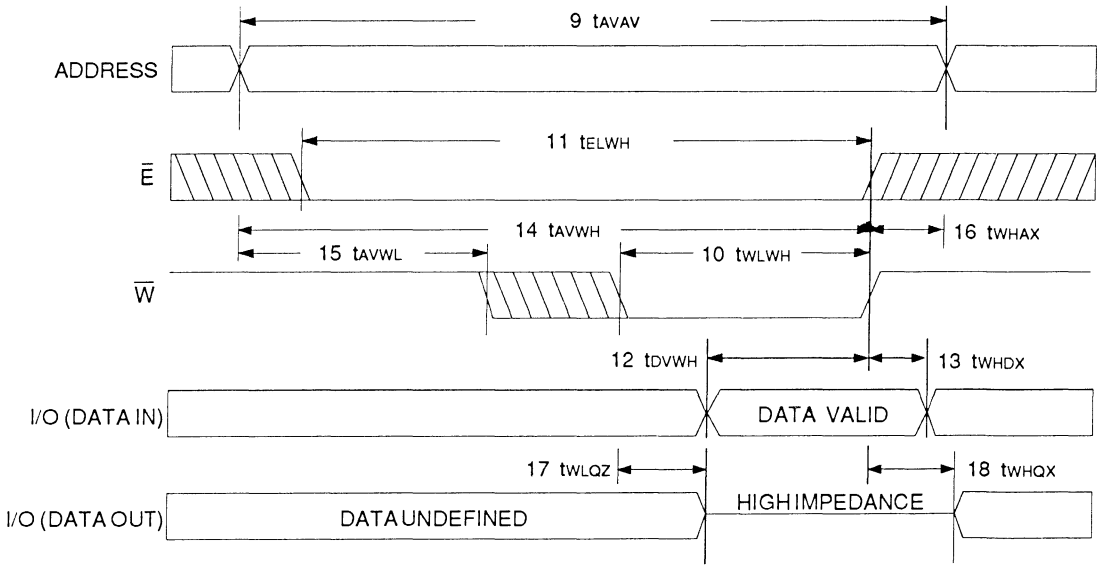
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le +125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

NO.	SYMBOL		PARAMETER	IMS1620M-45		IMS1620M-55		IMS1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
9	tAVAV	tWC	Write Cycle Time	40		50		60		ns	
10	tWLWH	tWP	Write Pulse Width	30		40		50		ns	
11	tELWH	tCW	Chip Enable to End of Write	30		40		50		ns	
12	tDVWH	tDW	Data Setup to End of Write	20		25		30		ns	
13	tWHDX	tDH	Data Hold after End of Write	0		0		0		ns	
14	tAVWH	tAW	Address Setup to End of Write	30		40		50		ns	
15	tAVWL	tAS	Address Setup to Start of Write	0		0		0		ns	
16	tWHAX	tWR	Address Hold after End of Write	0		0		0		ns	
17	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f, j
18	tWHQX	tOW	Output Active after End of Write	5		5		5		ns	i, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\ge V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 1



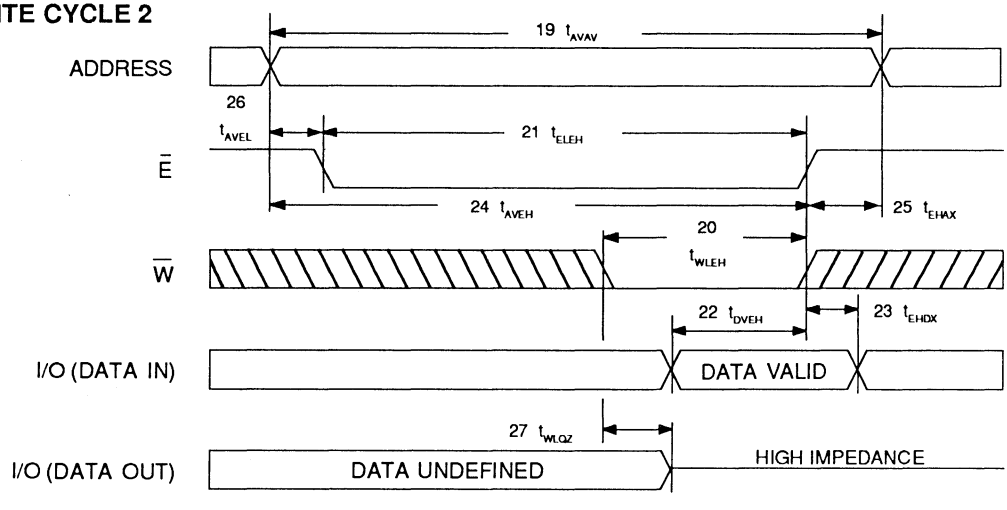
RECOMMENDED AC OPERATING CONDITIONS (-55°C ≤ Ta ≤ 125°C) (Vcc = 5.0V ±10%)

WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g, h]

NO.	SYMBOL		PARAMETER	IMS1620M-45		IMS1620M-55		IMS1620M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
19	tAVAV	tWC	Write Cycle Time	40		50		60		ns	
20	tWLEH	tWP	Write Pulse Width	30		40		50		ns	
21	tELEH	tCW	Chip Enable to End of Write	30		40		50		ns	
22	tDVEH	tDW	Data Setup to End of Write	20		25		30		ns	
23	tEHDX	tDH	Data Hold after End of Write	0		0		0		ns	
24	tAVEH	tAW	Address Setup to End of Write	30		40		50		ns	
25	tEHAX	tWR	Address Hold after End of Write	0		0		0		ns	
26	tAVEL	tAS	Address Setup to Start of Write	0		0		0		ns	
27	tWLQZ	tWZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f, j

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between VIH to VIL or VIL to VIH in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be ≥ VIH during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

WRITE CYCLE 2



DEVICE OPERATION

The IMS1620M has two control inputs, a Chip Enable (/E) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W input. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-third of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W $\geq$ V_{IH} min with /E $\leq$ V_{IL} max. Read access time is measured from either /E going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E is low. The outputs remain active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and long as /E remains low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by /E going low. As long as address is stable when /E goes low, valid data is at the outputs at the specified Chip Enable Access time. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1620M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on t_{ELQX} after the falling edge of /E (just as in a read cycle). The output buffers are then turned off within t_{WLQZ} of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until t_{WLQZ} to aviod bus contention.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active. The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1620M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area This will provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) (-55°C ≤ T_A ≤ 125°C)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		15	1200	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		10	800	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION

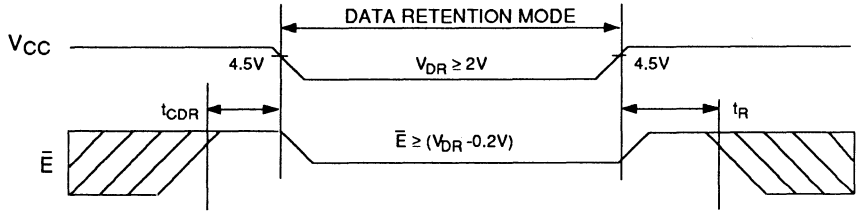
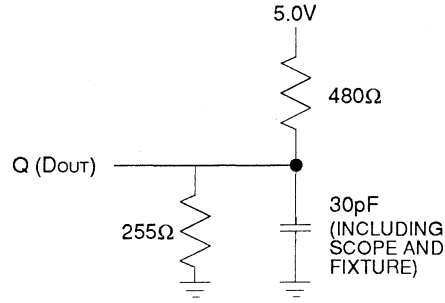


FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	Q	MODE
H	X	HI-Z	Standby (Isb)
L	H	Dout	Read
L	L	HI-Z	Write

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1620M IMS1620LM	45ns	CERAMIC DIP	IMS1620S-45M	IMS1620LS45M
	45ns	CERAMIC LCC	IMS1620N-45M	IMS1620LN45M
	55ns	CERAMIC DIP	IMS1620S-55M	IMS1620LS55M
	55ns	CERAMIC LCC	IMS1620N-55M	IMS1620LN55M
	70ns	CERAMIC DIP	IMS1620S-70M	IMS1620LS70M
	70ns	CERAMIC LCC	IMS1620N-70M	IMS1620LN70M

IMS1624M
IMS1624LM
CMOS
High Performance
16K x 4 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.6 Micron Design Rules
- Full Military Temperature Operating Range (-55°C to +125°C)
- MIL-STD-883C Processing
- 16K x 4 Bit Organization with Output Enable
- 45, 55, and 70 nsec Access Times
- Fully TTL Compatible
- Common Data Input & Output
- Three-state Output
- Power Down Function
- Single +5V ± 10% Operation
- 24-Pin, 300-mil DIP (JEDEC Std.)
- 28-Pin, 300-mil LCC (JEDEC Std.)
- Standard Military Drawing version available (refer to page B-7)
- Battery Backup Operation - 2V Data Retention (L version only)

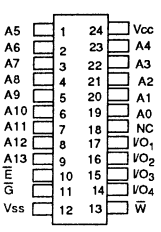
DESCRIPTION

The INMOS IMS1624M is a high performance 16Kx4 CMOS Static RAM processed in full compliance to MIL-STD-883C and guaranteed to operate over the full military temperature range. The IMS1624M provides maximum density and speed enhancements with the additional CMOS benefits of lower power and superior reliability.

The IMS1624M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624M provides a Chip Enable (/E) function that can be used to place the device into a low-power standby mode. The IMS1624M also includes an Output Enable (/G) for fast access to data and enhanced bus contention control.

The IMS1624LM is a low power version offering battery backup data retention operating from a 2 volt supply.

PIN CONFIGURATION



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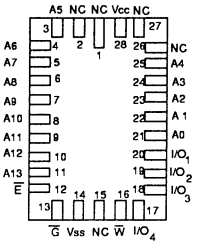
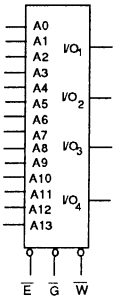
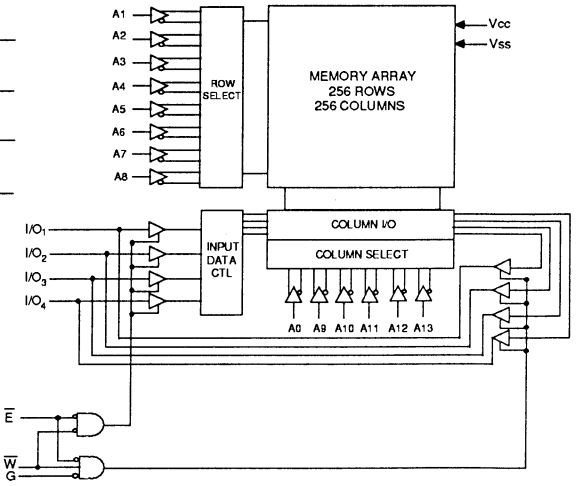


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{13}	ADDRESS INPUTS	Vcc POWER (+5V)
W̄	WRITE ENABLE	Vss GROUND
I/O	DATA IN/OUT	
Ē	CHIP ENABLE	
Ḡ	OUTPUT ENABLE	

IMS1624M/IMS1624LM

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O Pins (13-16).....-1.0 to (Vcc+0.5)
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

(One output at a time, one second duration)

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	55	25	125	°C	400 linear ft/min air flow

*V_{IL} min = -3 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ +125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		100	mA	tAVAV = tAVAV (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\overline{E}$ ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
	IMS1624L version		20		
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		19	mA	$\overline{E}$ ≥ (Vcc - 0.2) . All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1624L version		8		
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		20	mA	$\overline{E}$ ≥ (Vcc - 0.2) . Inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
	IMS1624L version		8		
I_{ILK}	Input Leakage Current (Any Input)		± 5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		± 10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OH} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OL} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels ..... V_{SS} to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels.. 1.5V
Output Load ..... See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0 MHZ)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	4	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

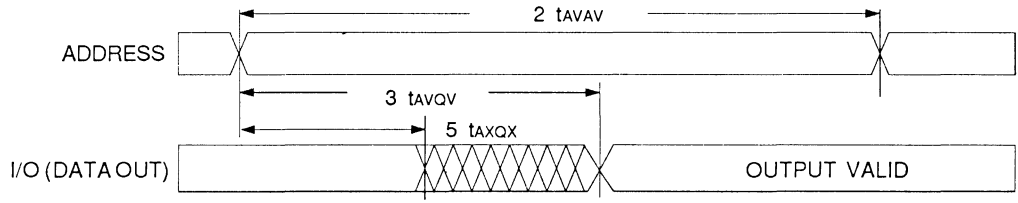
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

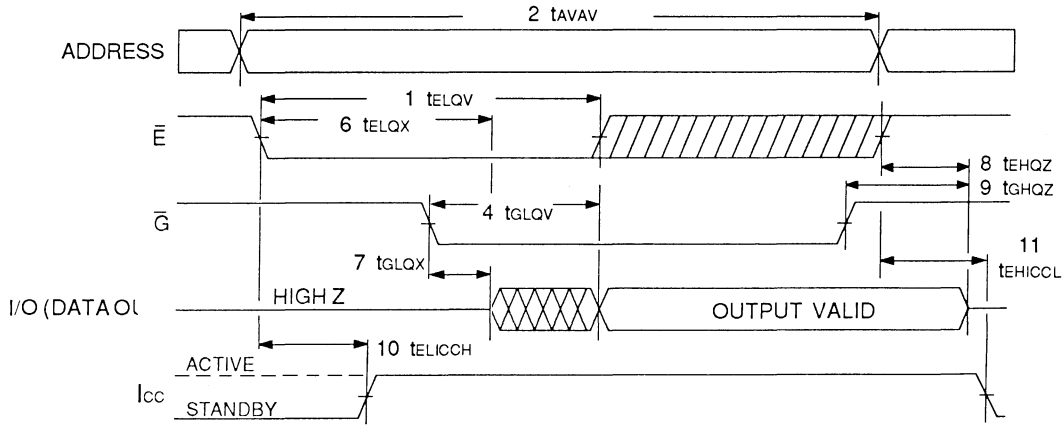
NO.	SYMBOL		PARAMETER	IMS1624M-45		IMS1624M-55		IMS1624M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	c
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	d
4	t_{GLQV}	t_{OE}	Output Enable Access Time		20		25		30	ns	
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	j
7	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	5		5		5		ns	j
8	t_{EHQZ}	t_{HZ}	Chip Disable to Output Inactive	0	15	0	20	0	25	ns	f, j
9	t_{GHQZ}	t_{OHZ}	Output Disable to Output Inactive	0	15	0	20	0	25	ns	f, j
10	t_{ELICCH}	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
11	t_{EHICCL}	t_{PD}	Chip Enable to Power Down		45		55		70	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected; $\overline{E}$ low.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c,d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

	SYMBOL		PARAMETER	IMS 1624-45		IMS 1624-55		IMS 1624-70		UNITS	NOTES
No	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
12	tAVAV	t WC	Write Cycle Time	40		50		60		ns	
13	tWLWH	t WP	Write Pulse Width	30		40		50		ns	
14	tELWH	t CW	Chip Enable to End of Write	30		40		50		ns	
15	tDVWH	t DW	Data Setup to End of Write	20		25		30		ns	
16	tWHDX	t DH	Data Hold after End of Write	0		0		0		ns	
17	tAVWH	t AW	Address Setup to End of Write	30		40		50		ns	
18	tAVWL	t AS	Address Setup to Start of Write	0		0		0		ns	
19	tWHAX	t WR	Address Hold after End of Write	0		0		0		ns	
20	tWLQZ	t WZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f,j
21	tWHQX	t OW	O/P Active after end of Write	0		0		0		ns	i,j

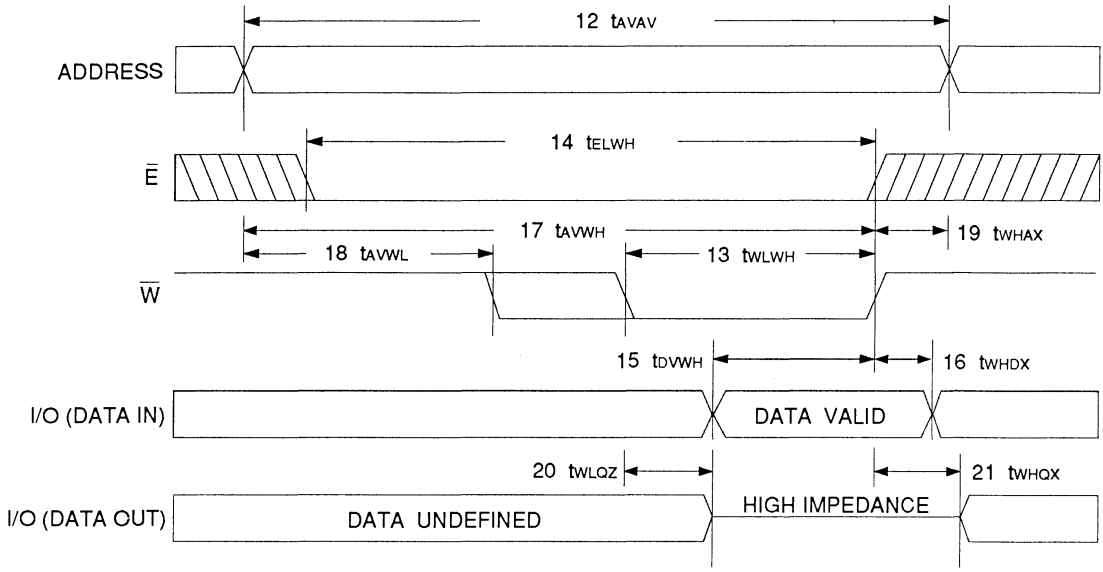
WRITE CYCLE 2: $\overline{E}$ CONTROLLED[g,h]

	SYMBOL		PARAMETER	IMS 1624-45		IMS 1624-55		IMS 1624-70		UNITS	NOTES
No	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
22	tAVAV	t WC	Write Cycle Time	40		50		60		ns	
23	tWLEH	t WP	Write Pulse Width	30		40		50		ns	
24	tELEH	t CW	Chip Enable to End of Write	30		40		50		ns	
25	tDVEH	t DW	Data Setup to End of Write	20		25		30		ns	
26	tEHDX	t DH	Data Hold after End of Write	0		0		0		ns	
27	tAVEH	t AW	Address Setup to End of Write	30		40		50		ns	
28	tEHAX	t WR	Address Hold after End of Write	0		0		0		ns	
29	tAVEL	t AS	Address Setup to Start of Write	0		0		0		ns	
30	tWLQZ	t WZ	Write Enable to Output Disable	0	15	0	20	0	25	ns	f,j

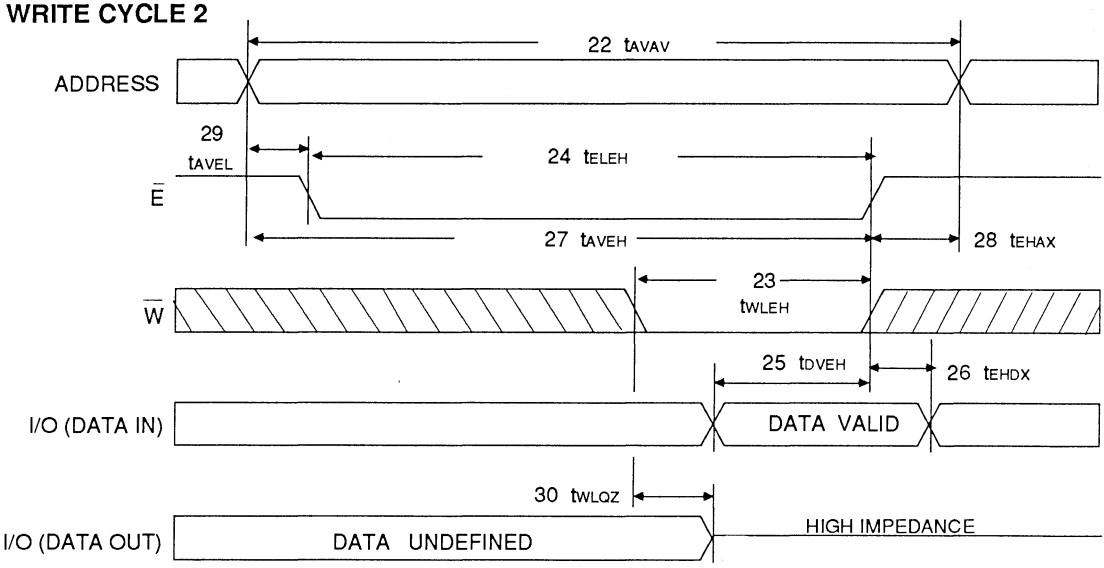
WRITE CYCLE 3: Fast Write, Outputs Disabled[g,h]

	SYMBOL		PARAMETER	IMS 1624-45		IMS 1624-55		IMS 1624-70		UNITS	NOTES
No	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
31	tAVAV	t WC	Write Cycle Time	25		30		35		ns	
32	tWLWH	t WP	Write Pulse Width	20		25		30		ns	
33	tDVWH	t DW	Data Setup to End of Write	20		25		30		ns	
34	tWHDX	t DH	Data Hold after End of Write	0		0		0		ns	
35	tAVWH	t AW	Address Setup to End of Write	20		25		30		ns	
36	tWHAX	t WR	Address Hold after End of Write	5		5		5		ns	
37	tAVWL	t AS	Address Setup to Start of Write	0		0		0		ns	

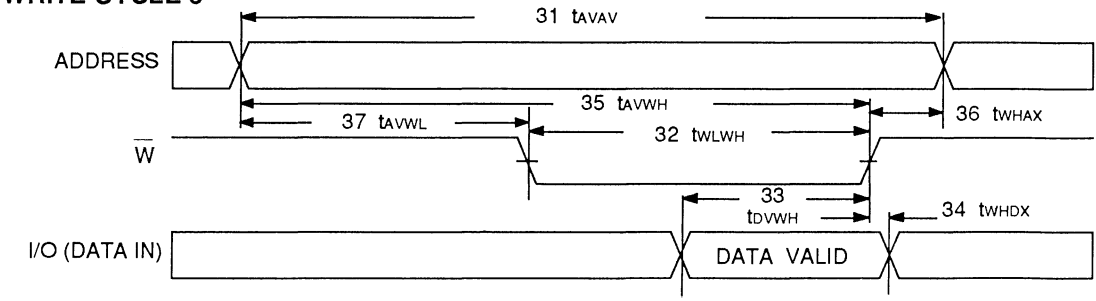
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}$ or $\overline{W}$ must be $\geq V_{IH}$ during address transitions.
Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.



WRITE CYCLE 2



WRITE CYCLE 3



DEVICE OPERATION

The IMS1624M has three control inputs, Chip Enable (/E), Output Enable (/G) and Write Enable (/W), 14 address inputs (A0 -A13), and four Data I/O pins.

The /E input controls device selection as well as active and standby modes. With /E low, the device is selected and the 14 address inputs are decoded to select one 4-bit word out of 16,384. Read and Write operations on the memory cells are controlled by the /W and /G inputs. With /E high, the device is deselected, the outputs are disabled and the power consumption is reduced to less than one-fourth of the active mode power with TTL levels and even lower with CMOS levels.

READ CYCLE

A read cycle is defined as /W ≥ VIHmin with /E and /G ≤ VILmax. Read access time is measured from the latter of either /E or /G going low or from valid address.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while /E and /G are low. The outputs remain active throughout READ CYCLE 1 and are valid at the specified address access time. The address inputs may change at access time and long as /E and /G remain low, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated bythe latter of /E or /G going low. As long as address is stable when /E goes low, valid data is at the outputs at thelatter of specified Chip Enable Access or Output Enable Access times. If address is not valid when /E goes low, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

WRITE CYCLE

The write cycle of the IMS1624M is initiated by the latter of /E or /W to transition from a high to a low. In the case of /W falling last, the output buffers are turned on tELQX after the falling edge of /E if /G is already low (just as in a read cycle). The output buffers are then turned off within tWLQZ of the falling edge of /W. During this interval it is possible to have bus contention between devices with common I/O configurations. Therefore input data should not be active until tWLQZ. To aviod bus contention, the /G input can be held high throughout the write operation.

WRITE CYCLE 1 waveform shows a write cycle terminated by /W going high. Data set-up and hold times are referenced to the rising edge of /W. When /W goes high at the end of the cycle with /E active, the output of the memory becomes active (if /G is low). The data from the memory will be the same as the input data unless the input data or address changes.

WRITE CYCLE 2 waveform shows a write cycle terminated by /E going high. Data set-up and hold times are referenced to the rising edge of /E. With /E high the outputs remain in the high impedance state.

WRITE CYCLE 3 waveform shows a write cycle controlled by /W, with /G high and /E low throughout the cycle. As the outputs will not become active during this operation, maximum data bandwidth is provided by allowing very short write cycles and eliminating any bus contention considerations.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1624M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 microfarad and be placed between each row of devices in the array. A larger capacitor to eliminate low frequency ripple should be placed near the edge connection where the power traces meet the backplane power. The larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area to provide a solid ground reference for the TTL drivers and prevent loss of operating margin of the drivers due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically.

DATA RETENTION (L version only) ($-55°C \le T_A \le 125°C$)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	$V_{IN} \le 0.2V$ or $\ge (V_{CC}-0.2V)$ $\overline{E} \ge (V_{CC}-0.2V)$
I_{CCDR1}	Data Retention Current		15	1200	µA	V_{CC}= 3.0 volts
I_{CCDR2}	Data Retention Current		10	800	µA	V_{CC}= 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j, k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j, k (t_{RC}= Read Cycle Time)

*Typical data retention parameters at 25°C.
Note j: Parameter guaranteed but not tested.
Note k: Supply recovery rate should not exceed 100mV per µS from V_{DR} to V_{CC} min.

LOW V_{CC} DATA RETENTION

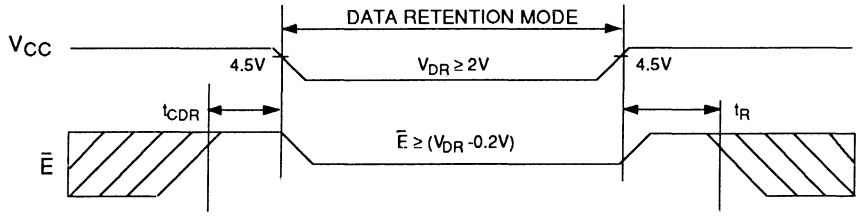
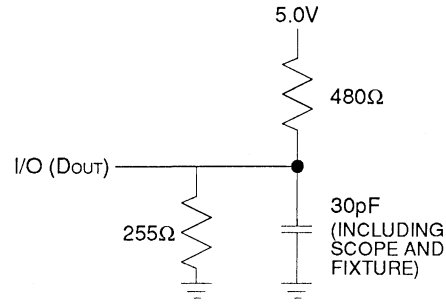


FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	I/O	MODE
H	X	X	HI-Z	Standby (Isb)
L	H	H	HI-Z	Output Disable
L	H	L	Dout	Read
L	L	X	Din	Write

Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1624M IMS1624LM	45ns	CERAMIC DIP	IMS1624S-45M	IMS1624LS45M
	45ns	CERAMIC LCC	IMS1624N-45M	IMS1624LN45M
	55ns	CERAMIC DIP	IMS1624S-55M	IMS1624LS55M
	55ns	CERAMIC LCC	IMS1624N-55M	IMS1624LN55M
	70ns	CERAMIC DIP	IMS1624S-70M	IMS1624LS70M
	70ns	CERAMIC LCC	IMS1624N-70M	IMS1624LN70M

IMS1630M
IMS1630LM
CMOS
High Performance
8K x 8 Static RAM
MIL-STD-883C

FEATURES

- INMOS' Very High Speed CMOS
- Military Temperature Range (-55°C to 125°C)
- Advanced Process - 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- 45, 55 and 70 ns Address Access Times
- 45, 55 and 70 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Inputs and Outputs
- Single +5V ± 10% Operation
- Fast Write Cycle when Outputs Disabled
- Standard Military Drawing version available
- 28 pin DIP, 32 pin LCC (JEDEC Standard)
- Battery Backup Operation - 2V data retention (L version only)

DESCRIPTION

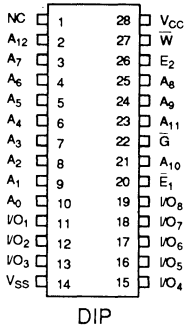
The IMS1630M is a high speed CMOS 8K x 8 Static RAM processed in full compliance to MIL-STD-883C.

The IMS1630M features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1630M provides two Chip Enable functions (/E1, E2) to place the circuit in a reduced power standby mode.

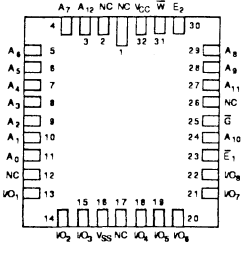
The IMS1630LM is a low power version offering battery backup data retention operating from a 2 volt supply.

The IMS1630M and IMS1630LM are VLSI Static RAMs intended for military applications that demand high performance and superior reliability.

PIN CONFIGURATION

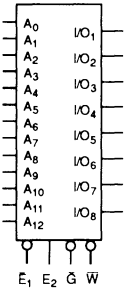


DIP

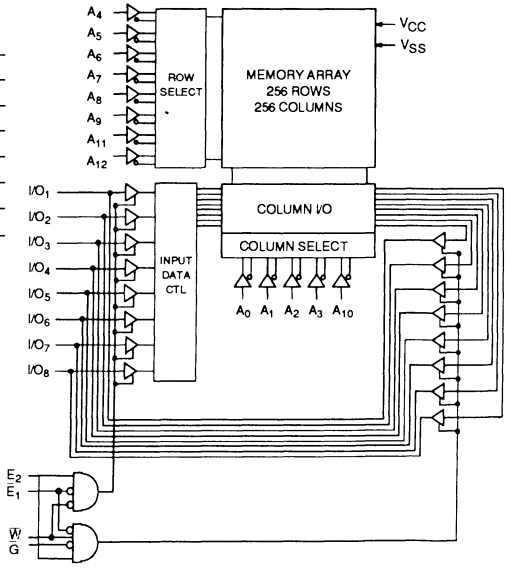


LCC

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_{12}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O_1-I/O_8	DATA IN/OUT		
$\overline{E}_1$, E_2	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to Vss.....-2.0 to 7.0V
Voltage on I/O.....-1.0 to (Vcc+0.5)V
Temperature Under Bias.....-55° C to 125°C
Storage Temperature .....-65° C to 150°C
Power Dissipation.....1W
DC Output Current.....25mA
(One output at a time, one second duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage	0	0	0	V	
V_{IH}	Input Logic "1" Voltage	2.0		Vcc+0.5	V	All inputs
V_{IL}	Input Logic "0" Voltage	-1.0*		0.8	V	All inputs
T_A	Ambient Operating Temperature	-55		+125	°C	400 linear ft/min air flow

*V_{IL} min = -3.0 volts for pulse width <20ns, note b.

DC ELECTRICAL CHARACTERISTICS (-55°C ≤ T_A ≤ 125°C) (V_{CC} = 5.0V ± 10%)[a]

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC1}	Average Vcc Power Supply Current		85	mA	tAVAV = tAVAV (min)
I_{CC2}	Vcc Power Supply Current (Standby,Stable TTL Input Levels)		30	mA	$\bar{E}$ ≥ V_{IH} . All other inputs at V_{IN} ≤ V_{IL} or ≥ V_{IH}
I_{CC3}	Vcc Power Supply Current (Standby, Stable CMOS Input Levels)		17	mA	$\bar{E}$ ≥ (Vcc - 0.2) . All other inputs at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{CC4}	Vcc Power Supply Current (Standby, Cycling CMOS Input Levels)		20	mA	$\bar{E}$ ≥ (Vcc - 0.2). All other inputs cycling at V_{IN} ≤ 0.2 or ≥ (Vcc - 0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±5	µA	Vcc = max V_{IN} = Vss to Vcc
I_{OLK}	Off State Output Leakage Current		±10	µA	Vcc = max V_{IN} = Vss to Vcc
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT} = -4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT} = 8mA

Note a: Icc is dependent on output loading and cycle rate, the specified values are obtained with the output unloaded.

AC TEST CONDITIONS

Input Pulse Levels .....Vss to 3V
Input Rise and Fall Times 5ns
Input and Output Timing Reference Levels..1.5V
Output Load .....See Figure 1

CAPACITANCE[b] (T_A=25°C, f=1.0MHz)[b]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note b: This parameter is sampled and not 100% tested.

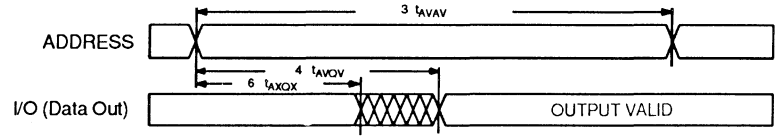
RECOMMENDED AC OPERATING CONDITIONS ($-55°C \le T_A \le 125°C$)($V_{CC} = 5.0V \pm 10\%$)

READ CYCLE[g]

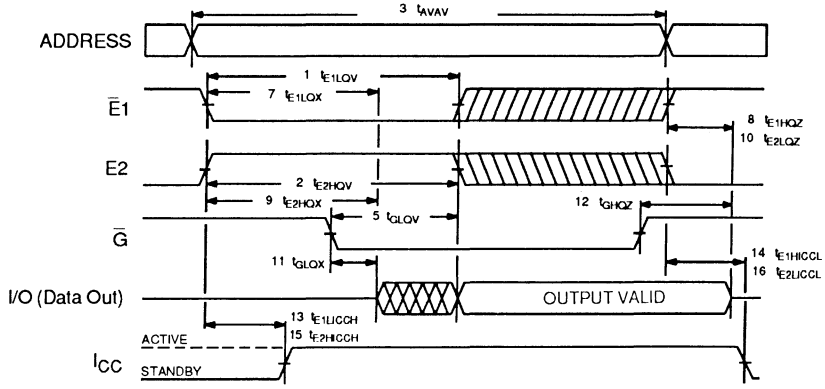
NO.	SYMBOL		PARAMETER	1630M-45		1630M-55		1630M-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{E1LQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{E2HQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
3	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	c
4	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	d
5	t_{GLQV}	t_{OE}	Output Enable to Data Valid		15		20		25	ns	
6	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
7	t_{E1LQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
8	t_{E1HQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	25	0	25	ns	f, j
9	t_{E2HQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
10	t_{E2LQZ}	t_{HZ}	Chip Disable to Output Inactive	0	20	0	25	0	25	ns	f, j
11	t_{GLQX}	t_{LZ}	Output Enable to Output Active	5		5		5		ns	
12	t_{GHQZ}	t_{HZ}	Output Disable to Output Inactive	0	20	0	25	0	25	ns	f, j
13	$t_{E1LICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
14	$t_{E1HICCL}$	t_{PD}	Chip Enable to Power Down		25		30		35	ns	j
15	$t_{E2HICCH}$	t_{PU}	Chip Enable to Power Up	0		0		0		ns	j
16	$t_{E2LICCL}$	t_{PD}	Chip Disable to Power Down		25		30		35	ns	j
		t_T	Input Rise and Fall Times		50		50		50	ns	e, j

Note c: For READ CYCLE 1 & 2, $\overline{W}$ is high for entire cycle.
Note d: Device is continuously selected, $\overline{E}1$ low, $\overline{G}$ low and E2 high.
Note e: Measured between V_{IL} max and V_{IH} min.
Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note j: Parameter guaranteed but not tested.

READ CYCLE 1[c, d]



READ CYCLE 2[c]



RECOMMENDED AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 125°C$) ($V_{CC} = 5.0V \pm 10\%$)

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[g,h]

No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630M-45 MIN	IMS 1630M-45 MAX	IMS 1630M-55 MIN	IMS 1630M-55 MAX	IMS 1630M-70 MIN	IMS 1630M-70 MAX	UNITS	NOTES
18	tAVAV	t WC	Write Cycle Time	45		55		70		ns	
19	tWLWH	t WP	Write Pulse Width	35		45		50		ns	
20	tE1LWH	t CW	Chip Enable 1 to End of Write	35		45		50		ns	
21	tE2HWH	t CW	Chip Enable 2 to End of Write	35		45		50		ns	
22	tDVWH	t DW	Data Setup to End of Write	20		25		25		ns	
23	tWHDX	t DH	Data Hold after End of Write	0		0		0		ns	
24	tAVWH	t AW	Address Setup to End of Write	35		45		50		ns	
25	tAVWL	t AS	Address Setup to Start of Write	0		0		0		ns	
26	tWHAX	t WR	Address Hold after End of Write	0		0		0		ns	
27	tWLQZ	t WZ	Write Enable to Output Disable	0	20	0	20	0	25	ns	f,j
28	tWHQX	t OW	Output Active After End of Write	5		5		5		ns	i,j

WRITE CYCLE 2: E1 OR E2 CONTROLLED[g,h]

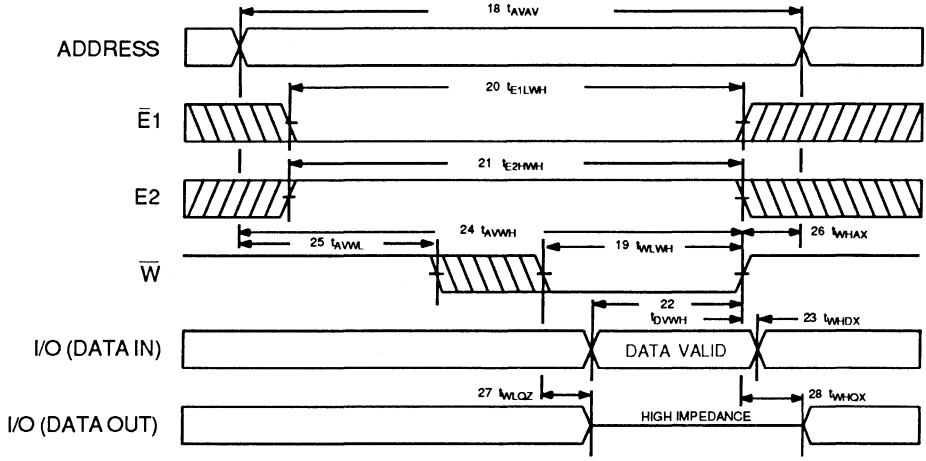
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630M-45 MIN	IMS 1630M-45 MAX	IMS 1630M-55 MIN	IMS 1630M-55 MAX	IMS 1630M-70 MIN	IMS 1630M-70 MAX	UNITS	NOTES
29	tAVAV	t WC	Write Cycle Time	45		55		70		ns	
30	tWLE1H	t WP	Write Pulse Width	35		45		50		ns	
31	tE1LE1H	t CW	Chip Enable 1 to End of Write	35		45		50		ns	
32	tE2HE2L	t CW	Chip Enable 2 to End of Write	35		45		50		ns	
33	tDVE1H	t DW	Data Setup to End of Write	20		25		25		ns	
34	tE1HDX	t DH	Data Hold after End of Write	0		0		0		ns	
35	tAVE1H	t AW	Address Setup to End of Write	35		45		50		ns	
36	tE1HAX	t WR	Address Hold after End of Write	0		0		0		ns	
37	tAVE1L	t AS	Address Setup to Start of Write	0		0		0		ns	
38	tWLQZ	t WZ	Write Enable to Output Disable	0	20	0	20	0	25	ns	f,j

WRITE CYCLE 3: FAST WRITE, OUTPUTS DISABLED (DEVICE CONTINUOUSLY SELECTED, $\overline{G}$ HIGH)[g,h]

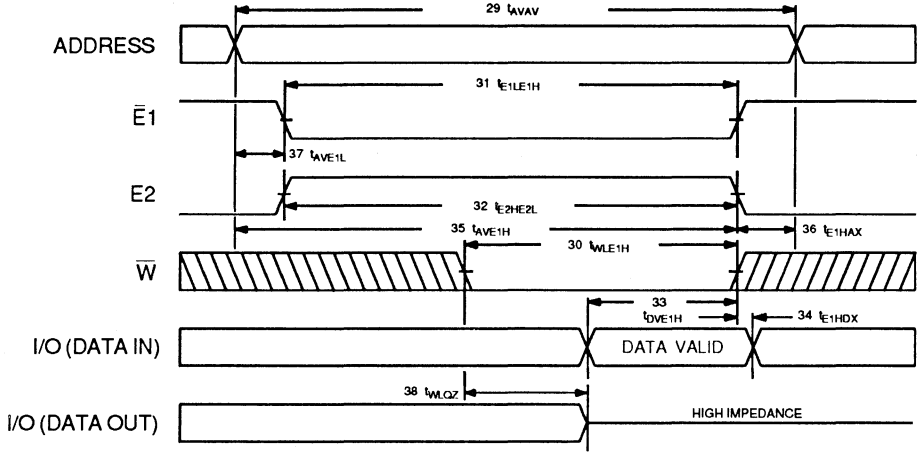
No	SYMBOL Stan'd	SYMBOL Alt.	PARAMETER	IMS 1630M-45 MIN	IMS 1630M-45 MAX	IMS 1630M-55 MIN	IMS 1630M-55 MAX	IMS 1630M-70 MIN	IMS 1630M-70 MAX	UNITS	NOTES
39	tAVAV	t WC	Write Cycle Time	25		30		35		ns	
40	tWLWH	t WP	Write Pulse Width	20		25		30		ns	
41	tDVWH	t CW	Data Set-up to End of Write	20		25		30		ns	
42	tWHDX	t CW	Data Hold After End of Write	0		0		0		ns	
43	tAVWH	t DW	Address Set-up to End of Write	20		25		30		ns	
44	tWHAX	t DH	Addres Hold After End of Write	0		0		0		ns	
45	tAVWL	t AS	Address Set-up to Start of Write	0		0		0		ns	

Note f: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note g: $\overline{E}1$, E2, $\overline{G}$ and $\overline{W}$ must transition between V_{IH} to V_{IL} or V_{IL} to V_{IH} in a monotonic fashion.
Note h: $\overline{E}1$, or $\overline{W}$ must be $\geq V_{IH}$ or E2 must be $\leq V_{IL}$ during address transitions.
Note i: If $\overline{W}$ is low when the later of $\overline{E}1$ goes low or E2 goes high, the outputs remain in the high impedance state.
Note j: Parameter guaranteed but not tested.

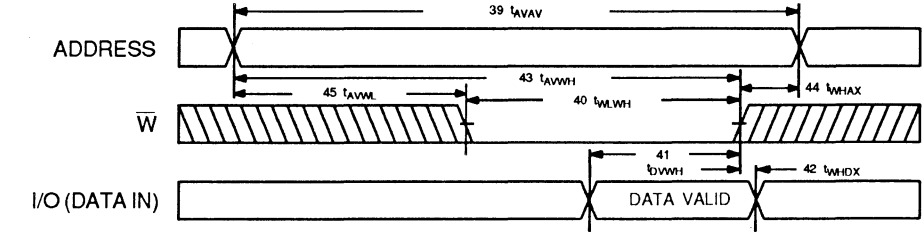
WRITE CYCLE 1



WRITE CYCLE 2



WRITE CYCLE 3



DEVICE OPERATION

The IMS1630M has four control inputs, Chip Enable1 ($\overline{E1}$), Chip Enable 2 (E2), Write Enable ($\overline{W}$) and Output Enable ($\overline{G}$). There are also13 address inputs (A0 -A12) and eight Data I/O lines (I/O 1 to I/O 8). The Enable inputs control device selection as well as active and standby modes. The $\overline{W}$ input controls the mode of operation (Read or Write). The $\overline{G}$ input controls only the state of the eight output drivers.

With both $\overline{E1}$ low and E2 high, the device is selected and the 13 address inputs are decoded to select one 8-bit word out of 8K words. Read and Write operations on the memory cells are controlled by the $\overline{W}$ input. With either $\overline{E1}$ high or E2 low, the device is deselected, the outputs disabled and the power consumption is reduced to less than one-fourth of the active mode power. $\overline{G}$ serves only to control the operation of the output drivers. When $\overline{G}$ is high, the output drivers are in a high impedance state, independant of the $\overline{E1}$, E2 and $\overline{W}$ inputs.

READ CYCLE

A read cycle is defined as $W \geq V_{IH}$ min with $\overline{E1} \leq V_{IL}$ max, $E2 \geq V_{IH}$ min and $\overline{G} \leq V_{IL}$ max. Read access time is measured from the later of either $\overline{E1}$ going low, E2 going high, valid address, or $\overline{G}$ going low.

The READ CYCLE 1 waveform shows a read access that is initiated by a change in the address inputs while $\overline{E1}$ is low and E2 is high (with $\overline{G}$ low). The output remains active throughout READ CYCLE 1 and is valid at the specified address access time. The address inputs may change at access time and the output remains valid for a minimum of tAXQX. As long as $\overline{E1}$ remains low and E2 is high, the cycle time is equal to the address access time.

The READ CYCLE 2 waveform shows a read access that is initiated by the later of $\overline{E1}$ going low, E2 going high or $\overline{G}$ going low. As long as address is stable when the later of $\overline{E1}$ goes low or E2 goes high, valid data is at the output at the later of tE1LQV, tE2HQV or tGLQV. If address is not valid when the later of $\overline{E1}$ goes low or E2 goes high, the timing is as specified in READ CYCLE 1. Chip Enable access time is not affected by the duration of the deselect interval.

The $\overline{G}$ signal controls the output buffer. $\overline{G}$ is required to be low (along with $\overline{E1}$ low and E2 high) in order for I/O1 - I/O 8 to be active.

WRITE CYCLE

The write cycle of the IMS1630M is initiated by the later of $\overline{E1}$ or W to transition from a high to a low or E2 transitioning from low to high. The G control will remove bus contention if held high throughout the duration of the write cycle. If G is low during a W controlled write cycle (Write Cycle 1), the output buffer will be turned on by the later of tE1LQX after the falling edge of E1 or tE2HQX after the rising edge of E2. The output buffer is then turned off within tWLQZ of the falling edge of $\overline{W}$. During this interval, it is possible to have bus contention between devices with common input/output connections. Therefore the recommended mode of operation is to keep $\overline{G}$ high during the write cycle. During a write cycle, data on the inputs is written into the selected cells and the outputs are floating.

For any write cycle, tAVWL, tAVE1L, or tAVE2H must be met, depending on whether $\overline{E1}$, E2 or $\overline{W}$ is the last to transition. After either $\overline{W}$ or $\overline{E1}$ goes high or E2 goes low to terminate the write cycle, addresses may change. If address set-up and hold times are not met, contents of other cells may be altered in unpredictable ways. The fidelity of the $\overline{W}$ control signal is very important. Excessive ringing on high to low transitions may cause signals to rise above V_{IL} max, violating the minimum $\overline{W}$ pulse width specification - tWLWH.

WRITE CYCLE 1 waveform shows a write cycle terminated by $\overline{W}$ going high. Data set-up and hold times are referenced to the rising edge of $\overline{W}$. When $\overline{W}$ goes high while $\overline{E1}$ is low and E2 is high, the outputs remain in a high impedance state (unless $\overline{G}$ is low). If $\overline{G}$ is low when $\overline{W}$ goes high at the end of a write cycle the data read from the memory will be the same as the data just written into the memory. Thus, no data bus contention will occur.

WRITE CYCLE 2 waveform shows a write cycle terminated by the later $\overline{E1}$ going high or E2 going low. Data set-up and hold times are referenced to the later of the rising edge of $\overline{E1}$ or the falling edge of E2. With either $\overline{E1}$ high or E2 low the outputs remain in the high impedance state.

When using WRITE CYCLE 1 proper management of the $\overline{G}$ control signal will avoid bus contention. If $\overline{G}$ is low when $\overline{W}$ goes high (with $\overline{E1}$ low and E2 high) the output buffers will be active tWHQX after the rising edge of $\overline{W}$. Data out will be the same as the data just written, unless the address changes. If input data from the previous cycle is still valid after the address changes, contention may result. Contention may also result if the device is selected ($\overline{E1}$ low, E2 high, $\overline{G}$ low) before $\overline{W}$ goes low and input data is valid early in the cycle. The recommended mode of operation is to keep $\overline{G}$ high except when reading data from the device, thus avoiding bus contention.

TTL VS. CMOS INPUTLEVELS

The INMOS 1630M is fully compatible with TTL input levels. The input circuitry of the IMS1630M is designed for maximum speed and also for conversion of TTL level signals to the CMOS levels required for internal operation. The IMS1630M consumes less power when CMOS levels are used instead of TTL levels. The lower CMOS Icc specifications (Icc3 and Icc4) may be achieved by using CMOS levels. The power consumption will be lower at typical TTL levels than at the worst case levels.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper power trace layout and placement of decoupling capacitors to maintain the operating margins of the IMS1630M. The impedance in the decoupling path from the power pin through the decoupling capacitor to the ground pin should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line inductance and the inductance and reactance of the decoupling capacitor.

Current transients associated with the operation of any high speed device have very high frequency components, so line inductance is the dominating factor. To reduce the line inductance, the power trace and ground trace should be gridded or provided by separate power planes. The decoupling capacitor supplies energy for high frequency current transients and should be located as close to the devices with as short lead length as possible. The high frequency decoupling capacitor should have a value of 0.1 µF and be placed between each row of devices in the array. A larger tantalum capacitor of a sufficient value to eliminate low frequency ripple, should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These larger capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path. The ground grid of the memory array should extend to the TTL driver periphery circuit area. This will provide a solid ground reference for the drivers and prevent loss of operating margin due to differential ground noise.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propagating down the lines, especially low going TTL signals, line termination is recommended. The termination may be either series or parallel.

The recommended technique is to use series termination. The series termination technique has the advantage of drawing no DC current and using a minimum number of components. This is accomplished by placing a series resistor in the signal line at the output of the TTL driver to dampen the reflection on the line. The resistor should be placed as close to the driver package as is practical. The line should be kept short by placing the driver-termination combination close to the memory array.

Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10 to 33 ohm range will be required. Because each design will result in a different signal impedance, a resistor of predetermined value may not properly match the signal path impedance. The proper value of resistance should therefore be selected empirically. A resistor of predetermined value may not properly terminate the transmission line.

Proper power distribution techniques, including adequate use of decoupling capacitors, and proper termination of TTL drive outputs are some of the most important yet basic guidelines that need to be followed when designing and building a memory board. The guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment free of noise spikes, undershoot, and excessive ringing. It is wise to verify signal fidelity by observation utilising a wideband oscilloscope and probe.

DATA RETENTION (L version only) (-55°C ≤ T_A ≤ 125°C)

SYMBOL	PARAMETER	MIN	TYP*	MAX	UNITS	NOTES
V_{DR}	Data Retention Voltage	2.0			volts	**V_{IN} ≤ 0.2V** or ≥ (Vcc -0.2V) $\overline{E}$ ≥(Vcc -0.2V)
I_{CCDR1}	Data Retention Current		15	1200	µA	V_{CC} = 3.0 volts
I_{CCDR2}	Data Retention Current		10	800	µA	V_{CC} = 2.0 volts
t_{EHVCCL}	Deselect Time (t_{CDR})	0			ns	j,k
t_{VCCHEL}	Recovery Time (t_R)	t_{RC}			ns	j,k (t_{RC} = Read Cycle Time)

* Typical data retention parameters at 25 °C

Note j: Parameter guaranteed but not tested

Note k: Supply recovery rate should not exceed 100mV per10µs from V_{DR} to V_{CC} min

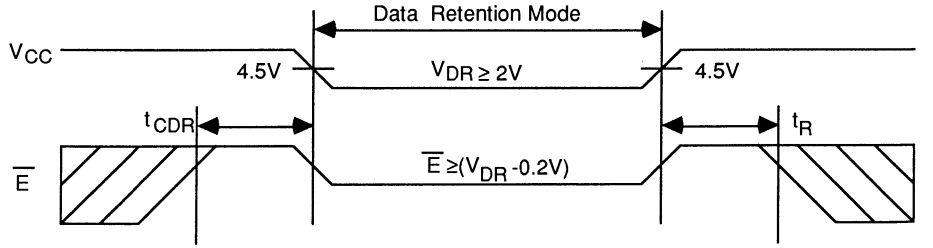
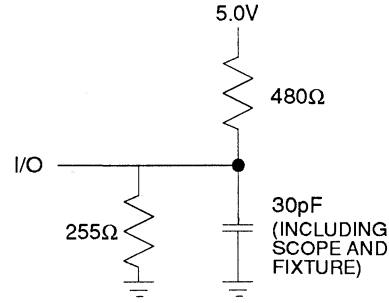


FIGURE 1. OUTPUT LOAD



TRUTH TABLE

$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	I/O	MODE
H	X	X	X	HI-Z	Standby (Isb)
X	L	X	X	HI-Z	Standby (Isb)
L	H	H	H	HI-Z	Output disable
L	H	H	L	Dout	Read
L	H	L	X	Din	Write

Standard Military Drawing version available, see SMD Reference Guide

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER	
			STANDARD	LOW POWER
IMS 1630M IMS1630LM	45ns	CERAMIC DIP	IMS1630S-45M	IMS1630LS45M
	45ns	CERAMIC LCC	IMS1630N-45M	IMS1630LN45M
	55ns	CERAMIC DIP	IMS1630S-55M	IMS1630LS55M
	55ns	CERAMIC LCC	IMS1630N-55M	IMS1630LN55M
	70ns	CERAMIC DIP	IMS1630S-70M	IMS1630LS70M
	70ns	CERAMIC LCC	IMS1630N-70M	IMS1630LN70M

IMS 1605M: 64K x 1
IMS 1625M: 16K x 4
IMS 1629M: 16K x 4 with Output Enable
IMS 1626/7M: 16K x 4 with Separate I/Os
IMS 1635M: 8K x 8
IMS 1695M: 8K x 9

IMS16X5M series High Performance Memory Products

Advance Information

MIL-STD-833C

FEATURES

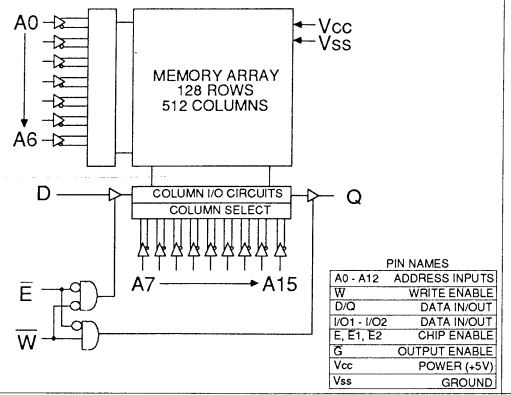
- INMOS' Very High Speed Double Metal CMOS
- Advanced Process-1.2 Micron Design Rules
- 64K Bit Devices
- 20, 25, and 35ns Address Access Times
- 20, 25 and 35 ns Chip Enable Access Times
- Fully TTL Compatible
- Single +5V ± 10% Operation
- Battery Backup Operation - 2V Data Retention, 10µA typical at 25°C
- Packages include: DIP and LCC

DESCRIPTION

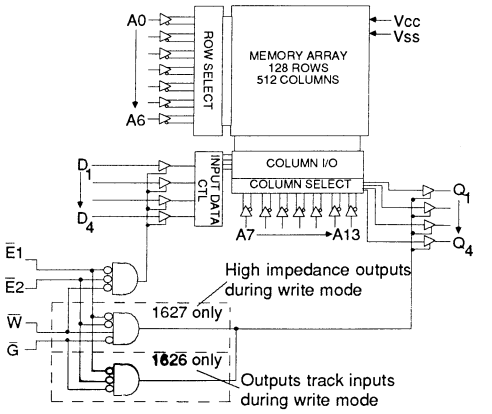
The INMOS IMS16X5M series are high speed advanced 64K double layer metal CMOS Static RAMs.

The range features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. A chip enable function ($\overline{E}$) that can be used to place the device into a low-power standby mode is available on all organisations. The 8K x 8 organisations provide an additional Chip Enable for reduced low-power standby mode. Output Enable ($\overline{G}$) is an enhancement on organisations requiring fast access to data and enhanced bus contention control. The 16x5M series are intended for military applications that demand high performance and superior reliability.

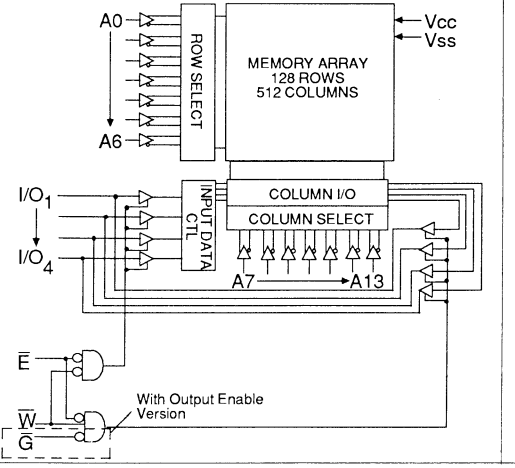
64K x 1



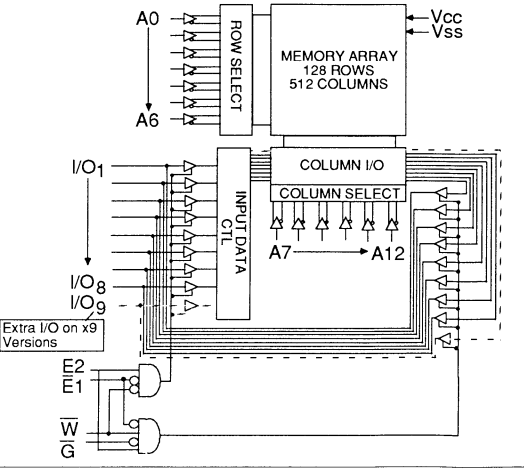
16K x 4 (Separate Inputs and Outputs)



16K x 4 (Without and with Output Enable)



8K x 8 / 8K x 9



IMS1800M CMOS High Performance 256K x 1 Static RAM MIL-STD-883C

Advance Information

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 256K x 1 Bit Organization
- 30, 35 and 45 ns Address Access Times
- 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Separate Data Input and Outputs
- Three-state Output
- 24 Pin 300-mil DIP and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

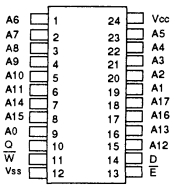
DESCRIPTION

The INMOS IMS1800M is a high performance 256Kx1 CMOS Static RAM. The IMS1800M provides maximum density and speed enhancements with the additional benefits of lower power and superior reliability.

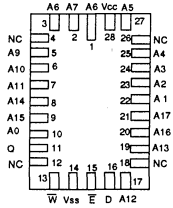
The IMS1800M features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1800M provides a Chip Enable function ($\overline{E}$) that can be used to place the device into a low power standby mode.

The IMS1800M is a high speed VLSI RAM intended for military applications which require high performance and superior reliability.

PIN CONFIGURATION

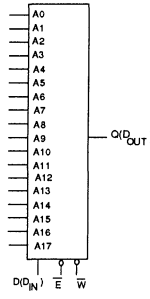


DIP and SOJ

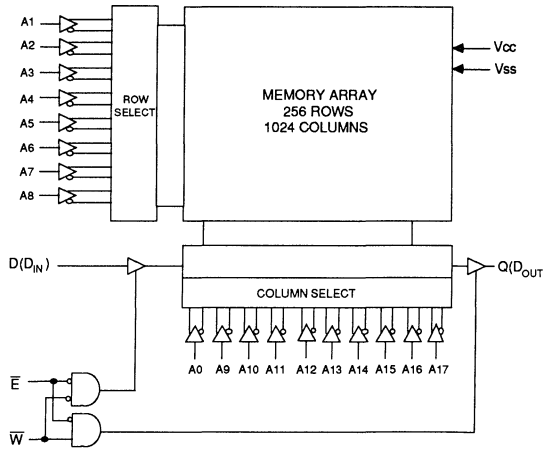


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{17}	ADDRESS INPUTS	Q	DATA OUT
$\overline{W}$	WRITE ENABLE	Vcc	POWER (+5V)
$\overline{E}$	CHIP ENABLE	Vss	GROUND
D	DATA INPUT		

IMS1820M CMOS High Performance 64K x 4 Static RAM MIL-STD-883C

Advance Information

FEATURES

- INMOS' Very High Speed CMOS
- Advanced Process - 1.2 Micron Design Rules
- 64K x 4 Bit Organization
- 30, 35 and 45 ns Address Access Times
- 30, 35 and 45 ns Chip Enable Access Times
- Fully TTL Compatible
- Common Data Input and Outputs
- Three-state Output
- 24 Pin 300-mil DIP and 28 Pin LCC
- Single +5V ± 10% Operation
- Power Down Function

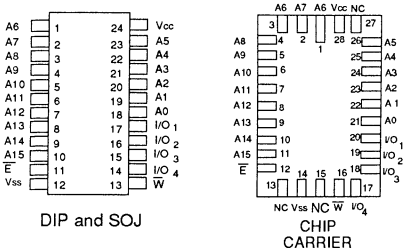
DESCRIPTION

The INMOS IMS1820M is a high performance 64Kx4 CMOS Static RAM. The IMS1820M allows speed enhancements to existing 64K x 4 applications with the additional benefit of reduced power consumption .

The IMS1820M features fully static operation requiring no external clocks or timing strobes, with equal access and cycle times. Additionally, the IMS1820M provides a Chip Enable function (/E) that can be used to place the device into a low power standby mode.

The IMS1820M is a high speed VLSI RAM intended for military applications which require high performance and superior reliability.

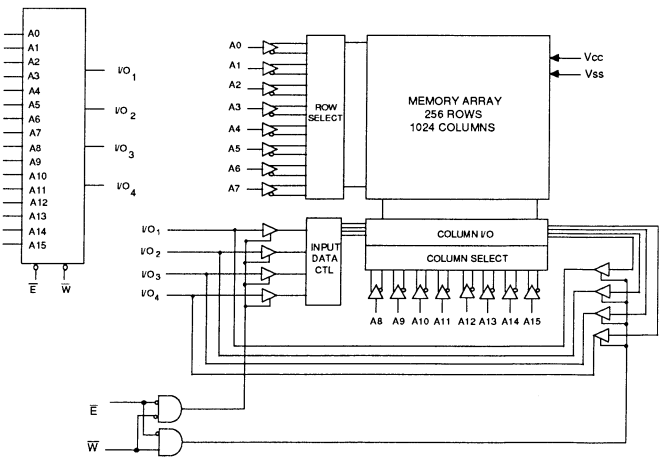
PIN CONFIGURATION



DIP and SOJ

CHIP CARRIER

BLOCK DIAGRAM



PIN NAMES

A_0 - A_{15}	ADDRESS INPUTS	Vcc	POWER (+5V)
$\overline{W}$	WRITE ENABLE	Vss	GROUND
I/O-I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		

IMS2600M

High Performance 64Kx1 Dynamic RAM MIL-STD-883C

FEATURES

- Full Military DRAM Temperature Operating Range (-55°C to +110°C)
- MIL-STD-883C Processing
- 100, 120 and 150nsec $\overline{RAS}$ Access Times
- Cycle Times of 160, 190 and 230ns
- Low Power:
  - 28mW Standby
  - 358mW Active (350ns Cycle Time)
  - 468mW Active (160ns Cycle Time)
- On-Chip Refresh using $\overline{CAS}$-before-$\overline{RAS}$
- 4ms / 256 Cycle Refresh, Pin 1 left as N/C for 256K expansion
- $\overline{RAS}$-Only Refresh Capability
- D_{OUT} Hold under $\overline{CAS}$ control
- JEDEC Standard 16-pin Configuration
- Read, Write Read-Modify-Write Capability both on Single Bit and in Nibble Mode Operation

DESCRIPTION

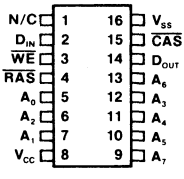
The INMOS IMS2600M 64Kx1 Dynamic RAM is processed in full compliance to MIL-STD-883C. This RAM is fabricated with INMOS' proprietary NMOS technology and utilizes innovative circuit techniques to achieve high performance, low power and wide operating margins.

Multiplexed addresses allows the IMS2600M to be packaged in the conventional 16 pin DIP. Additionally, the IMS2600M features new functional enhancements that make it more versatile than previous dynamic RAMs. CAS-before-RAS Refresh is an "on-chip" refresh mechanism that is upward compatible to 256K generations because pin 1 is left as a no connect. "Nibble Mode" also provides high speed serial access of 4 bits of data, thus providing the system equivalent of 4-way interleaving on chip.

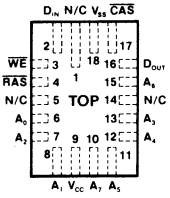
The IMS2600M is fully TTL compatible on all linputs and the output, and operates from a single +5V ±10% power supply.

The IMS2600M is a high speed VLSI RAM intended for military applications which demand high density as well as superior performance and reliability.

PIN CONFIGURATION

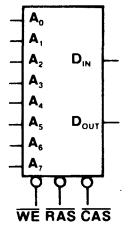


DIP

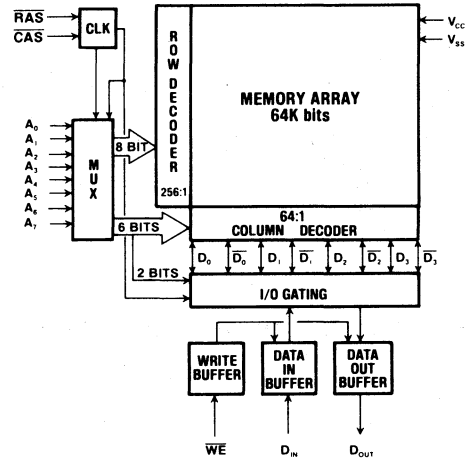


CHIP CARRIER

LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0-A_7	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
$\overline{RAS}$	ROW ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
V_{CC}	+5 VOLT SUPPLY INPUT
V_{SS}	GROUND

DEVICE OPERATION

The IMS2600M contains 65536 (2^{16}) bits of information as 256 (2^8) rows by 256 (2^8) columns. The sixteen addresses for unique bit selection are time-division multiplexed over eight address lines under control of the Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$) clocks. The normal sequence of $\overline{RAS}$ and $\overline{CAS}$ requires that $\overline{CAS}$ is high as $\overline{RAS}$ goes low. This causes the eight address inputs to be latched and decoded for selection of one of the 256 rows. The row addresses must be held for the specified period [t_{RAH} (min)] and then they may be switched to the appropriate column address. After the column addresses are stable for the specified column address setup time, $\overline{CAS}$ may be brought low. This causes the eight address inputs to be latched and used to select a single column in the specified row. The cycle is terminated by bringing $\overline{RAS}$ high. A new cycle may be initiated after $\overline{RAS}$ has been high for the specified precharge interval [t_{RP} (min)]. $\overline{RAS}$ and $\overline{CAS}$ must be properly overlapped and once brought low they must remain low for their specified pulse widths.

READ CYCLE

A read cycle is performed by sequencing $\overline{RAS}$ and $\overline{CAS}$ as described above while holding the $\overline{WE}$ input high during the period when $\overline{RAS}$ and $\overline{CAS}$ are both low. The read access time will be determined by the actual timing relationship between $\overline{RAS}$ and $\overline{CAS}$. If $\overline{CAS}$ goes low within the specified $\overline{RAS}$-to-$\overline{CAS}$ delay [t_{RCD} (max)], then the access time will be determined by $\overline{RAS}$ and be equal to t_{RAC} (max). If $\overline{CAS}$ occurs later than t_{RCD} (max) then the access time is measured from $\overline{CAS}$ and will be equal to t_{CAC} (max).

WRITE CYCLE

The IMS2600M will perform three types of write cycles: Early-Write, Late-Write or Read-Modify-Write. The difference between these cycles is that on an Early-Write D_{OUT} will remain open and on a Late-Write or Read-Modify-Write D_{OUT} will reflect the contents of the addressed cell before it was written.

The type of write cycle that is performed is determined by the relationship between $\overline{CAS}$ and $\overline{WE}$. For Early-Write cycles $\overline{WE}$ occurs before $\overline{CAS}$ goes low, and D_{IN} setup is referenced to the falling edge of $\overline{CAS}$. For Late-Write or Read-Modify-Write cycles $\overline{WE}$ occurs after $\overline{CAS}$, and D_{IN} setup is referenced to the falling edge of $\overline{WE}$.

The choice of write cycle timing is usually very system dependent and the different modes are made available to accommodate these differences. In general, the Early-Write timing is most appropriate for systems that have a bidirectional data bus. Because D_{OUT} remains inactive during Early-Write cycles, the D_{IN} and D_{OUT} pins may be tied together without bus contention.

DEVICE SELECTION AND OUTPUT CONTROL

Selection of a memory device for a read or write operation requires that both $\overline{RAS}$ and $\overline{CAS}$ be sequenced. A device is not selected if $\overline{RAS}$ is sequenced while $\overline{CAS}$ remains high or if $\overline{CAS}$ is sequenced while $\overline{RAS}$ remains high. The device must receive a properly overlapped $\overline{RAS}$/$\overline{CAS}$ sequence to be selected.

Once a device is selected the state of D_{OUT} becomes entirely controlled by $\overline{CAS}$. If $\overline{CAS}$ remains low when $\overline{RAS}$ goes high, D_{OUT} will remain in the state it was in when $\overline{RAS}$ went high. The output will remain unchanged even if a $\overline{RAS}$ sequence occurs while $\overline{CAS}$ is held low.

REFRESH

The IMS2600M remembers data by storing charge on a capacitor. Because the charge will leak away over a period of time it is necessary to access the data in the cell (capacitor) periodically in order to fully restore the stored charge while it is still at a sufficiently high level to be properly detected. For the IMS2600M any $\overline{RAS}$ sequence will fully refresh an entire row of 256 bits. To ensure that all cells remain sufficiently refreshed, all 256 rows must be refreshed every 4 ms.

The addressing of the rows for refresh may be sourced either externally or internally. If the row refresh addresses are to be provided from an external source, $\overline{CAS}$ must be high when $\overline{RAS}$ goes low. If $\overline{CAS}$ is high when $\overline{RAS}$ goes low, any type of cycle (Read, Write, Read-Modify-Write or $\overline{RAS}$ only) will cause the addressed row to be refreshed.

If $\overline{CAS}$ is low when $\overline{RAS}$ falls, the IMS2600M will use an internal 8-bit counter as the source of the row addresses and will ignore the address inputs. This $\overline{CAS}$-before-$\overline{RAS}$ refresh mode is a refresh-only mode and no data access is allowed. Also, $\overline{CAS}$-before-$\overline{RAS}$ refresh does not cause device selection and the state of D_{OUT} will remain unchanged.

NIBBLE MODE

The IMS2600M is designed to allow high-speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during Nibble Mode are determined by the eight row addresses and the most significant 6 bits of the column address. The low-order 2 bits of the column address (A_3, A_6) are used to select one of the 4 nibble bits for initial access. After the first bit is accessed the remaining nibble bits may be accessed by bringing $\overline{CAS}$ high then low (toggle) while $\overline{RAS}$ remains low. Toggling $\overline{CAS}$ causes A_3 and A_6 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for read, write and/or read-modify-write access (See Table 1 for example). If more than 4 bits are accessed during Nibble Mode, the address sequence will begin to repeat. If any bit is written during an access, the new value will be read on any subsequent accesses.

In Nibble Mode, read, write and read-modify-write operations may be performed in any desired combination. (e.g., first bit read, second bit write, third bit read-modify-write, etc.)

Table 1

NIBBLE MODE ADDRESSING SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	ROW ADDRESSES	COLUMN ADDRESSES A_3, A_6	
$\overline{RAS}$/$\overline{CAS}$	1	10101010	10101010	generated externally
toggle $\overline{CAS}$	2	10101010	10101011	
toggle $\overline{CAS}$	3	10101010	10101000	generated internally
toggle $\overline{CAS}$	4	10101010	10101001	
toggle $\overline{CAS}$	1	10101010	10101010	sequence repeats

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc relative to Vss.....-1.0 to +7.0V
Storage Temperature (Ceramic)....-65° C to +150°C
Power Dissipation.....1W
Short Circuit Output Current.....50mA
(One Second Duration)

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS [a, b]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{SS}	Supply Voltage		0		V	
V_{IH}	Logic "1" Voltage	2.4		Vcc+1	V	
V_{IL}	Logic "0" Voltage	-2.0		0.8	V	
T_A	Ambient Operating Temperature	-55°		110	°C	Still Air

DC Electrical Characteristics ($-55°C \le T_A \le 110°C$, $V_{CC} = 5.0V \pm 10\%$) [c]

SYM	PARAMETER		MIN	MAX	UNIT	NOTES
I_{CC_1}	Average Vcc Power Supply (Dynamic Operating) Current	IMS2600M-10		85	mA	tRC = 160ns, tRAS = 100ns
		IMS2600M-10		65		tRC = 350ns, tRAS = 100ns
		IMS2600M-12		85		tRC = 190ns, tRAS = 120ns
		IMS2600M-12		65		tRC = 350ns, tRAS = 120ns
		IMS2600M-15		75		tRC = 230ns, tRAS = 150ns
		IMS2600M-15		65		tRC = 350ns, tRAS = 150ns
I_{CC_2}	Supply Current (Active)			20	mA	RAS & CAS ≤ VIL (max)
I_{CC_3}	Standby Current			5.0	mA	RAS & CAS ≤ VIH (max)
I_{ILK}	Input Leakage Current (any input)			±10	µA	0V ≤VIN ≤ 5.5V (others = 0 V)
I_{OLK}	Output Leakage Current			±10	µA	DOUT = Hi-Z, 0V ≤ DOUT ≤ 5.5V
V_{OH}	Output High Voltage		2.4		V	IOH = -5.0 mA
V_{OL}	Output Low Voltage			0.4	V	IOL =+5.0 mA

Note a: All voltage values in this data sheet are with respect to Vss.
b: After power-up, a pause of 500 µs followed by eight initialization memory cycles is required to achieve proper device operation. Any interval greater than 4 ms with RAS inactivity requires eight reinitialization cycles to achieve proper device operation.
c: Icc is dependent on output loading and cycle rates. Specified values are obtained with output open.

AC TEST CONDITIONS

Input Pulse Levels.....0 to 3V
Input Rise and Fall Times.....5ns between 0.8 and 2.4V
Input and Output Timing Ref. Levels.....0.8 and 2.4V
Output Load.....Equivalent to 2 TTL Loads and 50pF

CAPACITANCE

SYM.	PARAMETER	MAX	UNITS	COND.
C_{IN}	I/P Cap $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	6	pF	d
C_{IN}	I/P Cap. Addresses	5	pF	d
C_{OUT}	O/P Capacitance	7	pF	d o

Note d: Capacitance measured with BOONTON METER.
o: CAS = VIH to disable DOUT

AC OPERATING CONDITIONS ($-55°C \leq T_A \leq +110°C$) ($V_{CC} = 5.0V \pm 10\%$)

NO.	SYM.	PARAMETER	IMS2600M-10		IMS2600M-12		IMS2600M-15		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{RC}	Random Read Cycle Time	160		190		230		ns	
2	t_{RAC}	Access Time from RAS		100		120		150	ns	h
3	t_{CAC}	Access Time from CAS		60		75		90	ns	i
4	t_{RAS}	RAS Pulse Width	100	10K	120	10K	150	10K	ns	
5	t_{RSH}	RAS Hold Time	60		75		90		ns	
6	t_{CAS}	CAS Pulse Width	60		75		90		ns	
7	t_{CSH}	CAS Hold Time	100		120		150		ns	
8	t_{RCD}	RAS to CAS Delay Time	15	40	17	45	20	60	ns	e, j
9	t_{CRS}	CAS to RAS Set-up Time	0		0		0		ns	
10	t_{RP}	RAS Precharge Time	50		60		70		ns	
11	t_{ASR}	Row Address Set-up Time	0		0		0		ns	
12	t_{RAH}	Row Address Hold Time	10		12		15		ns	
13	t_{ASC}	Column Address Set-up Time	0		0		0		ns	
14	t_{CAH}	Column Address Hold Time (Ref. CAS)	25		35		45		ns	
15	t_{AR}	Column Address Hold Time (Ref. RAS)	55		75		95		ns	
16	t_{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t_{RCH}	Read Command Hold Time (Ref. CAS)	0		0		0		ns	k
18	t_{RRH}	Read Command Hold Time (Ref. RAS)	0		0		0		ns	k
19	t_{OFF}	Output Buffer Turn-off Delay	0	25	0	25	0	30	ns	f
20	t_{WCS}	Write Command Set-up Time	0		0		0		ns	m
21	t_{WCH}	Write Command Hold Time (Ref. CAS)	25		30		35		ns	
22	t_{WCR}	Write Command Hold Time (Ref. RAS)	65		70		85		ns	
23	t_{WP}	Write Pulse Width	20		25		30		ns	
24	t_{DS}	Data-in Set-up Time	0		0		0		ns	l
25	t_{DH}	Data-in Hold Time (Ref. CAS)	25		30		35		ns	l
26	t_{DHR}	Data-in Hold Time (Ref. RAS)	55		70		85		ns	
27	t_{RW}	Read-Write Cycle Time	180		215		260		ns	
27	t_{RMW}	Read-Modify-Write Cycle Time	190		225		270		ns	
28	t_{RRW}	Read-Write Cycle RAS Pulse Width	120		145		180		ns	
28	t_{RRW}	Read-Modify-Write Cycle RAS P. W.	130		155		190		ns	
29	t_{CRW}	Read-Write Cycle CAS Pulse Width	90		105		130		ns	
29	t_{CRW}	Read-Modify-Write Cycle CAS P. W.	100		115		140		ns	
30	t_{RDW}	RAS to Write Delay	100		110		140		ns	m
31	t_{CWD}	CAS to Write Delay	60		70		90		ns	m
32	t_{RWL}	Write Command to RAS Lead Time	25		30		35		ns	

AC OPERATING CONDITIONS ($-55°C \leq T_A \leq 110°C$, $V_{CC} = 5.0V \pm 10\%$)

NO.	SYM.	PARAMETER	IMS2600M-10		IMS2600M-12		IMS2600M-15		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX		
33	t_{CWL}	Write Command to CAS Lead Time	25		30		35		ns	
34	t_{NC}	Nibble Mode Read Cycle Time	55		65		75		ns	
35	t_{NCAC}	Nibble Mode Acces Time from CAS		25		30		35	ns	
36	t_{NCAS}	Nibble Mode CAS Pulse Width	25		30		35		ns	
37	t_{NCP}	Nibble Mode CAS Precharge Time	20		25		30		ns	
38	t_{NRSH}	Nibble Mode RAS Hold Time	25		30		35		ns	
39	t_{NRMW}	Nibble Mode RMW Cycle Time	80		95		110		ns	
40	t_{NCRW}	Nibble Mode RMW CAS Pulse Width	45		60		70		ns	
41	t_{NCWD}	Nibble Mode CAS to Write Delay	20		25		30		ns	
42	t_{FCS}	Refresh Set-up for CAS (Ref. RAS)	0		0		0		ns	
43	t_{FCH}	Refresh Hold Time (Ref. RAS)	15		17		20		ns	
	t_{REF}	Refresh Period		4		4		4	ms	
	t_T	Input Rise and Fall Times	3	50	3	50	3	50	ns	n

NOTES:

e: t_{RCD} (max) is a derived parameter; t_{RCD} (max) = t_{RAC} (max) − t_{CAC} (max); t_{RCD} (min) is a restrictive parameter due to CAS-before-RAS refresh.

f: t_{OFF} (max) is defined as the time at which the output achieves the open circuit condition.

h: Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max).

i: Assumes that $t_{RCD} \geq t_{RCD}$ (max).

j: Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is determined exclusively by t_{CAC}.

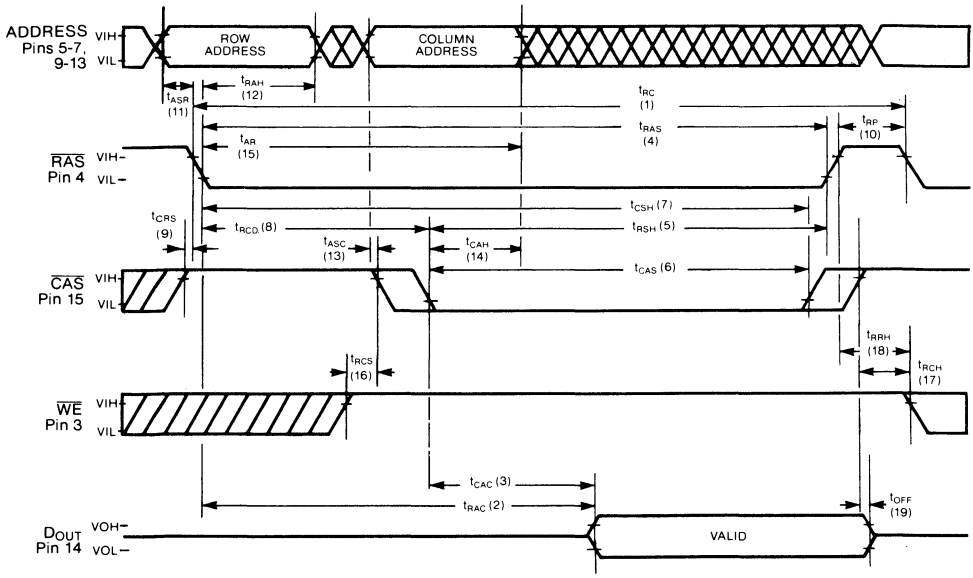
k: Either t_{RRH} or t_{RCH} must be satisfied for a Read cycle.

l: These parameters are referenced to CAS leading edge in Early-Write cycles, and to WE leading edge in Read-Write or Read-Modify-Write cycles.

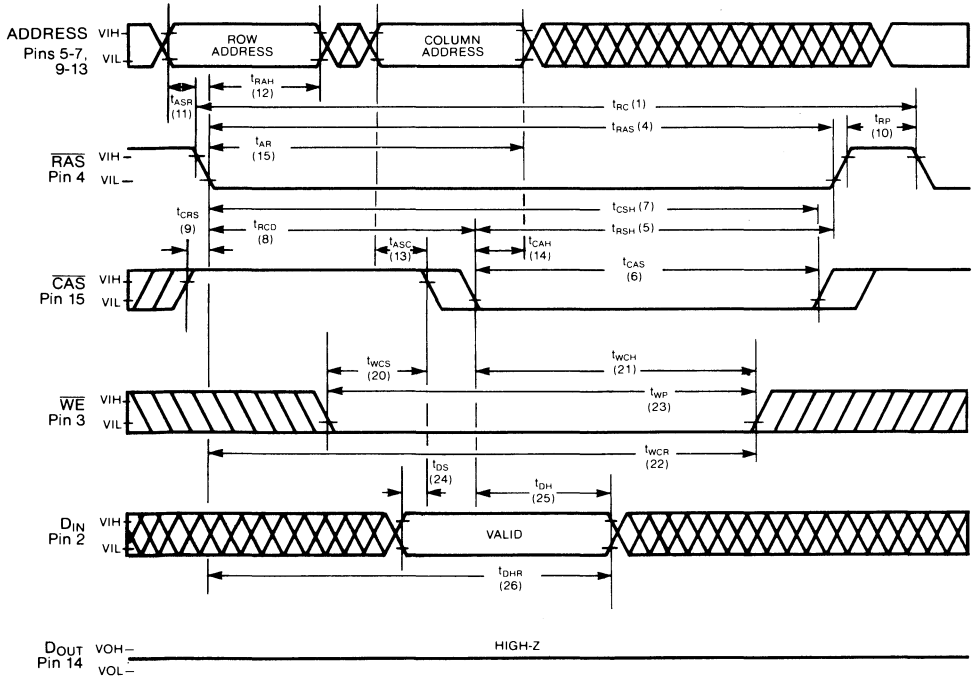
m: t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in Read-Write and Read-Modify-Write cycles only. If $t_{WCS} \geq t_{WCS}$ (min) the cycle is an Early-Write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min) the cycle is a Read-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met the condition of the data out is indeterminate at access time and remains so until CAS returns to V_{IH}.

n: The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner. Transition time measured between V_{IL} (max) and V_{IH} (min).

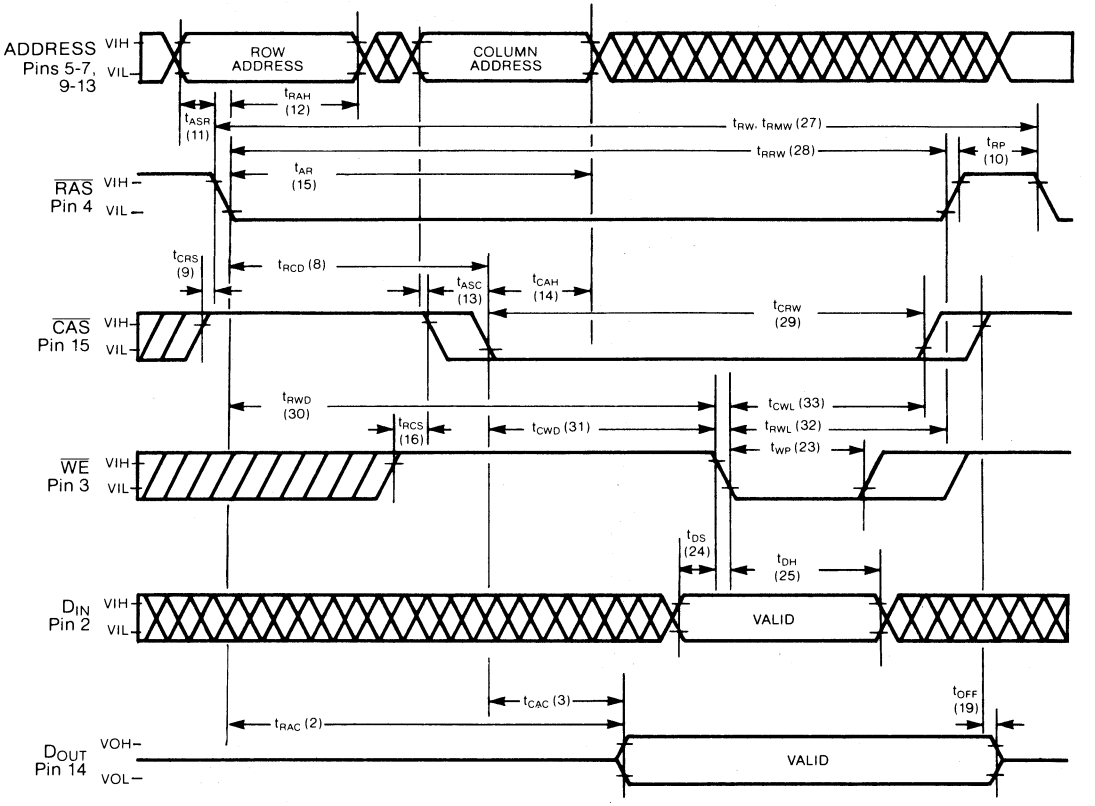
READ CYCLE



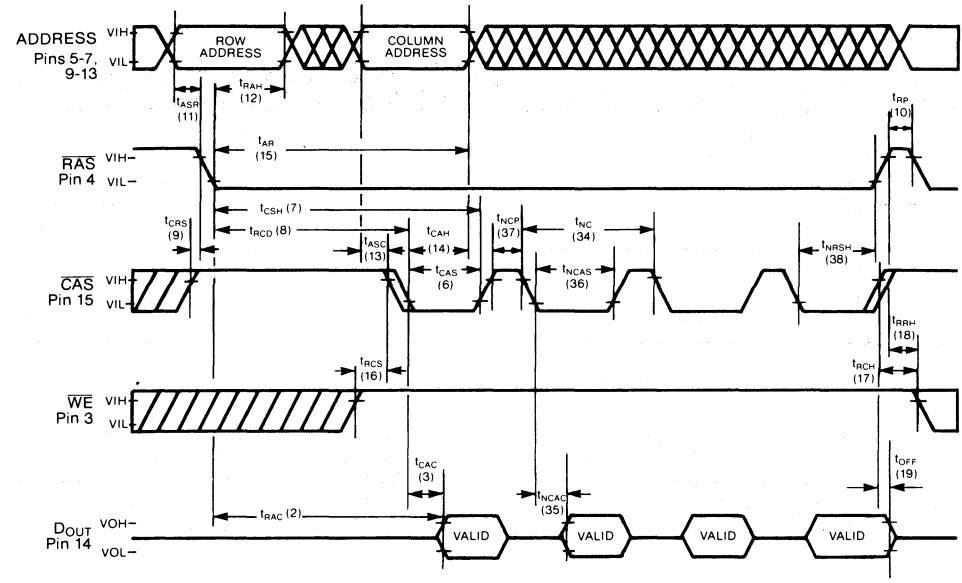
WRITE CYCLE



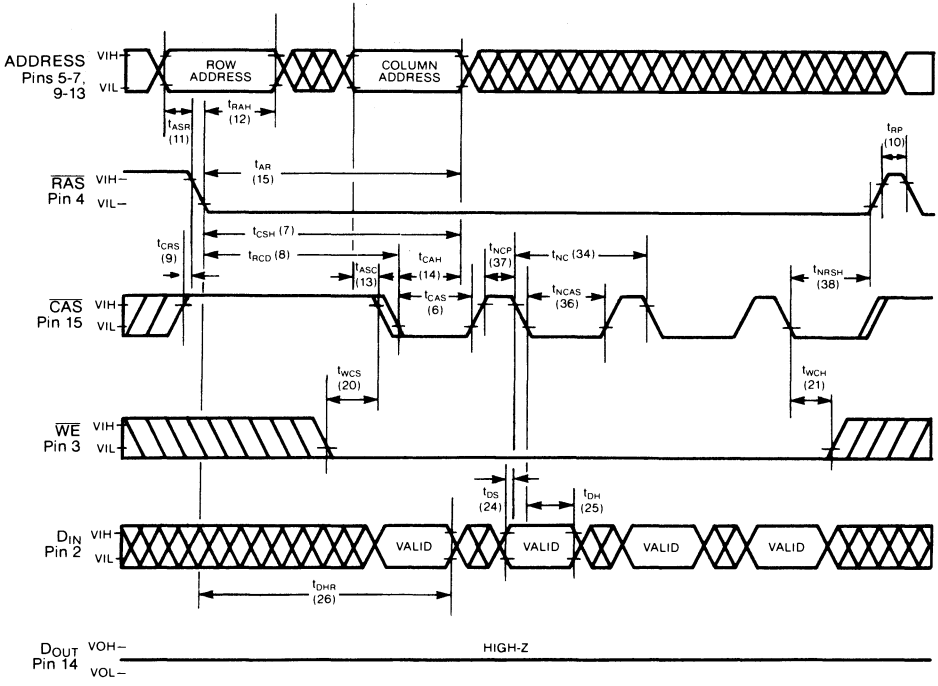
READ-WRITE/READ-MODIFY-WRITE CYCLE



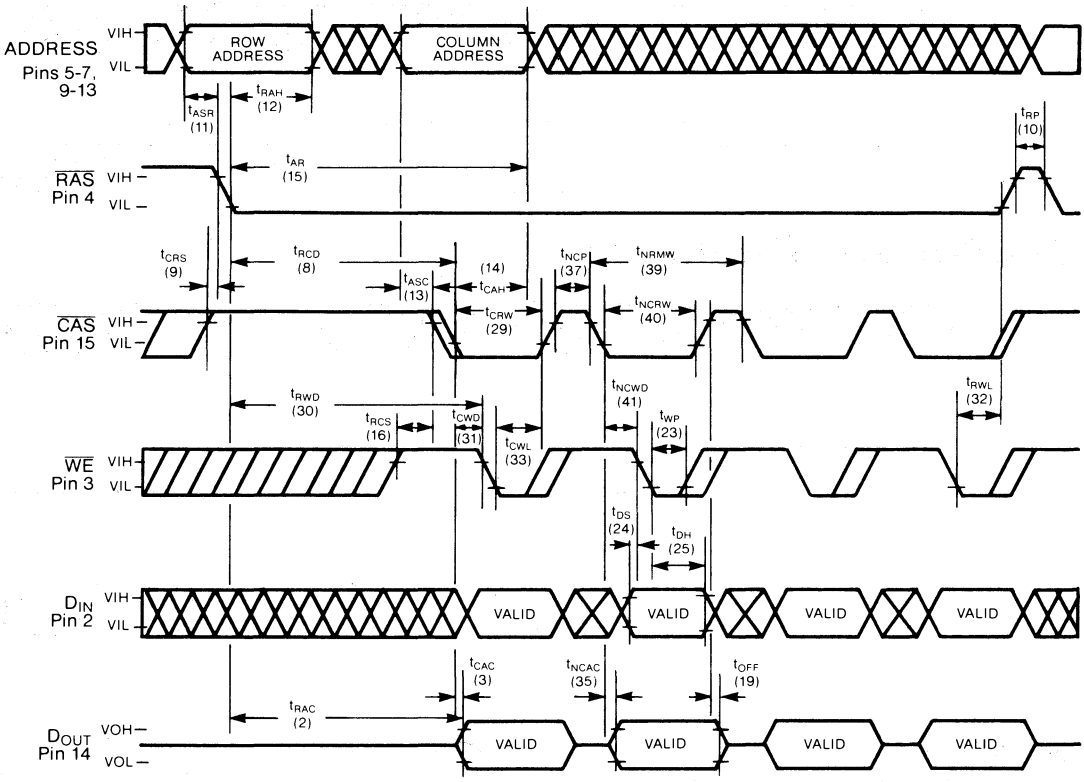
NIBBLE MODE READ CYCLE



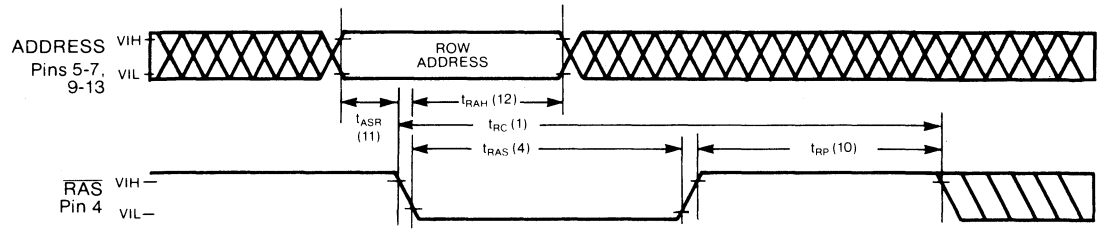
NIBBLE MODE WRITE CYCLE



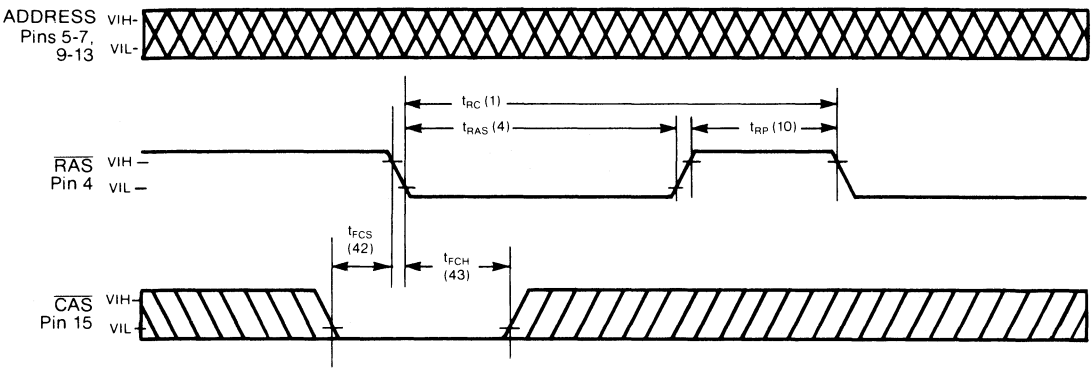
NIBBLE MODE READ-MODIFY-WRITE CYCLE



$\overline{RAS}$-ONLY REFRESH [$\overline{CAS} \geq V_{IH}$ (min)]



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH



APPLICATION

To ensure proper operation of the IMS2600M in a system environment it is recommended that the following guidelines on board layout and power distribution be followed.

POWER DISTRIBUTION

The recommended power distribution scheme combines proper trace layout and placement of decoupling capacitors. The impedance in the decoupling path from the power pin (8) through the decoupling capacitor, to the ground pin (16) should be kept to a minimum. The impedance of this path is determined by the series impedance of the power line and the decoupling capacitor.

To reduce the power line impedance, it is recommended that the power trace and ground trace be gridded or provided by separate power planes. To prevent loss of signal margins due to differential ground noise, the ground grid of the memory array should be extended to the TTL drivers in the peripheral circuitry. A high-frequency decoupling capacitor with a value of 0.1μF should be placed between the rows of memory devices in the array. A larger tantalum capacitor with a value between 22μF and 47μF should be placed near the memory board edge connection where the power traces meet the backplane power distribution system. These large capacitors provide bulk energy storage to prevent voltage drop due to the main supply being located off the memory board and at the end of a long inductive path.

TERMINATION

Trace lines on a memory board in the array look to TTL driver signals like low impedance, unterminated transmission lines. In order to reduce or eliminate the reflections of the TTL signals propogating down the lines, especially low-going TTL signals, line termination is recommended. The termination may be either parallel or series but the series termination technique has the advantages of drawing no DC current and using a minimum of components. The recommended technique is to use series termination.

A series resistor in the signal line at the output of the TTL driver to match the source impedance of the TTL driver to the signal line will dampen the reflections on the line. The line should be kept short with the driver/termination combination close to the memory array. Some experimentation will have to be done to find the proper value to use for the series termination to minimize reflections, but generally a series resistor in the 10Ω to 30Ω range will be required.

Proper power distribution techniques, including adequate use of decoupling capacitors, along with proper termination of TTL driver outputs, are among the most important, yet basic guidelines to be followed. These guidelines are intended to maintain the operating margins of all devices on the memory board by providing a quiet environment relatively free of noise spikes and signal reflections.

ORDERING INFORMATION

DEVICE	SPEED	PACKAGE	PART NUMBER
IMS 2600M	100ns	CERAMIC DIP	IMS2600S-100M
	100ns	CERAMIC LCC	IMS2600N-100M
	100ns	CERAMIC DIP	IMS2600K-100M
	120ns	CERAMIC DIP	IMS2600S-120M
	120ns	CERAMIC LCC	IMS2600N-120M
	120ns	CERAMIC DIP	IMS2600K-100M
	150ns	CERAMIC DIP	IMS2600S-150M
	150ns	CERAMIC LCC	IMS2600N-150M
	150ns	CERAMIC DIP	IMS2600K-100M

military qualification

A Military Qualification

A.1 Military qualification

A.1.1 Military product program

The INMOS Military Product Program has been developed to meet the increasingly demanding requirements for Class B memory product in accordance with paragraph 1.2.1 of MIL-STD-883 'Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices'.

All INMOS MIL-STD-883 Class B product is screened to the specifications of Method 5004 with electrical testing executed over the military temperature range -55°C to +125°C.

Each inspection lot is subjected to the requirements of method 5004 Group A Electrical sampling and Group B Mechanical and Environmental sample testing. Additionally, all new product and changes to product as defined in MIL-M-38510 paragraph 3.4.2 [major changes] is qualified per method 5005 Group C [Die related] and Group D [Package related tests]. Periodic Conformance Testing is carried out per the requirements of MIL-STD-883 paragraph 1.2.1 for all relevent die families and package types.

INMOS MIL-STD-883 product in hermetically sealed packages includes an organic die overcoat [RTV] for enhanced alpha-particle protection. INMOS uses the Alternate Die Inspection procedure in Method 5004 paragraph 3.3.1 which allows for a low magnification visual inspection but requires an additional Temperature Cycle screen in assembly, followed by a voltage stress and low level leakage electrical screen in final test.

Full details of INMOS' military processing are included in INMOS Specification 49-9047, 'General Military Processing Specification', which may be obtained upon request from INMOS.

Suitability for use in specific applications should be determined by using the guidelines of MIL-STD-454.

By specifying an INMOS military product, the user is assured of a product which has been subjected to the full Screening and Quality Conformance requirements of paragraph 1.2.1 of MIL-STD-883 in addition to the full range of in-house process, test and quality control functions designed to enhance the quality and reliability of all INMOS products.

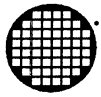
A.1.2 Standard military drawing program

The INMOS Standard Military Drawing (SMD) program was introduced in 1986 to supply military and governmental products. The SMD Program was implemented by the US Government and its associated subcontractors to provide the industry with a single SMD for each military IC requirement. These SMDs are intended to replace the multiplicity of Source Control Drawings (SCDs) generated by each contractor. Components specified according to the SMD Program are standard military MIL-STD-883 compliant devices.

INMOS, and other IC manufacturers, initiate the development of SMDs in conjunction with military contractors who have significant demand for the particular device. Together they initiate an SMD proposal which the Defense Electronics Supply Center (DESC) screens and approves. Accepted SMDs are then circulated by DESC to industry vendors and consumers to obtain multiple sources and registered users.

INMOS fully supports the Standard Military Drawing Program and the DESC efforts to expand its usage.

Appendix B, which details cross reference information, lists each approved INMOS product by its SMD number and the corresponding INMOS part number.



cross reference

B Cross Reference

B.1 Product Cross Reference

AMD	INMOS
AM2147-35	IMS1203-35
AM2147-45	IMS1203-45
AM2147-45M	IMS1203-45M
AM2147-55M	IMS1203-45M
AM2148/9-35	IMS1223-35
AM2148/9-45	IMS1223-45
AM2148/9-55	IMS1223-45
AM2148/9-70	IMS1223-45
AM2148/9-45M	IMS1223-45M
AM2148/9-55M	IMS1223-45M
AM2148/9-70M	IMS1223-45M
AM2168/9-35	IMS1423-35
AM2168/9-40	IMS1423-35
AM2168/9-45	IMS1423-45
AM2168/9-50	IMS1423-45
AM2168/9-55	IMS1423-55
AM2168/9-70	IMS1423-55
AM2168/9-45M	IMS1423-45M
AM2168/9-55M	IMS1423-55M
AM2168/9-70M	IMS1423-55M
AM2167-35	IMS1403-35
AM2167-45	IMS1403-45
AM2167-55	IMS1403-55
AM2167-70	IMS1403-55
AM2167-45M	IMS1403-45M
AM2167-55M	IMS1403-55M
AM99C68-35	IMS1423-35
AM99C68-45	IMS1423-45
AM99C68-55	IMS1423-55
AM99C88-70	IMS1630L-70
AM99C88-100	IMS1630L-100
AM99C88-150	IMS1630L-120

Cypress	INMOS
CY2147-35	IMS1203-35
CY2147-45	IMS1203-45
CY2147-55	IMS1203-45
CY2147-45M	IMS1203-45M
CY2147-55M	IMS1203-45M
CY2148/9-25	IMS1223-25
CY2148/9-35	IMS1223-35
CY2148/9-45	IMS1223-45
CY2148/9-55	IMS1223-45
CY2148/9-45M	IMS1223-45M
CY2148/9-55M	IMS1223-45M
CY7C147-25	IMS1203-25
CY7C147-35	IMS1203-35
CY7C147-45	IMS1203-45
CY7C147-35M	IMS1203-35M
CY7C147-45M	IMS1203-45M
CY7C167-25	IMS1403-25
CY7C167-35	IMS1403-35
CY7C167-45	IMS1403-45
CY7C167-35M	IMS1403-35M
CY7C167-45M	IMS1403-45M
CY7C168-25	IMS1423-25
CY7C168-35	IMS1423-35
CY7C168-45	IMS1423-45
CY7C168-35M	IMS1423-35M
CY7C168-45M	IMS1423-45M

Cypress	INMOS
CY7C187-25	IMS1600-25
CY7C187-35	IMS1600-35
CY7C187-45	IMS1600-45
CY7C187-35L	IMS1600-35M
CY7C187-35LM	IMS1601L-35M
CY7C187-45L	IMS1600-45M
CY7C187-45LM	IMS1601L-45M
CY7C164-25	IMS1620-25
CY7C164-35	IMS1620-35
CY7C164-45	IMS1620-45
CY7C164-35M	IMS1620-35M
CY7C164-45M	IMS1620-45M
CY7C166-25	IMS1624-25
CY7C166-35	IMS1624-35
CY7C166-45	IMS1624-45
CY7C166-35M	IMS1624-35M
CY7C166-45M	IMS1624-45M
CY7C185-35	IMS1630L-35
CY7C185-45	IMS1630L-45
CY7C185-55	IMS1630L-55
CY7C197-25	IMS1800-25
CY7C197-35	IMS1800-35
CY7C197-45	IMS1800-45
CY7C194-25	IMS1820-25
CY7C194-35	IMS1820-35
CY7C194-45	IMS1820-45

EDI	INMOS
84H16CP-25	IMS1620-25
84H16CP-30	IMS1620-30
84H16CP-35	IMS1620-35
84H16CP-45	IMS1620-45
84H16CP-55	IMS1620-55
8808HC-45	IMS1630L-45
8808HC-55	IMS1630L-55
8808HC-70	IMS1630L-70
8808CL-100	IMS1630L-100
8808CL-120	IMS1630L-120
EDI84H64C	IMS1820-45

Fujitsu	INMOS
MB81C67-25	IMS1403-25
MB81C67-35	IMS1403-35
MB81C67-45	IMS1403-45
MB81C67-55	IMS1403-55
MB81C68-25	IMS1423-25
MB81C68-30	IMS1423-25
MB81C68-45	IMS1423-45
MB81C68-55	IMS1423-55
MB81C71-25	IMS1600-25
MB81C71-35	IMS1600-35
MB81C71-45	IMS1600-45
MB81C71-55	IMS1600-55
MB81C74-25	IMS1620-25
MB81C74-35	IMS1620-35
MB81C74-45	IMS1620-45
MB81C74-55	IMS1620-55
MB81C75-25	IMS1624-25
MB81C75-35	IMS1624-35
MB81C75-45	IMS1624-45
MB81C75-55	IMS1624-55
MB81C78-35	IMS1630L-35
MB81C78-45	IMS1630L-45
MB8464A-70	IMS1630L-70
MB8464A-80	IMS1630L-70
MB8464A-100	IMS1630L-100
MB8464A-120	IMS1630L-120
MB81C81-45	IMS1800-45
MB81C84-45	IMS1820-45

GE/RCA	INMOS
CDM5167-55	IMS1403-55
CDM6264-120	IMS1630L-120

B Cross Reference

Goldstar	INMOS
GM76C64-45	IMS1600-45
GM76C64-55	IMS1600-55
GM76C164-25	IMS1620-25
GM76C164-35	IMS1620-35
GM76C164-45	IMS1620-45
GM76C88-60	IMS1630L-55
GM76C88-80	IMS1630L-70

Harris	INMOS
HM65262-55	IMS1403-55
HS65162-90	IMS1630L-70

Hitachi	INMOS
HM6147-35	IMS1203-35
HM6147-45	IMS1203-45
HM6147-55	IMS1203-45
HM6148-35	IMS1223-35
HM6148-45	IMS1223-45
HM6148-55	IMS1223-45
HM6167-35	IMS1403-35
HM6167-45	IMS1403-45
HM6167H-45	IMS1403-45
HM6167H-55	IMS1403-55
HM6268-25	IMS1423-25
HM6268-35	IMS1423-35
HM6268-45	IMS1423-45
HM6268-55	IMS1423-55
HM6287-25	IMS1600-25
HM6287-35	IMS1600-35
HM6287-45	IMS1600-45
HM6287-55	IMS1600-55
HM6287L-25	IMS1601L-25
HM6287L-35	IMS1601L-35
HM6287L-45	IMS1601L-45
HM6287L-55	IMS1601L-55
HM6288-25	IMS1620-25
HM6288-30	IMS1620-30
HM6288-35	IMS1620-35
HM6264-100	IMS1630L-100
HM6264-120	IMS1630L-120
HM6207P/LP-35	IMS1820-35
HM6207P/LP-45	IMS1820-45
HM6208HP/LP-25	IMS1820-25
HM6208HP/LP-35	IMS1820-35
HM6208P/LP-35	IMS1820-35
HM6208P/LP-45	IMS1820-45

Hyundai	INMOS
HY61C67-25	IMS1403-25
HY61C67-35	IMS1403-35
HY61C67-45	IMS1403-45
HY61C67-55	IMS1403-55
HY61C68-35	IMS1423-35
HY61C68-45	IMS1423-45
HY61C68-55	IMS1423-55
HY62C87-35	IMS1600-35
HY62C87-45	IMS1600-45
HY62C87-55	IMS1600-55
HY62C88-35	IMS1620-35
HY62C88-45	IMS1620-45
HY62C88-55	IMS1620-55
HY62C64-45	IMS1630L-45
HY62C64-55	IMS1630L-55
HY62C62-70	IMS1630L-70

IDT	INMOS
IDT6167-25	IMS1403-25
IDT6167-35	IMS1403-35
IDT6167-45	IMS1403-45
IDT6167-55	IMS1403-55
IDT6167-35B	IMS1403-35M
IDT6167-45B	IMS1403-45M
IDT6167-55B	IMS1403-55M
IDT6167-70B	IMS1403-55M
IDT6168-25	IMS1423-25
IDT6168-35	IMS1423-35
IDT6168-45	IMS1423-45
IDT6168-55	IMS1423-55
IDT6168-25B	IMS1423-25M
IDT6168-35B	IMS1423-35M
IDT6168-45B	IMS1423-45M
IDT6168-55B	IMS1423-55M
IDT7187-25	IMS1600-25
IDT7187-30	IMS1600-25
IDT7187-35	IMS1600-35
IDT7187-45	IMS1600-45
IDT7187-55	IMS1600-55
IDT7187-25B	IMS1600-25M
IDT7187-30B	IMS1600-25M
IDT7187-35B	IMS1600-35M
IDT7187-45B	IMS1600-45M
IDT7187-55B	IMS1600-55M
IDT7188-25	IMS1620-25
IDT7188-30	IMS1620-30
IDT7188-35	IMS1620-35
IDT7188-45	IMS1620-45
IDT7188-70	IMS1620-55
IDT7188-25B	IMS1620-25M
IDT7188-30B	IMS1620-30M
IDT7188-35B	IMS1620-35M
IDT7188-45B	IMS1620-45M
IDT7188-70B	IMS1620-55M

IDT(Cont'd)	INMOS
IDT7198-25	IMS1624-25
IDT7198-30	IMS1624-30
IDT7198-35	IMS1624-35
IDT7198-45	IMS1624-45
IDT7198-70	IMS1624-55
IDT7198-25B	IMS1624-25M
IDT7198-30B	IMS1624-30M
IDT7198-35B	IMS1624-35M
IDT7198-45B	IMS1624-45M
IDT7198-70B	IMS1624-55M
IDT71C64-35	IMS1630L-35
IDT71C64-45	IMS1630L-45
IDT71C64-55	IMS1630L-55
IDT71C64-70	IMS1630L-70
IDT71C64-85	IMS1630L-70
IDT71C64-100	IMS1630L-100
IDT71C64-120	IMS1630L-120
IDT71C64-45B	IMS1630L-45M
IDT71C64-55B	IMS1630L-55M
IDT71C64-70B	IMS1630L-70M
IDT71257S/L-25	IMS1800-25
IDT71257S/L-35	IMS1800-35
IDT71257S/L-45	IMS1800-45
IDT71258S/L-25	IMS1820-25
IDT71258S/L-35	IMS1820-35
IDT71258S/L-45	IMS1820-45

Lattice	INMOS
SR16K4-35	IMS1423-35
SR16K4-45	IMS1423-45
SR16K4-55	IMS1423-55
SR16K4-45M	IMS1423-45M
SR16K4-55M	IMS1423-55M
SR64K1-35	IMS1600-35
SR64K1-45	IMS1600-45
SR64K1-55	IMS1600-55
SR64K1-45M	IMS1600-45M
SR64K1-55M	IMS1600-55M
SR64K4-25	IMS1620-25
SR64K4-30	IMS1620-30
SR64K4-35	IMS1620-35
SR64K4-45	IMS1620-45
SR64K4-55	IMS1620-55
SR64K4-45M	IMS1620-45M
SR64K4-55M	IMS1620-55M
SR64E4-25	IMS1624-25
SR64E4-30	IMS1624-30
SR64E4-35	IMS1624-35
SR64E4-45	IMS1624-45
SR64E4-55	IMS1624-55
SR64E4-45M	IMS1624-45M
SR64E4-55M	IMS1624-55M
SR64K8-35	IMS1630L-35
SR64K8-40	IMS1630L-35
SR64K8-45	IMS1630L-45
SR64K8-55	IMS1630L-55
SR64K8-45M	IMS1630L-45M
SR64K8-55M	IMS1630L-55M
SR256K1-35	IMS1800-35
SR256K1-45	IMS1800-45
SR256K4-35	IMS1820-35
SR256K4-45	IMS1820-45

Matra-Harris	INMOS
HM65747-25	IMS1203-25
HM65747-35	IMS1203-35
HM65747-45	IMS1203-45
HM65748-25	IMS1223-25
HM65748-35	IMS1223-35
HM65748-45	IMS1223-45
HM65767-25	IMS1403-25
HM65767-35	IMS1403-35
HM65767-45	IMS1403-45
HM65767-55	IMS1403-55
HM65768-25	IMS1423-25
HM65768-35	IMS1423-35
HM65768-45	IMS1423-45
HM65768-55	IMS1423-55
HM65787-25	IMS1600-25
HM65787-35	IMS1600-35
HM65787-45	IMS1600-45
HM65788-25	IMS1620-25
HM65788-35	IMS1620-35
HM65788-45	IMS1620-45
HM65641-55	IMS1630L-55
HM65641-70	IMS1630L-70
HM65641-90	IMS1630L-70
HM2064-2/-8/-15	IMS1630L-70M

Micron	INMOS
MT5C1601-25	IMS1403-25
MT5C1601-35	IMS1403-35
MT5C1604-25	IMS1423-25
MT5C1604-25	IMS1423-25
MT5C6401-25	IMS1600-25
MT5C6401-35	IMS1600-35
MT5C6401-45	IMS1600-45
MT5C6404-25	IMS1620-25
MT5C6404-35	IMS1620-35
MT5C6404-45	IMS1620-45
MT5C6405-25	IMS1624-25
MT5C6405-35	IMS1624-35
MT5C6405-45	IMS1624-45
MT5C2561-25	IMS1800-25
MT5C2561-35	IMS1800-35
MT5C2561-45	IMS1800-45
MT5C2564-25	IMS1820-25
MT5C2564-35	IMS1820-35
MT5C2561-45	IMS1820-45

Mitsubishi	INMOS
M5M21C67-35	IMS1403-35
M5M21C67-45	IMS1403-45
M5M21C67-55	IMS1403-55
M5M21C68-35	IMS1423-35
M5M21C68-45	IMS1423-45
M5M21C68-55	IMS1423-55
M5M5187-25	IMS1600-25
M5M5187-35	IMS1600-35
M5M5187-45	IMS1600-45
M5M5187-55	IMS1600-55
M5M5188AP-25	IMS1620-25
M5M5188AP-55	IMS1620-25
M5M5188P-45	IMS1620-45
M5M5188P-55	IMS1620-55
M5M5178-35	IMS1630L-35
M5M5178-45	IMS1630L-45
M5M5178-55	IMS1630L-55
M5M5165-100	IMS1630L-100
M5M5165-120	IMS1630L-120
M5M5257AP-25	IMS1800-25
M5M5257AP-35	IMS1800-35
M5M5257P-35	IMS1800-35
M5M5257P-45	IMS1800-45
M5M5258AP-25	IMS1820-25
M5M5258AP-55	IMS1820-35
M5M5258P-35	IMS1820-35
M5M5258P-45	IMS1820-45

Mosel	INMOS
MS6167-35	IMS1403-35
MS6167-45	IMS1403-45
MS6167-55	IMS1403-55
MS6167-70	IMS1403-70
MS6168-35	IMS1423-35
MS6168-45	IMS1423-45
MS6168-55	IMS1423-55
MS6168-70	IMS1423-70
MS6287-45	IMS1600-45
MS6287-55	IMS1600-55
MS6287-70	IMS1600-70
MS6288-45	IMS1620-45
MS6288-55	IMS1620-55
MS6288-70	IMS1620-70
MS6264	IMS1630L
MS6264L	IMS1630L

Motorola	INMOS
MCM6147-55	IMS1203-55
MCM6147-70	IMS1203-70
MCM2167-45	IMS1403-45
MCM2167-55	IMS1403-55
MCM2167-70	IMS1403-70
MCM6168-25	IMS1423-25
MCM6168-35	IMS1423-35
MCM6168-45	IMS1423-45
MCM6168-55	IMS1423-55
MCM6168-70	IMS1423-70
MCM6287-25	IMS1600-25
MCM6287-35	IMS1600-35
MCM6287-45	IMS1600-45
MCM62L87-25	IMS1601L-25
MCM62L87-35	IMS1601L-35
MCM62L87-45	IMS1601L-45
MCM62L87-55	IMS1601L-55
MCM6288-25	IMS1620-25
MCM6288-30	IMS1620-30
MCM6288-35	IMS1620-35
MCM6288-45	IMS1620-45
MCM6288-55	IMS1620-55
MCM6290-25	IMS1624-25
MCM6290-30	IMS1624-30
MCM6290-35	IMS1624-35
MCM6290-45	IMS1624-45
MCM6290-55	IMS1624-55
MCM6264-35	IMS1630L-35
MCM6264-45	IMS1630L-45
MCM6164-45	IMS1630L-45
MCM6264-55	IMS1630L-55
MCM6164-55	IMS1630L-55
MCM6164-70	IMS1630L-70
MCM6064-70	IMS1630L-70
MCM6064-100	IMS1630L-100
MCM6064-120	IMS1630L-120

B Cross Reference

Motorola	INMOS
MCM6207-25	IMS1800-25
MCM6207-35	IMS1800-35
MCM6208-25	IMS1820-25
MCM6208-35	IMS1820-35

National	INMOS
NMC2147H	IMS1203-35M
NMC2147H-1	IMS1203-35
NMC2147H-2	IMS1203-45
NMC2147H-3	IMS1203-45
NMC2147H-3L	IMS1203-45
NMC2148H-2	IMS1223-45
NMC2148H-3	IMS1223-45
NMC6164	IMS1630L
NMC6164L	IMS1630L

NEC	INMOS
μPD2147-25	IMS1203-25
μPD2147-35	IMS1203-35
μPD2147-45	IMS1203-45
μPD4311-35	IMS1403-35
μPD4311-45	IMS1403-45
μPD4311-55	IMS1403-55
μPD4314-35	IMS1423-35
μPD4314-45	IMS1423-45
μPD4314-55	IMS1423-55
μPD4361-40	IMS1600-35
μPD4361-45	IMS1600-45
μPD4361-55	IMS1600-55
μPD4362-45	IMS1620-45
μPD4362-55	IMS1620-55
μPD4364-100	IMS1630L-100
μPD4364-120	IMS1630L-120
μPD4464-120	IMS1630L-120
μPD43254-35	IMS1820-35
μPD43254-45	IMS1820-45

Oki	INMOS
MSM5165-100	IMS1630L-100

Performance	INMOS
P4C168-25	IMS1423-25
P4C168-30	IMS1423-25
P4C168-35	IMS1423-35
P4C168-45	IMS1423-45
P4C187-25	IMS1600-25
P4C187-30	IMS1600-25
P4C187-35	IMS1600-35
P4C188-25	IMS1620-25
P4C188-30	IMS1620-30
P4C188-35	IMS1620-35
P4C188-45	IMS1620-45
P4C188-55	IMS1620-55
P4C164-35	IMS1630L-35
P4C164-45	IMS1630L-45

Samsung	INMOS
KM6264-70	IMS1630L-70
KM6264-100	IMS1630L-100
KM6264-120	IMS1630L-120

B Cross Reference

SGS-Thomson	INMOS
MK41H66-25	IMS1403-25
MK41H66-35	IMS1403-35
MK41H68-25	IMS1423-25
MK41H68-35	IMS1423-35
MK41H87-25	IMS1600-25
MK41H87-35	IMS1600-35
MK41H87-45	IMS1600-45
MK41H87-55	IMS1600-55
MK48H64-55	IMS1630L-55
MK48H64-70	IMS1630L-70

Sharp	INMOS
LH5167-55	IMS1403-55
LH5164-100	IMS1630L-100
LH5164-120	IMS1630L-120
LH52252A-25	IMS1800-25
LH52252-35	IMS1800-35
LH52252-45	IMS1800-45
LH52251A-25	IMS1820-25
LH52251-35	IMS1820-35
LH52251-45	IMS1820-45

S-MOS	INMOS
SRM2367-35	IMS1403-35
SRM2367-45	IMS1403-45
SRM2268-45	IMS1423-45
SRM2268-55	IMS1423-55
SRM2261-55	IMS1600-55
SRM2274-35	IMS1620-35
SRM2274-45	IMS1620-45
SRM2274-55	IMS1620-55
SRM2264C-90	IMS1630L-70
SRM2264C-100	IMS1630L-100
SRM2264C-120	IMS1630L-120
SRM20258-45	IMS1820-45

Sony	INMOS
CXK5164-25	IMS1600-25
CXK5164-35	IMS1600-35
CXK5164-45	IMS1600-45
CXK5164-55	IMS1600-55
CXK5464-25	IMS1620-25
CXK5464-30	IMS1620-25
CXK5464-35	IMS1620-35
CXK5864-70	IMS1630L-70
CXK5864-100	IMS1630L-100
CXK5864-120	IMS1630L-120
CXK1256-35	IMS1800-35
CXK1256-45	IMS1800-45
CXK1256-55	IMS1800-45
CXK54256-35	IMS1820-35
CXK54256-45	IMS1820-45
CXK54256-55	IMS1820-45

STC	INMOS
STC6167-55	IMS1403-55
STC6264-45	IMS1630L-45
STC6264-55	IMS1630L-55
STC6264-70	IMS1630L-70
STC6264-90	IMS1630L-70
STC6264-120	IMS1630L-120

Texas Ins.	INMOS
SMJ61CD16-25	IMS1403-25
SMJ61CD16-35	IMS1403-35
SMJ61CD16-45	IMS1403-45
SMJ64C16-35	IMS1423-35
SMJ64C16-45	IMS1423-45
SMJ61CD64-30	IMS1600-25
SMJ61CD64-35	IMS1600-35
SMJ61CD64-55	IMS1600-55
SMJ64C64-30	IMS1620-30
SMJ64C64-40	IMS1620-35
SMJ64C64-55	IMS1620-55

B Cross Reference

Toshiba	INMOS
TM2068-25	IMS1423-25
TM2068-35	IMS1423-35
TM2068-45	IMS1423-45
TM2068-55	IMS1423-55
TC5562-35	IMS1600-35
TC5562-45	IMS1600-45
TC5561-45	IMS1600-45
TC5561-55	IMS1600-55
TC55416-25	IMS1620-25
TC55416-35	IMS1620-35
TC55416-45	IMS1620-45
TC5565-100	IMS1630L-100
TC5565-120	IMS1630L-120
TC5564-120	IMS1630L-120
TC55464-25	IMS1820-25
TC55464-35	IMS1820-35

UMC	INMOS
UM6167-45	IMS1403-45
UM6167-55	IMS1403-55
UMC6168-45	IMS1423-45
UMC6168-55	IMS1423-55

Vitelic	INMOS
V61C67-35	IMS1403-35
V61C67-45	IMS1403-45
V61C67-55	IMS1403-55
V61C68-35	IMS1423-35
V61C62-45	IMS1620-45
V61C62-55	IMS1620-55
V61C64-45	IMS1630L-45
V61C64-55	IMS1630L-55
V61C64-70	IMS1630L-70
V65C64-100	IMS1630L-100
V65C64-120	IMS1630L-120
V62C64-120	IMS1630L-120

VLSI	INMOS
VT20C68-25	IMS1423-25
VT20C68-35	IMS1423-35
VT20C68-45	IMS1423-45
VT64H1-35	IMS1600-35
VT64K54-25	IMS1620-25
VT64K54-35	IMS1620-35
VT64K54-45	IMS1620-45
VT29C98-35	IMS1630L-35
VT29C98-45	IMS1630L-45

Winbond	INMOS
W2464-100	IMS1630L-100
W2464-120	IMS1630L-120

B.2 Standard Military Drawing Reference

SMD Number	INMOS Part Number
4K x 1 (IMS1203)	
5962-8751301VC	SMD1203S-25M
5962-8751301XC	SMD1203A-25M
5962-8751302VC	SMD1203S-35M
5962-8751302XC	SMD1203A-35M
5962-8751303VC	SMD1203S-45M
5962-8751303XC	SMD1203A-45M
1K x 4 (IMS1223)	
5962-8751304VC	SMD1223S-25M
5962-8751304XC	SMD1223A-25M
5962-8751305VC	SMD1223S-35M
5962-8751305XC	SMD1223A-35M
5962-8751306VC	SMD1223S-45M
5962-8751306XC	SMD1223A-45M
16K x 1 (IMS1403)	
8413202RC	SMD1403S-45M
8413202YA	SMD1403N-45M
8413205RC	SMD1403S-35M
8413205YA	SMD1403N-35M
8413208RC	SMD1403S-55M
8413208YA	SMD1403N-55M
4K x 4 (IMS1423)	
5962-8670512RC	SMD1423S-35M
5962-8670512XA	SMD1423N-35M
5962-8670512ZC	SMD1423Y-35M
5962-8670513RC	SMD1423S-45M
5962-8670513XA	SMD1423N-45M
5962-8670513ZC	SMD1423Y-45M
5962-8670514RC	SMD1423S-55M
5962-8670514XA	SMD1423N-55M
5962-8670514ZC	SMD1423Y-55M
5962-8670515RC	SMD1423S-70M
5962-8670515XA	SMD1423N-70M
5962-8670515ZC	SMD1423Y-70M

SMD Number	INMOS Part Number
64K x 1 (IMS1600/IMS1601L)	
5962-8601503XC	SMD1600S-45M
5962-8601503ZA	SMD1600N-45M
5962-8601504XC	SMD1601S-45LM
5962-8601504ZA	SMD1601N-45LM
5962-8601505XC	SMD1600S-55M
5962-8601505ZA	SMD1600N-55M
5962-8601506XC	SMD1601S-55LM
5962-8601506ZA	SMD1601N-55LM
5962-8601507XC	SMD1600S-70M
5962-8601507ZA	SMD1600N-70M
5962-8601508XC	SMD1601S-70LM
5962-8601508ZA	SMD1601N-70LM
16K x 4 (IMS1624)	
5962-8685911LC	SMD1624S-70LM
5962-8685911XA	SMD1624N-70LM
5962-8685912LC	SMD1624S-70M
5962-8685912XA	SMD1624N-70M
5962-8685913LC	SMD1624S-55LM
5962-8685913XA	SMD1624N-55LM
5962-8685914LC	SMD1624S-55M
5962-8685914XA	SMD1624N-55M
5962-8685915LC	SMD1624S-45LM
5962-8685915XA	SMD1624N-45LM
5962-8685916LC	SMD1624S-45M
5962-8685916XA	SMD1624N-45M
8K x 8 (IMS1630)	
5962-8552504XC	SMD1630S-70M
5962-8552504YA	SMD1630N-70M
5962-8552505XC	SMD1630S-55M
5962-8552505YA	SMD1630N-55M
5962-8552510XC	SMD1630S-55LM
5962-8552510YA	SMD1630N-55LM
5962-8552511XC	SMD1630S-70LM
5962-8552511YA	SMD1630N-70LM

Lead Finish Cross Reference

	DIP	LCC	Flat Pack
A = Hot solder dipped	K	N	B/T
C = Gold plated	S	-	A/Y
X = Vendor option	S	-	A/Y

quality and reliability

The INMOS quality programme is set up to be attentive to every phase of the semiconductor product life cycle. This includes specific programmes in each of the following areas:

- Total Quality Control (TQC)
- Quality and Reliability in Design
- Document Control
- New Product Qualification
- Product Monitoring Programme
- Production Testing and Quality Monitoring Procedure

C.1 Total quality control (TQC) and reliability programme

Our objective to continuously build improved quality and reliability into every INMOS part has resulted in a comprehensive Quality/Reliability Programme of which we are proud. This programme demonstrates INMOS' serious commitment to supporting the quality and reliability needs of the electronics marketplace.

INMOS is systematically shifting away from a traditional screening approach to quality control and towards one of building in Experimental Design quality through Statistical Process Control (SPC). This new direction was initiated with a vigorous programme of education and scientific method training.

In the first year of the programme approximately 80 INMOS employees worldwide received thorough SPC training. This training has been extended to cover advanced SPC and experimental design. Some of the courses taught are listed below:

- Experimental Design Techniques
- Statistical Process Control Methods
- Quality Concepts
- Problem Solving Techniques
- Statistical Software Analysis Techniques

Today INMOS utilizes experimental design techniques and process control/monitoring throughout its development and manufacturing cycles. The following TQC tools are currently supported by extensive databases and analysis software.

1. Pareto charts
2. Cause/Effect Diagrams
3. Process Flow Charts
4. Run Charts
5. Histograms
6. Correlation Plots
7. Control Charts
8. Experimental Design
9. Process Capability Studies

C.2 Quality and reliability in design

The INMOS quality programme begins with the design of new INMOS products. The following procedures are examples from the INMOS programme to design quality and reliability into every product.

Innovative design techniques are employed to achieve product performance using, whenever possible, state of the art techniques. For example, INMOS uses 300 nm gate oxides on its high performance graphics, SRAM and MICRO products to obtain the reliability inherent in the thicker gate oxide. In addition, circuit design engineers work hand in hand with process engineers to optimise the design for the process and the process for the product family. The result is a highly reliable design implemented in a process technology

achievable within manufacturing.

INMOS products are designed to have parametric margins beyond the product target specifications. The design performance is verified using simulations of circuit performance over voltage and temperature values beyond those of specified product operation, including verification beyond the military performance range. In addition, the device models are chosen to ensure tolerance to wide variations in process parameters beyond those expected in manufacture.

The design process includes consideration of quality issues such as signal levels available for sensing, reduction of internal noise levels, stored data integrity and testability of all device functions. Electro-static damage protection techniques are included in the design with input protection goals of 2K volts for MIL-STD-883 testing methods. Specific customer requirements can be met by matching their detailed specifications against INMOS designed in margins.

The completion of the design includes the use of INMOS computer aided design software to fully check and verify the design and layout. This improves quality as well as ensuring the timely introduction of new products.

C.3 Document control

The Document Control Department maintains control over all manufacturing specifications, lot travellers, procurement specifications and drawings, reticle tapes and test programmes. New specifications and changes are subject to approval by the Engineering and Manufacturing managers or their delegates. Change is rigorously controlled through an Engineering Change Notice procedure, and QA department managers screen and approve all such changes.

An extensive archiving system ensures that the history of any Change Notice is readily available.

Document Control also has responsibility for controlling in-line documentation in all manufacturing areas which includes distribution of specifications, control of changes and liaison with production control and manufacturing in introducing changed procedures into the line.

Extensive use is made of computer systems to control documentation on an international basis.

C.4 New product qualification

INMOS performs a thorough internal product qualification prior to the delivery of any new product, other than engineering samples of prototypes to customers.

Care is taken to select a representative sample from the final prototype material. This typically consists of three different production lots. Testing is then done to assure the initial product reliability levels are achieved. Product qualifications are done in accordance with MIL-STD-883, methods 5004 and 5005, or CECC/BS9000.

The initial INMOS qualification data, and the ongoing monitor data can be very useful in the user qualification decision process. INMOS also has a very successful history of performing customer qualification testing in-house and performing joint qualification programmes with customers. INMOS remains committed to joint customer/vendor programmes.

C.5 Product monitoring programme

At the levels of quality and reliability performance required today (low PPM and FIT levels), it is essential that a large statistically significant, current product database be maintained. One of the programmes that INMOS uses to accomplish this is the Product Monitoring Programme (PMP).

The PMP is a comprehensive ongoing programme of reliability testing. A small sample is pulled from production lots of a particular part type. This population is then used to create the specific samples to put on the various operating and environmental tests. Tests run in this programme include extended temperature operating life, THB and temperature cycle. Efforts are continuing to identify and correlate more accelerated

tests to be used in the PMP.

C.6 Production testing and quality monitoring procedure

C.6.1 Reliability testing

INMOS' primary reliability test method is to bias devices at their maximum rated operating power supply level in a 140° C ambient temperature. A scheme of time varying input signals is used to simulate the complete functional operation of the device. The failure rate is then computed from the results of the operating life test using Arrhenius modelling for each specific failure mechanism known. The failure rate is reported at a temperature that is a typical worst case application environment and is expressed in units of FITs where 1 FIT = 1 Fail in 10E9 device hours, (100 FIT = 0.01%/1000 Hrs). The current database enables the failure rate to be valid over various environmental conditions.

The failure rate goal for INMOS products is 100 FITs or less at product introduction with a 50 FIT level to be attained within one year.

For plastic packaged product, additional testing methods and reliability indices become important. Humidity testing is used to evaluate the relative hermeticity of the package, and thermal cycling tests are used principally to evaluate the durability of the assembly (e.g. die/bond attach).

The Humidity Test comprises of temperature, humidity, bias (THB) at 85°C, 85% Relative Humidity, and a 5V static bias configuration selected to maintain the component in a state of minimum power dissipation and enhance the formation of galvanic corrosion. INMOS reliability goals have always been to meet or better the current 'industry standards' and a target of less than 1% failures through 1000 hours of THB at 90% confidence has been set.

The Thermal Cycling tests are performed from −65°C to + 150 °C for 500–1000 cycles, with no bias applied. Thermal Shock tests using a liquid to liquid (Freon) method are cycled between −55°C and + 125 °C. The INMOS Reliability qualification and monitoring goal for the above tests is less than 1% failures at 90% confidence.

C.6.2 Production testing

Electrical testing at INMOS begins while the devices are still in wafer form before being divided into individual die. While in this form, two different types of electrical test are performed.

The Parametric Probe test is to verify that the individual component parameters are within their design limits. This is accomplished by testing special components on the wafer. The results of these tests provide feedback to our wafer fab manufacturing facilities which allows them to ensure that the components used in the actual devices perform within their design limits. This testing is performed on all lots which are processed, and any substandard wafers discarded. These components are placed in the scribe streets of the wafer so they are destroyed in the dicing operation when they are not of any further use. By placing them there, valuable chip real estate is saved, thereby holding down cost while still providing the necessary data.

The Electrical Probe test performed on all wafers is the test of each individual circuit or chip on every wafer. The defective dice are identified so they may be later discarded after the wafer has been separated into individual die. This test fully exercises the circuits for all AC and DC datasheet parameters in addition to verifying functionality.

After the dice have been assembled into packages they are again tested in our Final Test operation. In a mature product the typical flow is:

- Preburn-in test
- Burn-in at 140°C
- Final test

- PDA (Percent Defect Allowed)
- Device Symbolisation
- QA Final Acceptance

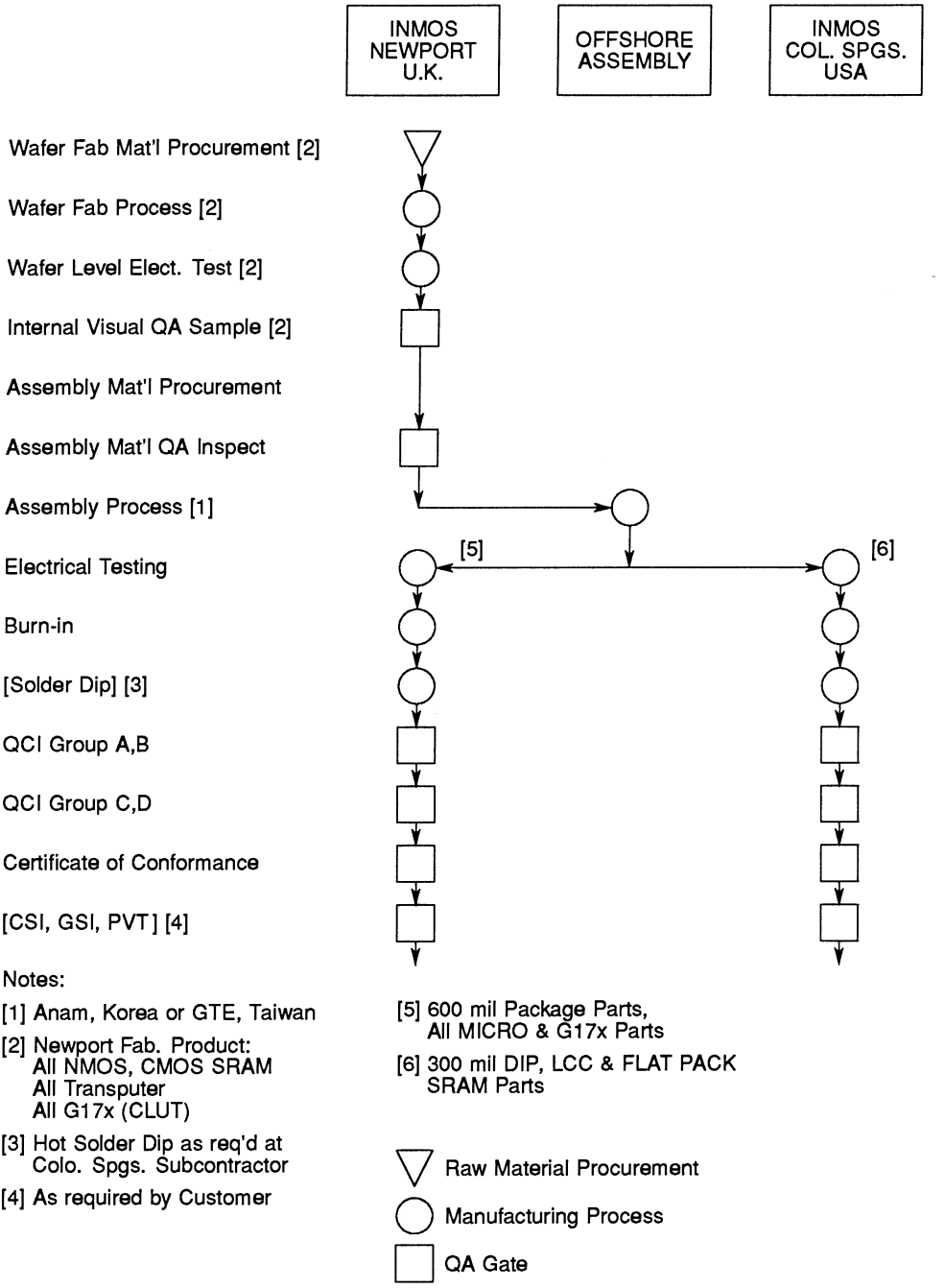
The temperature setting used for hot testing is selected so that the junction temperature is the same as it would be after thermal stabilisation occurred in the specified environment. This is calculated using the hot temperature power dissipation along with the thermal resistance of the package used. All INMOS product is electrically tested and burned-in prior to shipment. Historically, the industry has selected burn-in times using the MIL Standards as a guide (when the market would support the cost) or on a 'best guess' basis dominated by cost considerations. Whereas INMOS invoke a burn-in reduction exercise to ensure the reduced time has no reliability impact.

C.6.3 Quality monitoring procedure

In the Outgoing Quality Monitoring programme, random samples are pulled from lots, that have been successfully tested to data sheet criteria. Rejected lots are 100% retested and more importantly, failures are analysed and corrective actions identified to prevent the recurrence of specific problems.

The extensive series of electrical tests with the associated Burn-in PDA limits and Quality Assurance tests ensure we will be able to continue to improve our high quality and reliability standards.

INMOS MIL-STD-883C/MIL-I-45208
MATERIAL PROCUREMENT & PRODUCT FLOW



Notes:

[1] Anam, Korea or GTE, Taiwan

[2] Newport Fab. Product:
All NMOS, CMOS SRAM
All Transputer
All G17x (CLUT)

[3] Hot Solder Dip as req'd at Colo. Spgs. Subcontractor

[4] As required by Customer

[5] 600 mil Package Parts, All MICRO & G17x Parts

[6] 300 mil DIP, LCC & FLAT PACK SRAM Parts

▽ Raw Material Procurement

○ Manufacturing Process

□ QA Gate

general information

D.1 Thermal considerations

D.1.1 Thermal resistance

An electronic circuit can be characterised by its resistance (impedance), potential differences, current sources, capacitance and time constants. A thermal circuit can be expressed in terms of thermic resistance, thermic differences, heat sources, thermic capacitances and thermic time constants.

The ability of the device package to conduct heat from the chip to the environment is expressed in terms of thermal resistance. The term normally used is Theta ja, written θ_{ja}. It is often separated into two components:

The thermal resistance from the Junction to Case θ_{jc},
and
The thermal resistance from Case to Ambient θ_{ca}.
θ_{ja} represents the total resistance to heat flow from the Chip to Ambient. It is expressed as follows:

$$\theta_{jc} + \theta_{ca} = \theta_{ja}$$

D.1.2 Junction temperature

Junction Temperature (Tj) of a powered integrated circuit is the temperature measured at the substrate diode. When the chip is powered, the heat generated causes the Tj to rise above the ambient temperature (Ta). Tj is calculated by by multiplying the power dissipation of the device by the thermal resistance of the package and adding the ambient temperature to the result.

$$Tj = (Pd.\theta_{ja}) + Ta$$

D.1.3 K-Factor and θ_{ja} Measurement

There is a simple way of measuring the thermal resistance of θ_{ja} of any package. The basic idea is to use the forward voltage drop of a calibrated diode to measure the change in junction temperature due to a known power dissipation. The thermal resistance can be calculated using the following equation:

$$\theta_{ja} = \frac{\Delta Tj}{Pd} = \frac{Tj - Ta}{Pd}$$

Now, If the current through the diode is constant and the temperature changes, we can calculate the temperature coefficient (also called the K-Factor) using the following equation:

$$K = \frac{T_2 - T_1}{V_{F2} - V_{F1}}$$

K = temperature coefficient (°/mV)
T_2 = higher temperature test (°C)
T_1 = lower temperature test (°C)
V_{F2} = forward voltage at T_2
V_{F1} = forward voltage at T_1

D.1.4 Factors affecting θ_{ja}

There are several factors which affect the thermal resistance of any IC package. Effective thermal management requires a sound understanding of all these variables. Package variables include the leadframe design and materials, the plastic or the ceramic used to encapsulate the device and to a lesser extent other variables such as the die and die attach methods. Other factors that have a significant impact on θ_{ja} include

the substrate upon which the IC is mounted, the density of the layout, the air gap between the package and the substrate, the number and length of traces on the board, the use of thermally conducting epoxies and external cooling methods.

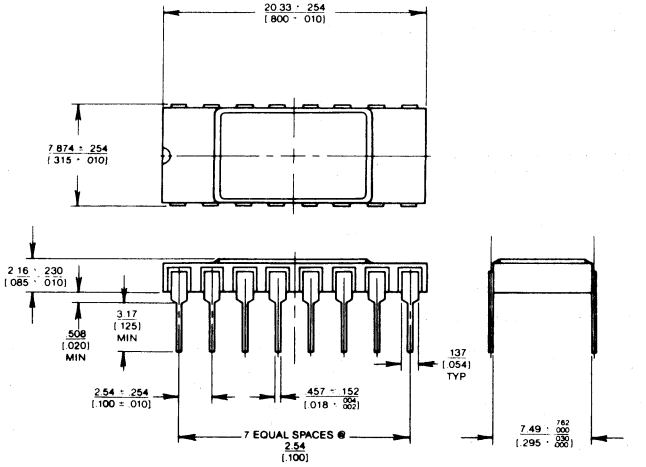
The following list is a summary of θ_{ja}, θ_{jc}, and θ_{jx} for the current range of device types and corresponding package styles where data exists. Thermal resistance is expressed in degC/*Watt*.

Note: θ_{jx} takes into account the 400 linear ft/min moving air measurement condition often specified/required by customers. It is obtained by multiplying θ_{ja} by 0.6. θ_{jc} is measured from the hottest part of the case.

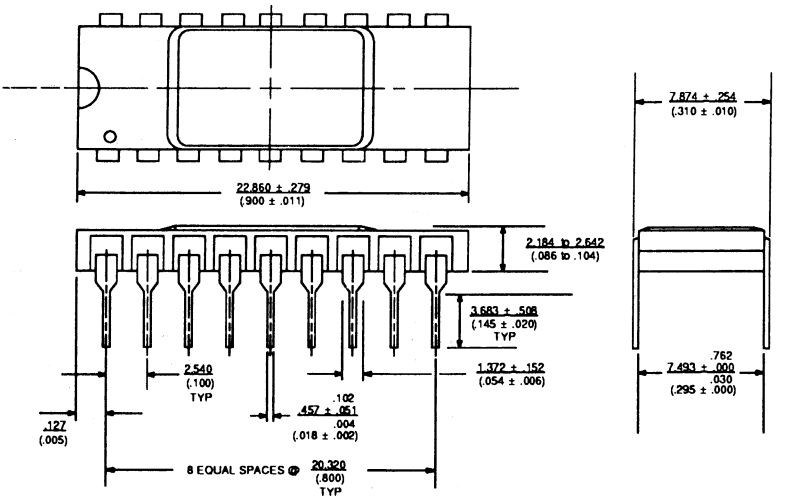
Pin Count	Pin Pitch	Device Types	Pkg	θ_{ja}	θ_{jc}	θ_{jx}
16	0.3"	2600	S	63.1	1.3	37.9
16	–	2600	N	–	–	–
16	–	2600	K	–	–	–
18	0.3"	1203 1223	P	–	–	–
18	0.3"	1203 1223	S	–	–	–
18	–	1203 1223	A	–	–	–
20	0.3"	1400 1420 1403 1423	P	95.0	17.7	56.4
20	0.3"	1400 1420 1403 1423	S	57.6	5.7	31.7
20	–	1400 1420 1403 1423	Y	85.7	8.1	46.9
20	–	1400 1420 1403 1423	N	63.5	–	38.1
20	–	1400 1420 1403 1423	W	–	–	–
20	–	1400 1420 1403 1423	E	–	–	–
22	0.3"	1600 1601 1620	P	85.4	14.9	50.2
22	0.3"	1600 1601 1620	S	47.2	4.5	25.9
22	–	1600 1601 1620	W	–	–	–
24	–	1600 1601 1620	E	–	–	–
24	0.3"	1624	P	–	–	–
24	0.3"	1624	S	–	–	–
24	–	1624	N	52.6	5.1	31.3
24	–	1624	E	–	–	–
28	0.6"	1630	S	48.8	3.7	29.3
28	–	1630	N	–	–	–

Note: measurements are made on Eutectic attached die with RTV overcoat.

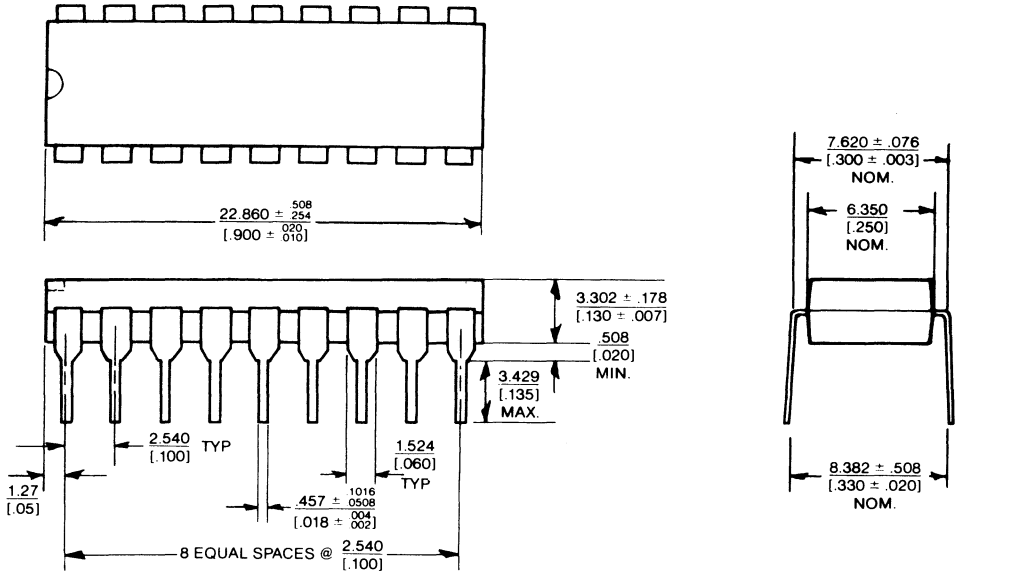
16 PIN CERAMIC DUAL-IN-LINE



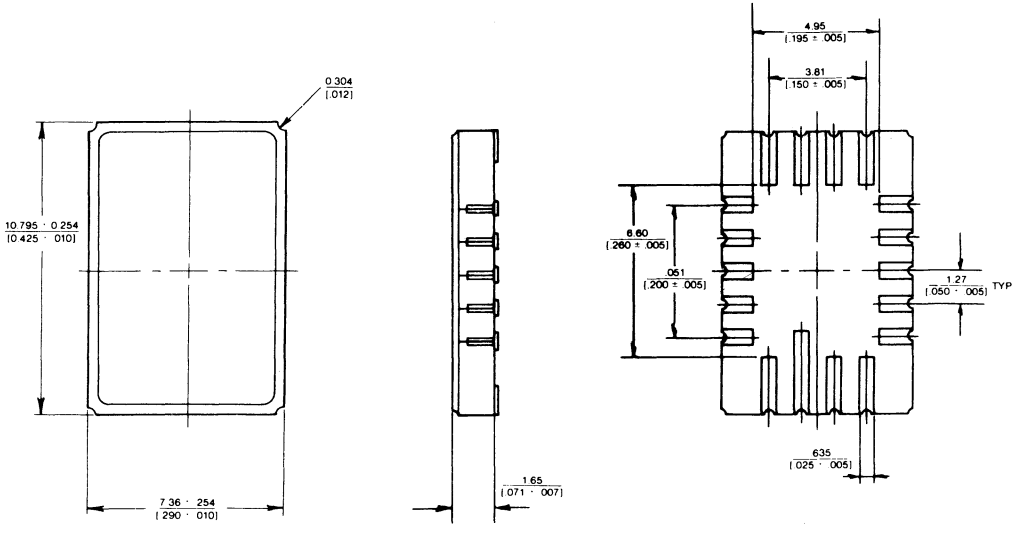
18 PIN CERAMIC DUAL-IN-LINE



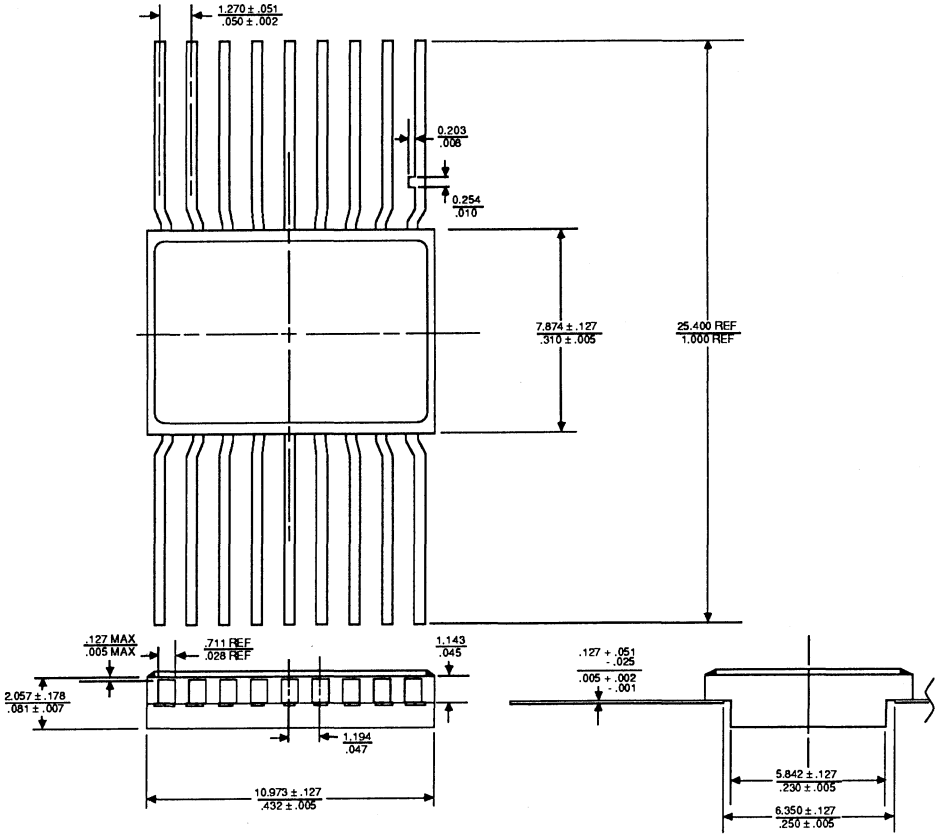
18 PIN PLASTIC DUAL-IN-LINE



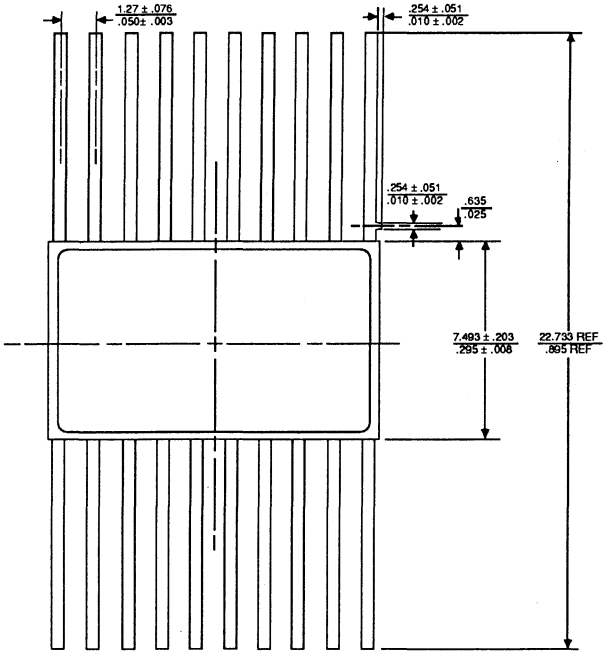
18 PIN CERAMIC LEADLESS CHIP CARRIER

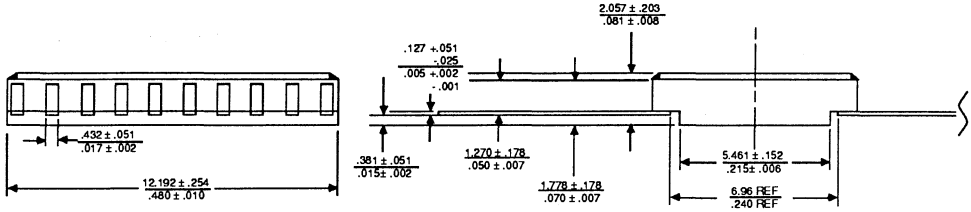


18 PIN FLAT PACK

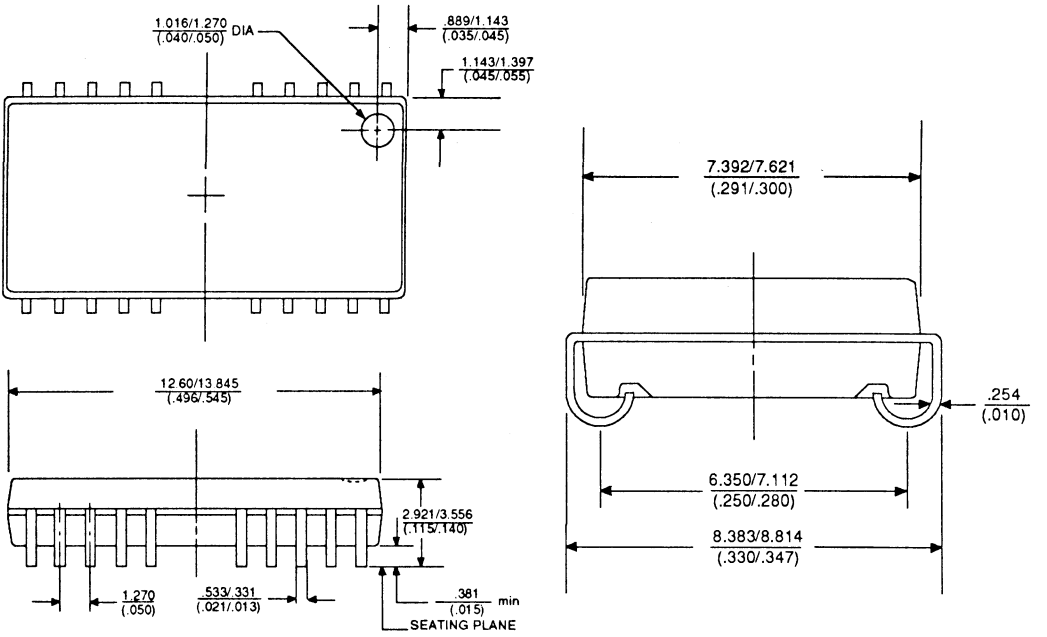


20 PIN FLAT PACK





20 PIN PLASTIC J-LEADED SMALL OUTLINE



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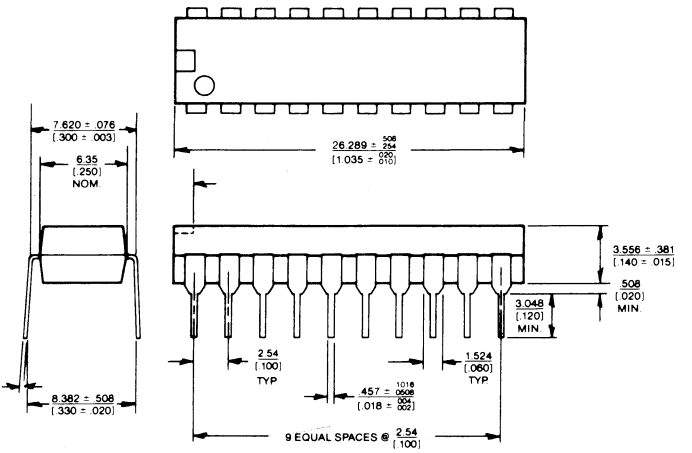
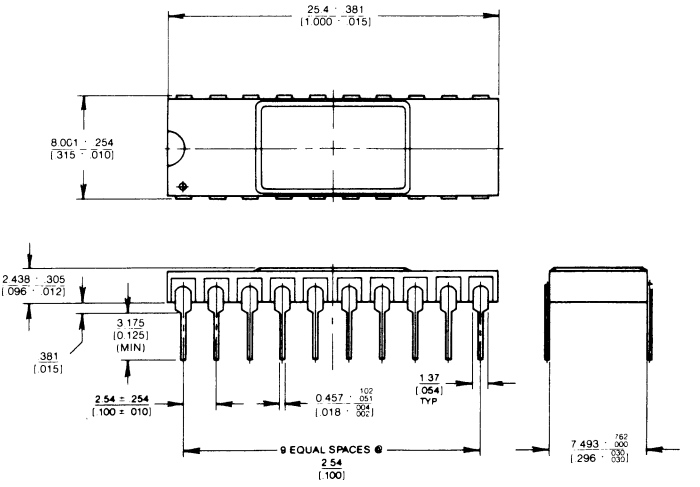
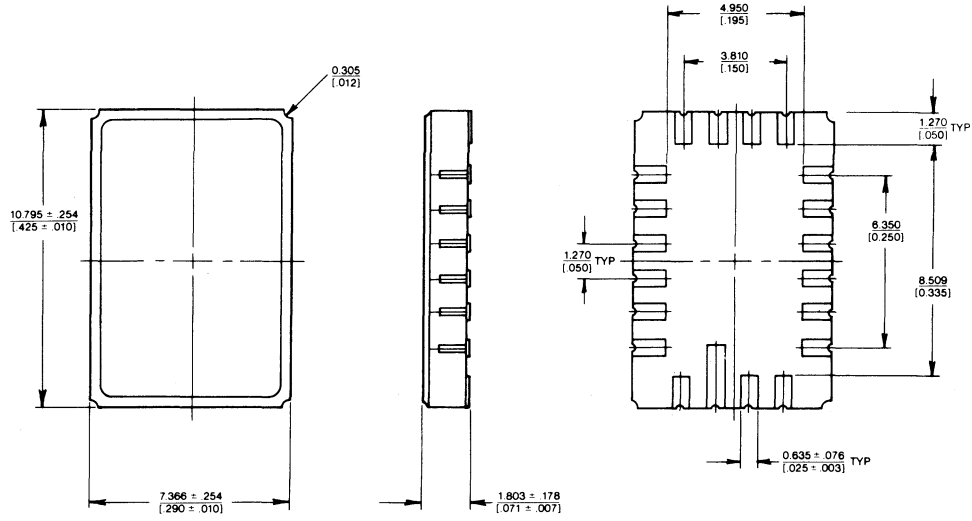


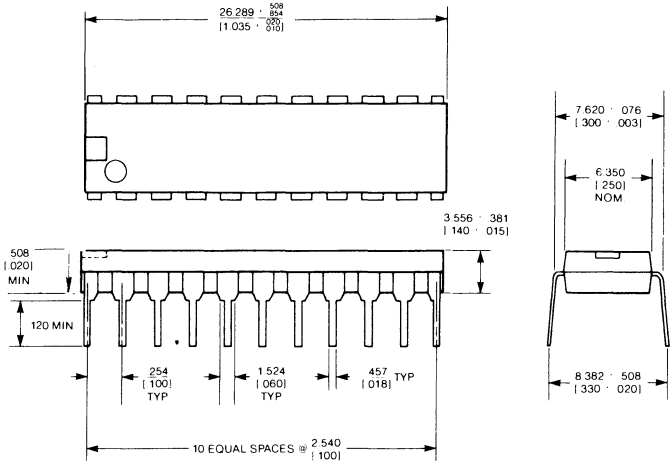
20 PIN CERAMIC DUAL-IN-LINE



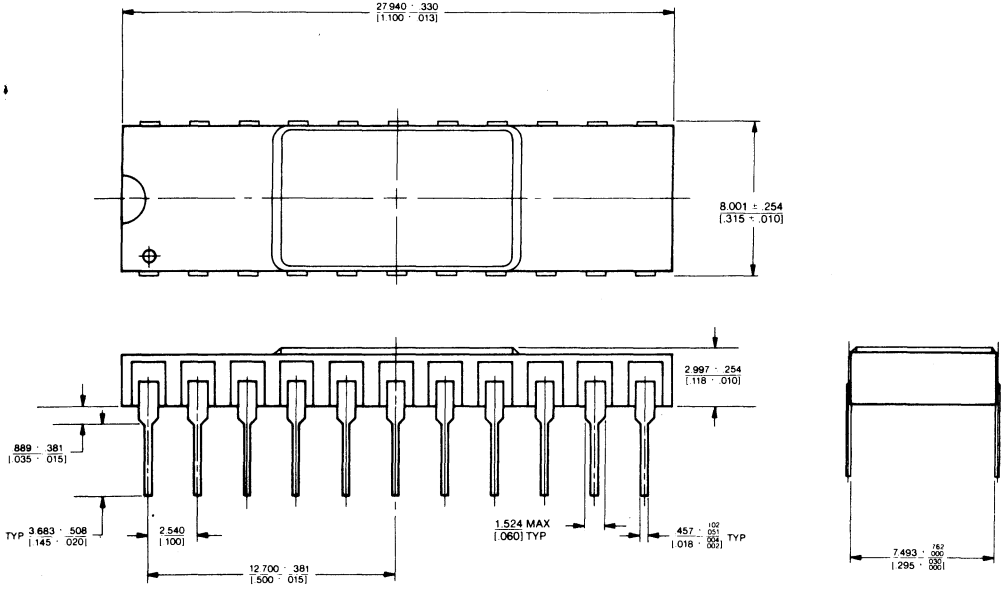
20 PIN CHIP CARRIER



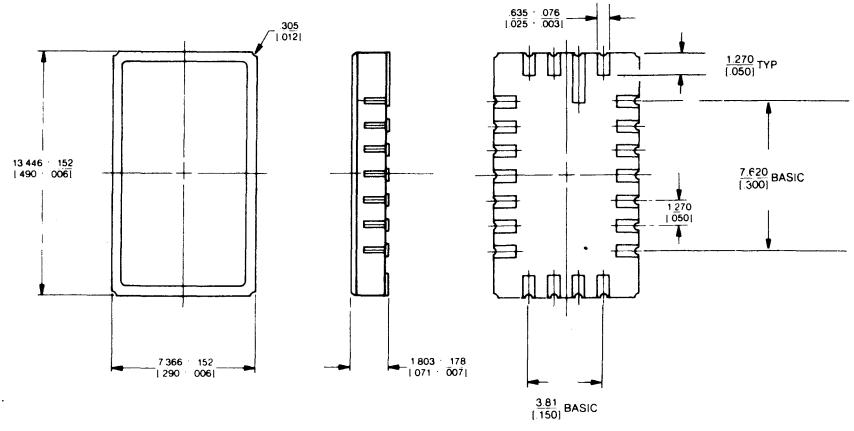
22 PIN PLASTIC DUAL-IN-LINE



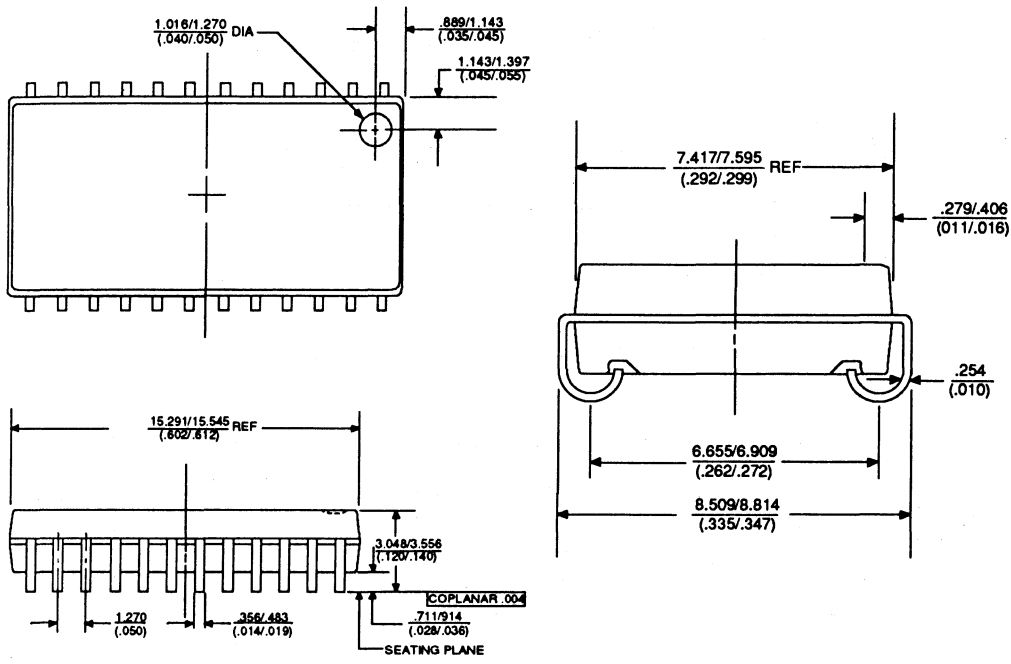
22 PIN CERAMIC DUAL-IN-LINE



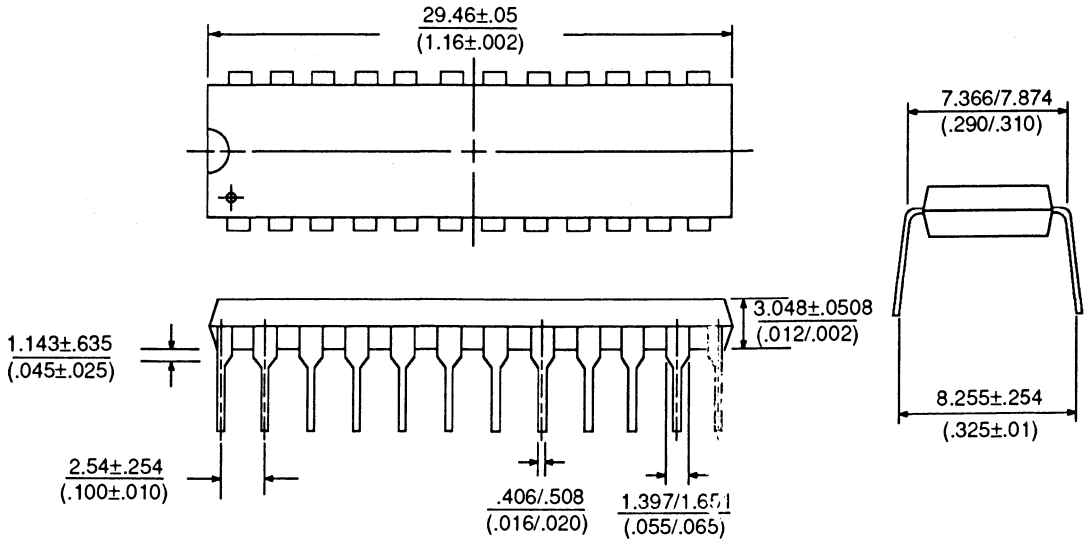
22 PIN CHIP CARRIER



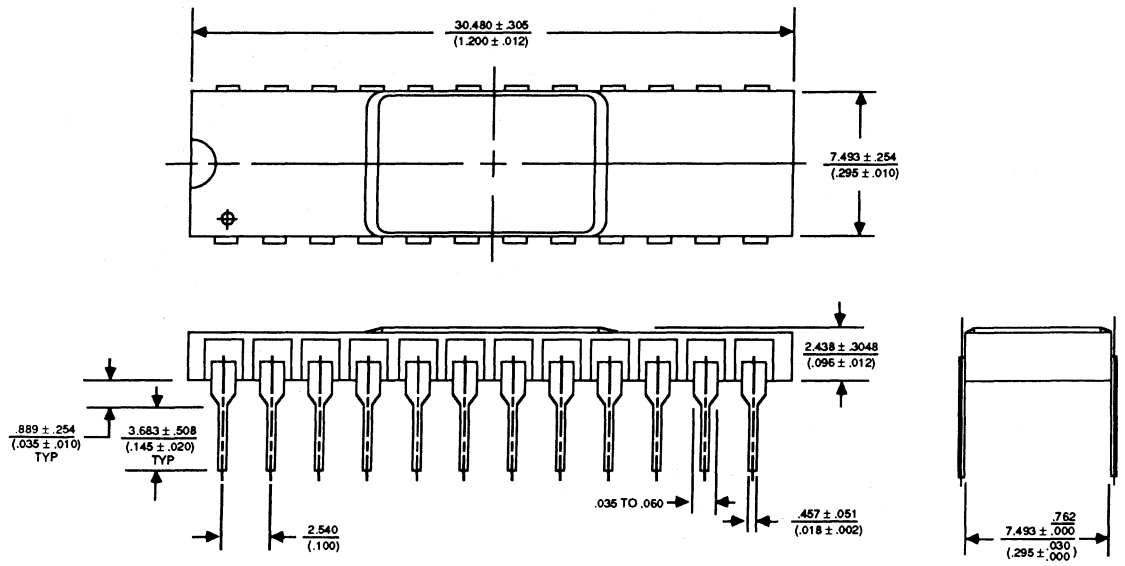
24 PIN PLASTIC J-LEADED SMALL OUTLINE



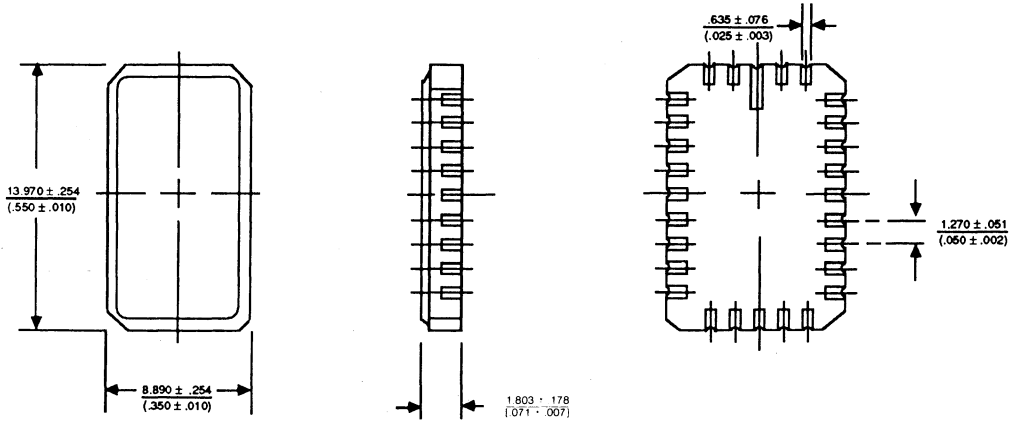
24 PIN PLASTIC DIP



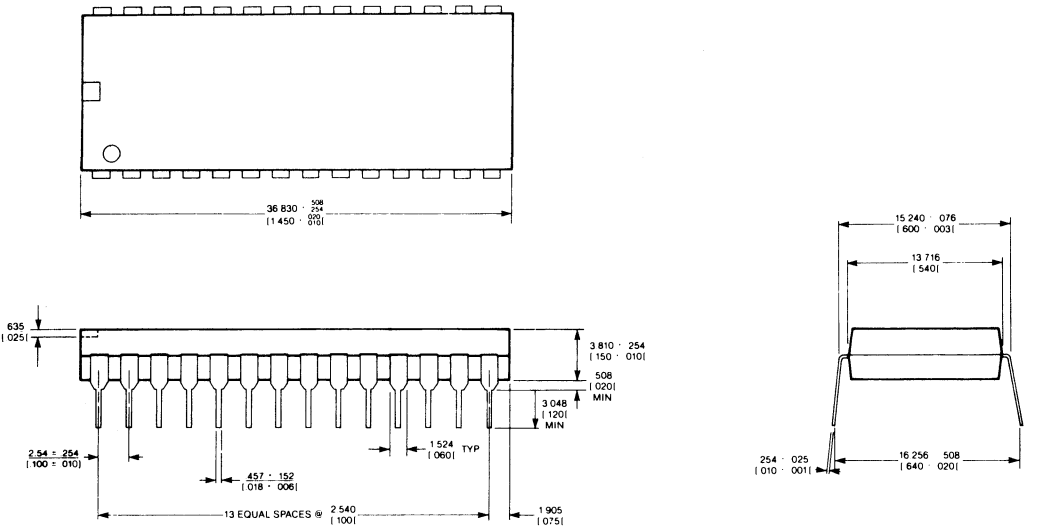
24 PIN CERAMIC DUAL-IN-LINE



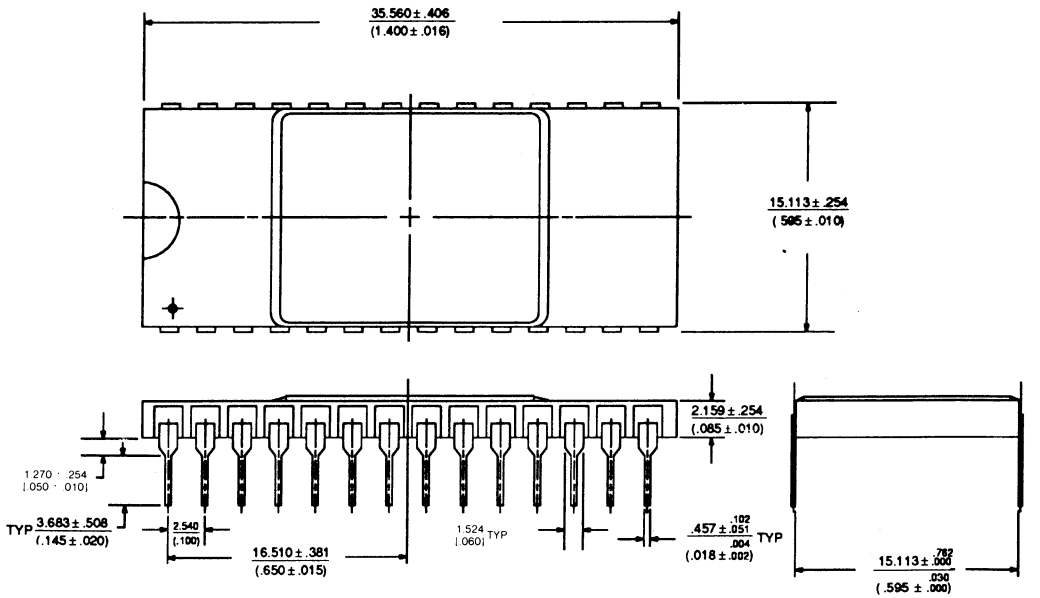
28 PIN CERAMIC LEADLESS CHIP CARRIER



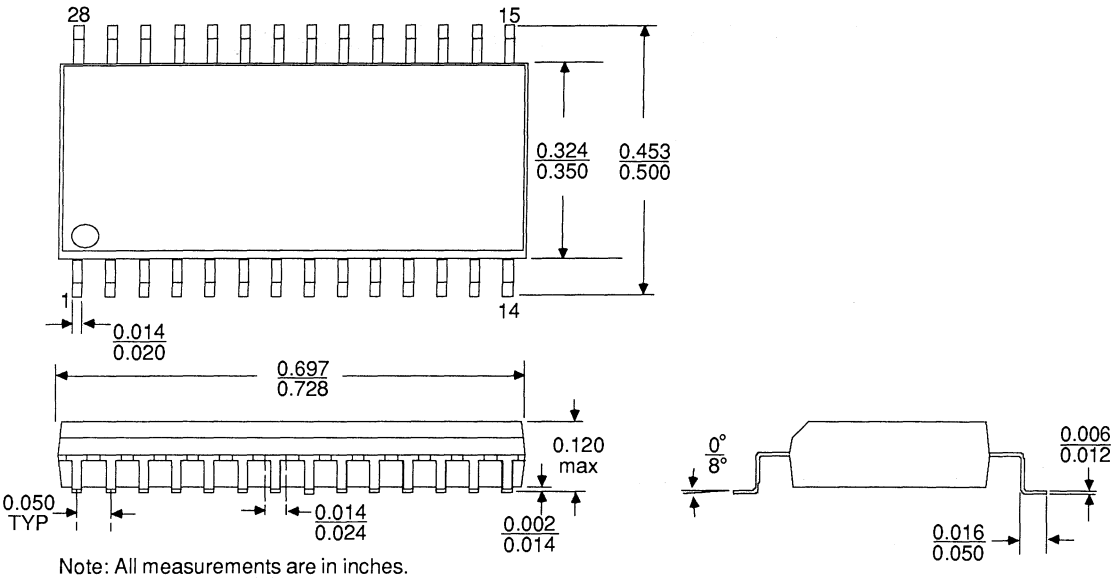
28 PIN PLASTIC DUAL-IN-LINE



28 PIN CERAMIC DUAL-IN-LINE

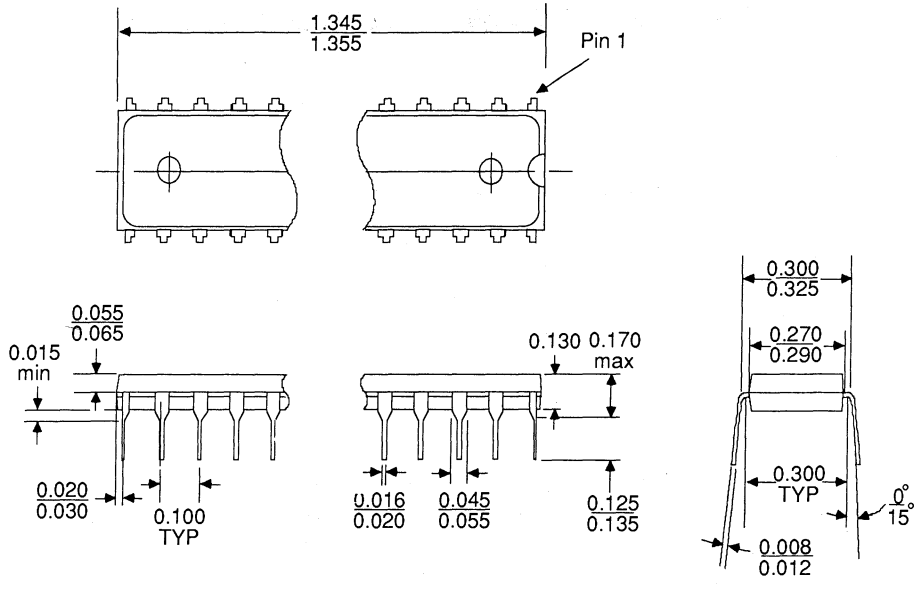


28 PIN SOIC



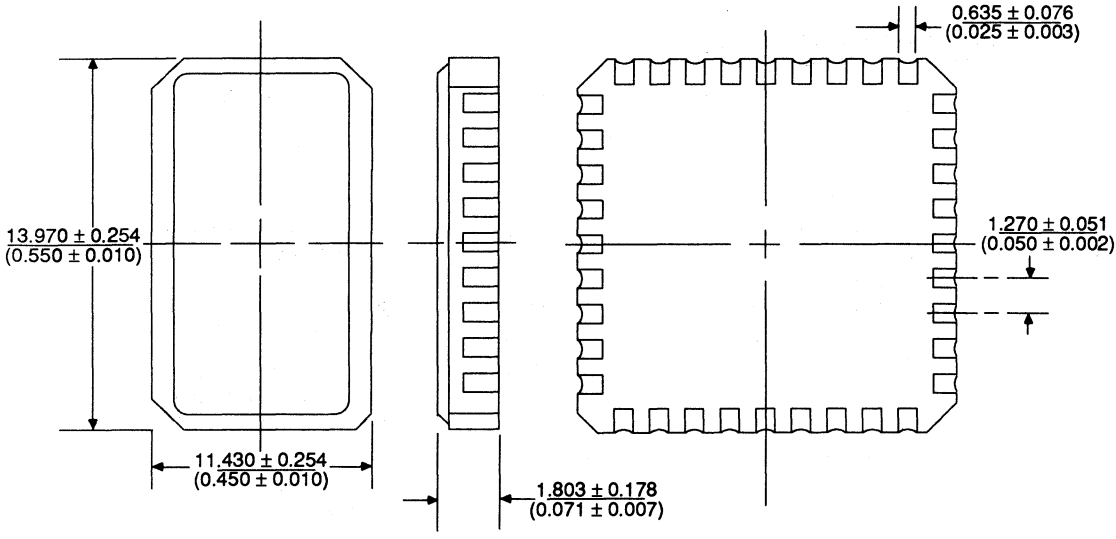
Note: All measurements are in inches.
Top figure denotes minimum dimension; bottom figure denotes maximum dimension.

28 PIN SKINNY DIP

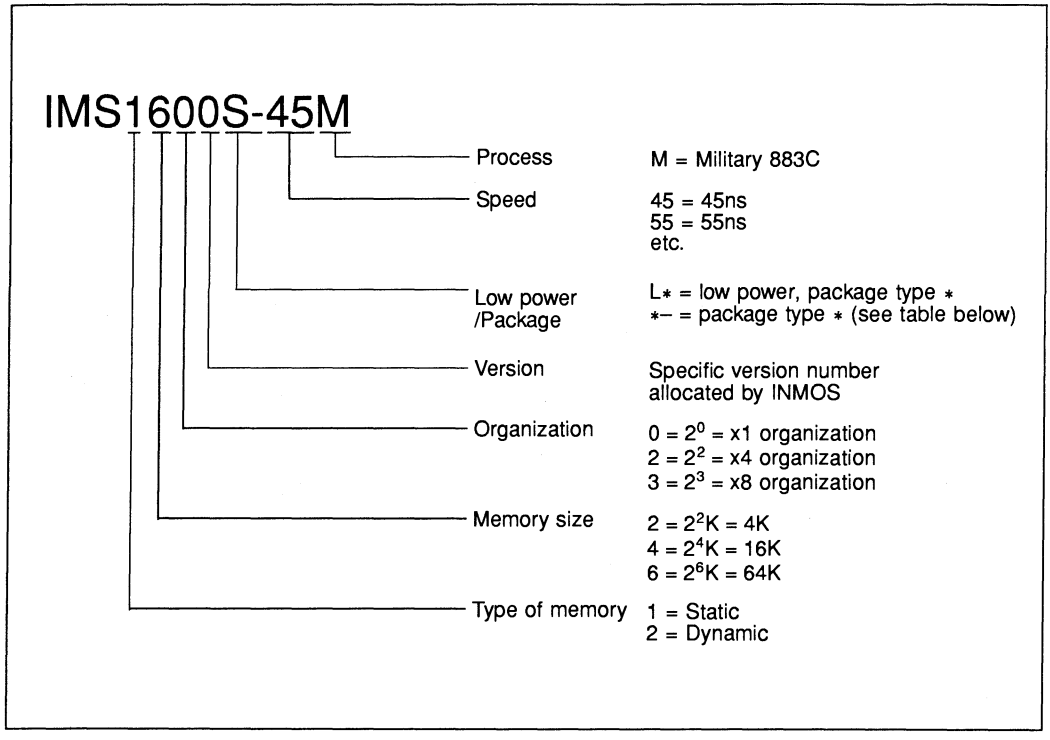


Note: All measurements are in inches.
Top figure denotes minimum dimension; bottom figure denotes maximum dimension.

32 PIN CERAMIC LEADLESS CHIP CARRIER



D.3 Product numbering, package designators and ordering information



Type	Package	Lead finish
A	Formed flat-pack	gold
B	Formed flat-pack	solder
C	LCC	gold
D	Cerdip	solder
E	Small outline, J-bend	solder
G	PGA	gold
H	Small outline, Gull wing	solder
J	PLCC, J-bend	solder
K	Sidebraze ceramic DIP	solder
N	Ceramic LCC	solder
P	Plastic DIP	solder
S	Sidebraze ceramic DIP	gold
T	(Skinny) Flat-pack	solder
W	Ceramic LCC	gold
Y	(Skinny) Flat-pack	gold