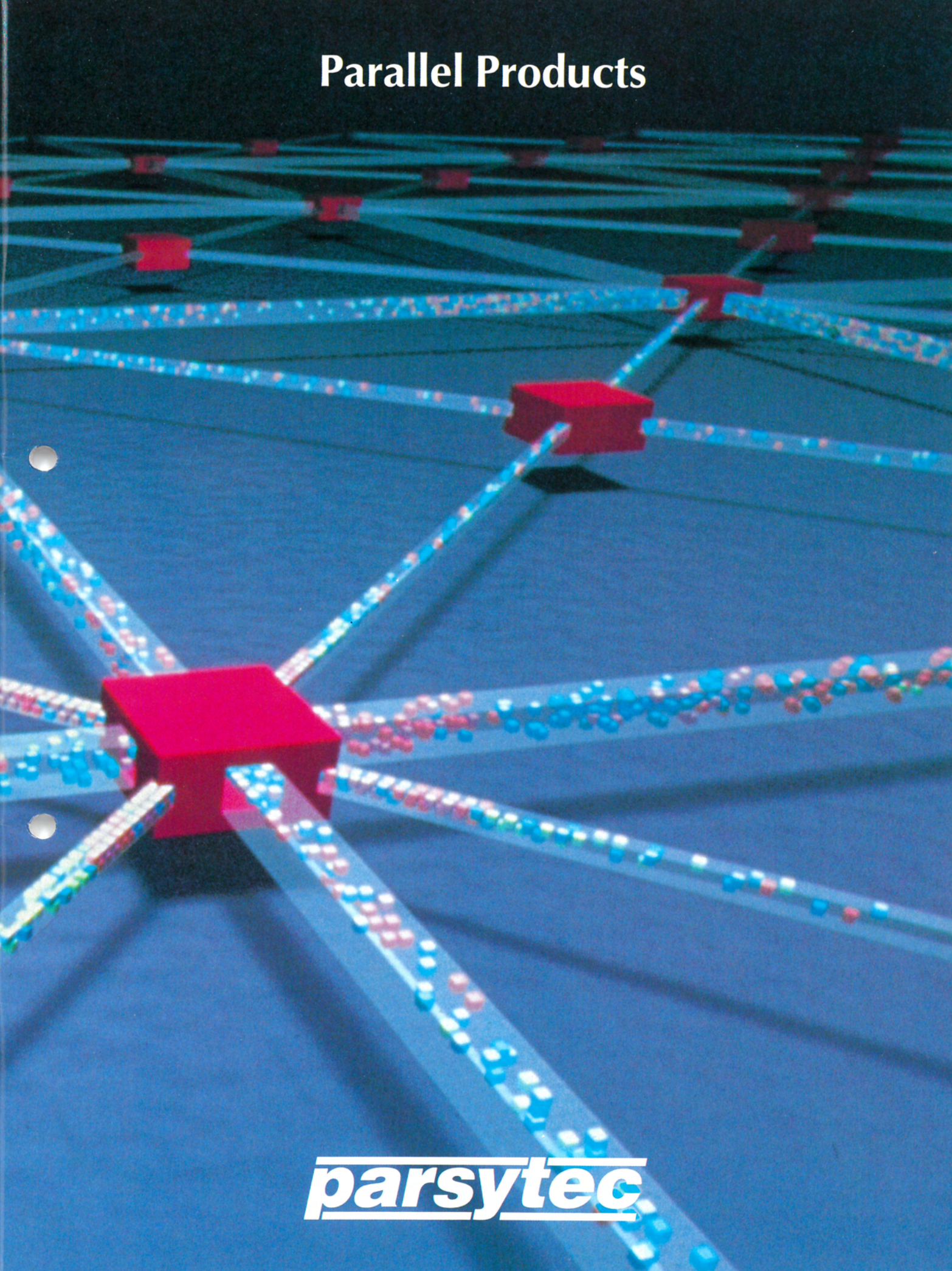
# Parallel Products



parsytec

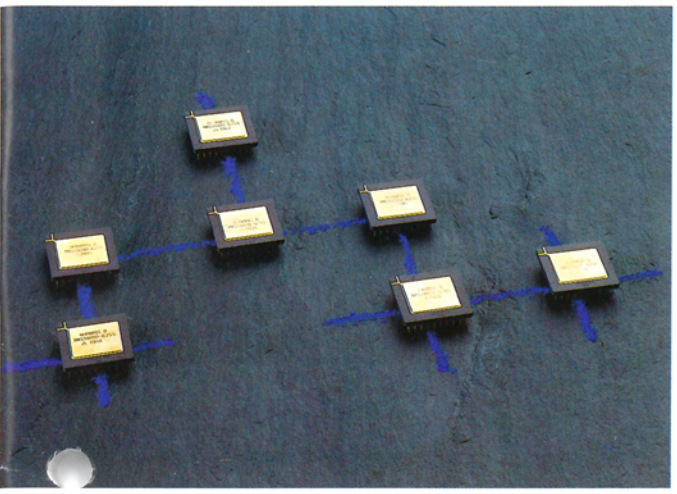
# Contents





Front Cover: Scene from the movie "Siemens: Netzknoten 2000"

# Introduction



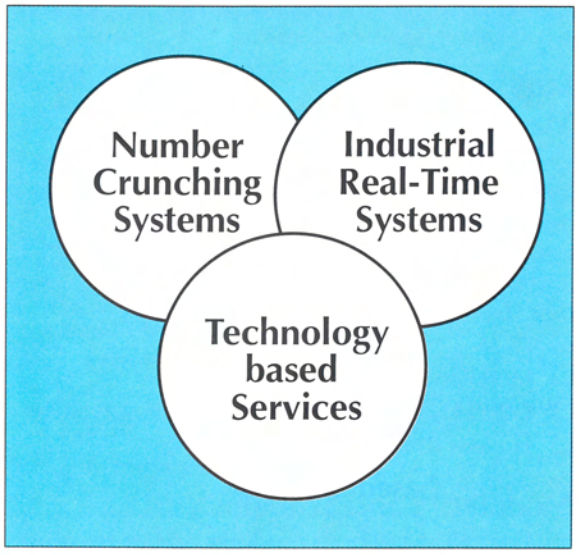
Over recent years the demand for high speed computers has risen dramatically. With this growth in demand has come an increase in performance. Although single-processor computer performance has grown rapidly in the past, this rate of growth cannot be sustained. The speed of light and the laws of quantum

mechanics impose fundamental physical limits which cannot be breached. Economic constraints are equally significant; processor, bus and memory technologies are steadily becoming more exotic and expensive in an attempt to make them faster. A different and more cost effective way to increase processing power is to construct multiple-processor computers.

The Inmos Transputer is a high performance, 32-bit, RISC processor which supports parallelism at the hardware level. A key feature of this processor is its communication links to other Transputers. These links have direct access to memory, independently of the central processor. A Transputer can simultaneously communicate and perform calculations in a balanced way. This enables the efficient sharing of a single computational task amongst several processors, communicating via their links. As the computational demands of an application increase, the processing power of the system can be increased by adding more Transputers, simply and cost effectively.

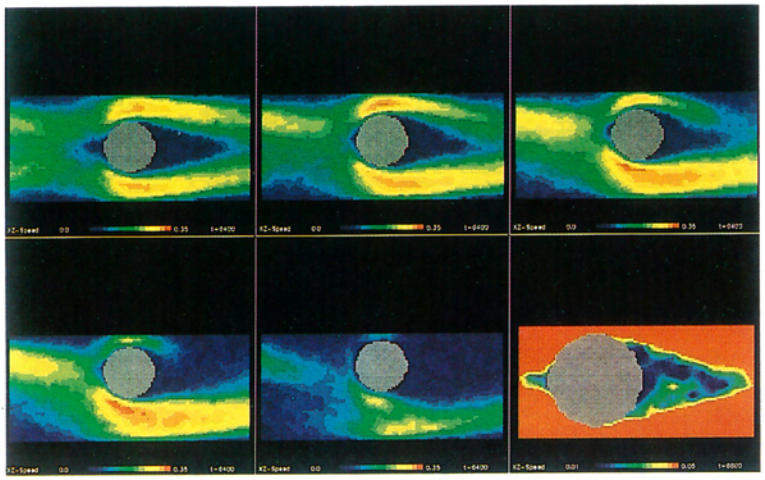
Founded in 1985, Parsytec was one of the first companies to turn the Transputer concept into a working product and is now the market leader in parallel systems. A long term commitment to the use of current and successive generations of Transputers ensures a coherent hardware migration path with the confidence of software portability across our range of systems. Parsytec has more than 600 installations in over 20 countries, supporting a wide range of projects from computationally intensive applications to real-time industrial control systems. The support of these projects has given us unrivalled experience in the application of parallel processing techniques in a wide range of areas.

To meet a rapidly growing demand for sales, service and technical support, subsidiaries, offering technology based services, have been established in major markets including Germany, the USA and Great Britain. These organisations have a direct involvement in an increasing number of customer projects and applications. Furthermore, distributors give local support in most European countries, the Far East, Australia and Africa.



# Number Crunching Systems

Numerically intensive applications such as Computational Fluid Dynamics, or scientific and engineering simulations, often place severe demands on computer systems. Parsytec systems meet these demands by providing cost effective performance in a user-friendly environment, offering standard languages and a flexible approach to processor topology. Frequently these types of applications involve the development of new algorithms. To support such activities, our systems provide a high degree of reconfigurablity. A multiuser capabability enables the easy, effective and secure shared use of our systems.



3D Flow through Nybolt Spacer, KLSA Amsterdam

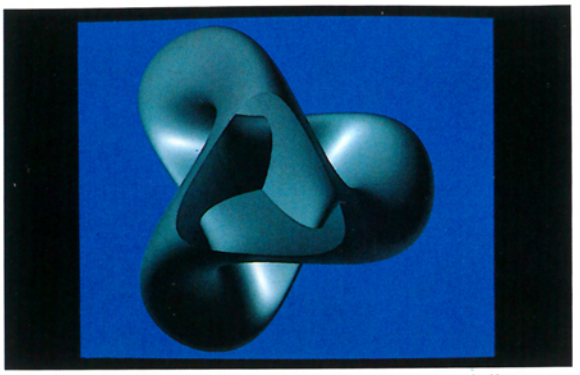
## Multiple Virtual Machine Architecture (MVMA)

To meet these requirements, we have developed the Multiple Virtual Machine Architecture (MVMA) which is the basis for our number crunching systems: the MultiCluster-2 series and the SuperCluster series. The MVMA embodies the following properties:

- ❑ **Modularity and Scalability**
- ❑ **Consistency and Compatibility across systems**
- ❑ **Highest Reliability**

## Modularity and Scalability

The MVMA is both modular and open, allowing system integrators the freedom and flexibility to configure the optimum processor and I/O structure for their application. The scalable properties of the Transputer allow the user to achieve potentially any performance level by adding more processors.



Visualization in Mathem. Sciences, IWR Heidelberg

However, a modular, scalable system requires features that transcend the number of processors. These features include: reconfiguration support, which allows software to control the configuration of any processor network in a system, regardless of the size; multiuser capabilities, which enable a parallel computer to be shared as a processor pool without system overhead; reliability, which is ensured by features such as error protected memory and is an essential quality in a system designed to be scalable within several orders of magnitude of performance; and integrability into existing and future environments, such as workstations or LANs.

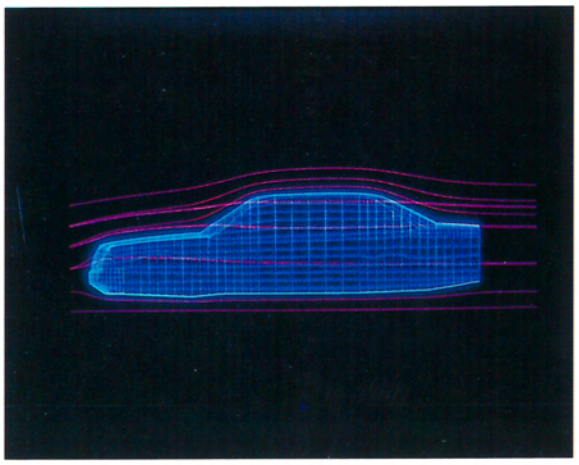
Simply adding processors is only one aspect of expanding system performance. To achieve true scalability, modular systems require that the appropriate hardware and software infrastructure is embedded in the system design to provide full functionality over a wide range of performance levels. Parsytec systems have achieved this quality of scalability with their Multiple Virtual Machine Architecture.

## Consistency and Compatibility

A product line with a consistent approach to hardware design and with a software environment which ensures compatibility, allows a simple entry into parallel processing having many upgrade options.

## Highest Reliability

Many Parsytec systems are used in industrial applications where very high reliability is of the utmost importance. To ensure that all our systems meet the most demanding specifications, only the most advanced and most reliable components are used in their construction. The Parsytec UniLink standard allows long distance communication in hostile environments with a high degree of noise immunity.



Aerodynamic Simulation

Error Detection and Correction (EDC) memory subsystems are available. EDC logic automatically checks RAM, correcting single-bit errors when necessary. This is an important advantage in numerically intensive computations where resetting and restarting calculations is time consuming and costly. Further fault tolerance is provided by the Helios operating system which adds to the overall high reliability of Parsytec products.

The Multiple Virtual Machine Architecture is realised as a Physical Machine and a Virtual Machine.

## The Physical Machine

The Physical Machine (PM) comprises integrated front-end and back-end computers. The front-end workstation provides a familiar environment running standard software packages, operating systems, languages and tools, and supports medium speed access to peripherals. Front-ends supported include Sun, PC, PS/2, VAX, and Macintosh systems. Additional front-ends are supported via Ethernet, TCP/IP and FDDI.

The back-end comprises specific Parsytec hardware, with an unlimited capability for expansion, using processor modules or special I/O boards, which give high speed access to peripheral devices. The processors in the Parsytec system can be connected in a flexible manner using software controlled Network Configuration Units (NCUs).

## The Virtual Machine

A Virtual Machine (VM) consists of a portion of a PM which has the same capabilities as a whole machine. The VM of a user comprises a number of processors allocated to that user. This VM might be all the processors in the machine or only a small fraction of them. For these processors, the user defines an appropriate

topology and the software he wants to run. The NCUs guarantee that each user is physically independent of all other users by partitioning the machine. This ensures the highest possible security for individual applications.

For example, one user may run a numerically intensive application continuously for several days within one partition, whilst others are developing and debugging their own programs within other partitions. All user partitions are completely independent and may run totally different programming environments and languages.

The Network Configuration Manager software (NCM) guarantees simple, democratic and dynamic access to the pool of processors. All users have an equal priority in requesting processors from the NCM. Allocation of resources can occur during normal operation with users claiming and freeing processors as required.

### Application Examples

- ❑ **Computational Fluid Dynamics**
- ❑ **Finite Element Methods**
- ❑ **Monte Carlo Simulation**
- ❑ **Combinatorial Optimisation**
- ❑ **Neural Networks**
- ❑ **Molecular Modelling**
- ❑ **Computational Physics**
- ❑ **Science and Statistics**
- ❑ **Mathematical Simulation**
- ❑ **Aerodynamic Simulation**

# Industrial Real-Time Systems

Real-time applications need a coherent family of products providing high speed data communications across a wide range of applications.

A common requirement is to integrate all parts of a complex factory in such a way, that the whole system behaves as a homogeneous entity.

In order to satisfy this requirement, it must be possible to design and implement local subsystems in a structured manner, using a top-down methodology. Examples of this include supervisory control and data acquisition systems running under real-time constraints in areas such as process control, automation, materials handling and production.

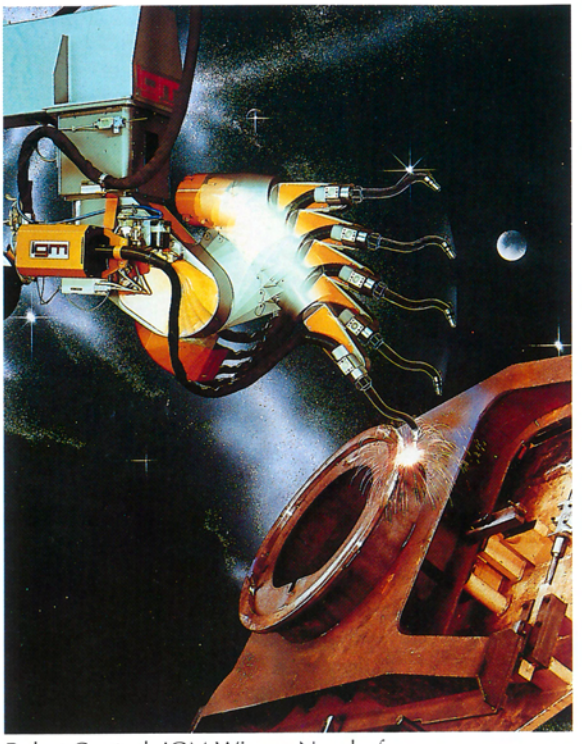
## Application Examples

- ❑ Pattern Recognition
- ❑ Robot Control
- ❑ Data Acquisition
- ❑ Image Processing
- ❑ Automation
- ❑ Manufacturing Control
- ❑ Quality Control

In industrial real-time control applications, Parsytec's Transputer systems provide the combined benefits of parallel processing, scalability, fault tolerance and reliable recovery from error. The Transputer's rapid response to external interrupts and fast task switching ensure effective real-time performance. The modularity, provided by a coherent family of products, enables the integration of local systems as a structured part of a complex, yet homogeneous, entity.

Parsytec systems are used in industrial applications where very high reliability is of the utmost importance. To ensure that all our systems meet the most demanding specifications, only the most advanced and most reliable components are used in their construction.


Car Performance Simulation, VW Wolfsburg




Robot Control, IGM Wiener Neudorf

Long distance link interconnection is provided by the UniLink communication standard which uses a differential RS-422 interface for high noise immunity. This enables the construction and operation of physically separated distributed process control systems where individual devices can communicate by converting bus signals into UniLink communications. Such bus bridges exist for PCs and Micro Channel, VME, NuBus, Sun, and VAX systems. The UniLink reset mechanism allows any Transputer node in a system to be reset independently. Any failure can be isolated and action taken to recover without affecting the operation of the rest of the system.

In embedded applications, UniLink connections can be hard-wired using inexpensive fixed cables. In a harsh industrial environment, interconnection reliability and performance are ensured through the use of high quality components, cables and power supplies. All Parsytec boards and systems are plug compatible and can be connected to standard Inmos links. Connection to third party boards, conforming to industry standards, such as Ethernet and RS422, is comprehensively supported.

# Parallel Systems

## A Continuous Range of Solutions

From dedicated simple systems right up to powerful supercomputers, serving many users, there is an appropriate Parsytec parallel solution, which builds on existing hardware and software.


## MultiCluster-1 Series for up to 30 Processors

The MultiCluster-1 can be used either as an expansion to existing inworkstation modules, or as a standalone target system. With a topology, configurable to suit the application, the single-height MultiCluster-1 rack can house any combination of UniLink expansion modules.

## MultiCluster-2 Series from 16 to 64 Processors

The MultiCluster-2 series, with its Multiple Virtual Machine Architecture, is designed for several users requiring support for software reconfiguration of topology, or for single users requiring greater power and flexibility. It provides a framework for reconfigurable systems with up to 64 Transputers.

## SuperCluster Series from 64 to 1000 Processors

The SuperCluster has been designed as a reconfigurable, Transputer array capable of comprising up to 1000 processors; a design objective was its use in massively parallel supercomputing applications. Its Multiple Virtual Machine Architecture offers simple modular expansion.It has totally autonomous multiuser subnets configurable under software control, and the option of extended fault-tolerant features for critical applications.

The MultiCluster-1, MultiCluster-2 and SuperCluster offer a continuous and consistent upgrade path. As more processing power or functionality is required, the user can add to existing Parsytec modules.

## Easy Transition to Higher Performance

Due to the modular structure, it is very simple to expand a system. Processing power can be increased by the further addition of processing modules. Reconfigurability and multiuser capabilities can be achieved through the incorporation of Network Configuration Units with existing processing modules. An example upgrade path might be:

1) Start with a UniLink Multi-Transputer module with a PC-bus adapter inside an IBM-compatible PC/AT.

2) Connect the PC to further UniLink modules housed in a MultiCluster-1 expansion unit via a UniLink cable.

3) Replace the MultiCluster-1 housing with a MultiCluster-2, retaining existing UniLink modules. Software controlled reconfiguration of up to 64 processors is supported.

4) Transfer your existing application directly to a SuperCluster when it requires processing power beyond 64 Transputers. Existing UniLink modules can be integrated into the SuperCluster, providing host interfaces, Ethernet LAN and other I/O functions.

# MultiCluster-1 Series

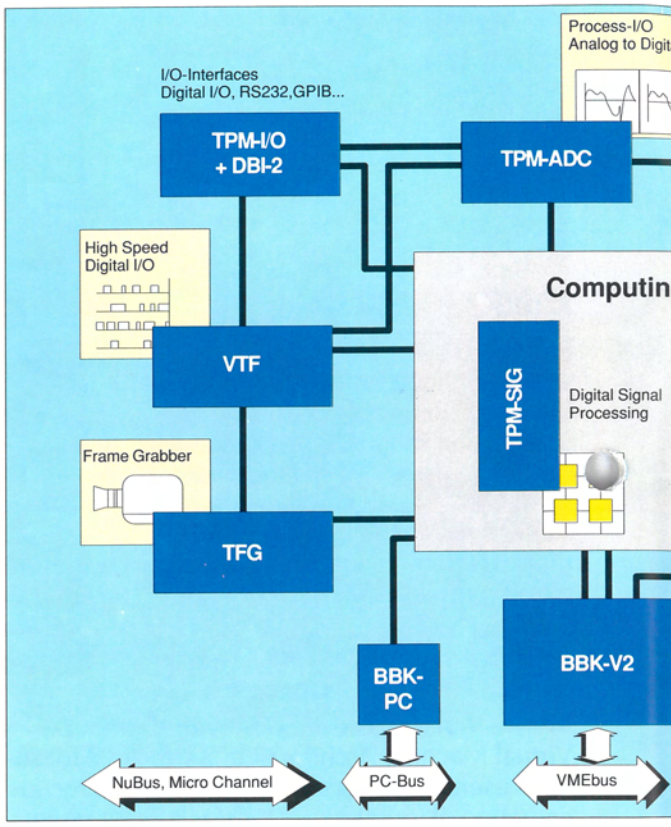
The MultiCluster-1 is a racked system supporting the reconfigurable interconnection of Parsytec modules. This allows the user to construct a particular system, tailored to specific requirements such as number of processors, link topology, amount of memory and I/O configuration. Transputers may be added incrementally as computational needs increase.

The MultiCluster-1 can house the complete range of UniLink modules, whilst the user's choice of host development system or front-end is readily accommodated via interface modules.

## Expansion Unit

Up to 15 modules from the Parsytec range can be held in the MultiCluster-1 expansion rack. The required processor topology can be configured using UniLink connections fed through the MultiCluster backplane. Four external sockets provide UniLink interconnection, including reset lines.

For systems with graphics or video modules (for example the graphics display subsystems, or the Transputer frame grabber), standard BNC connectors are provided on the rear of the unit.



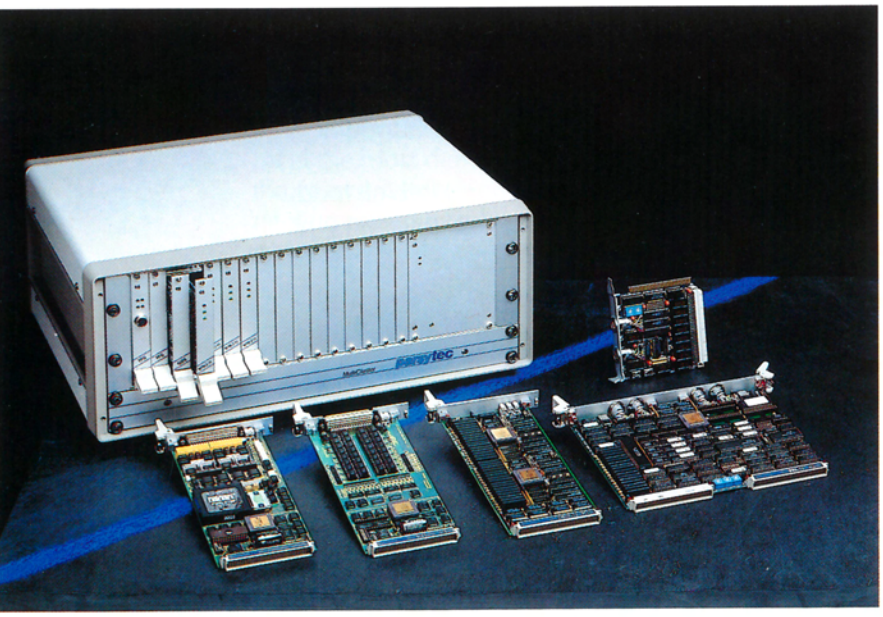

## System Unit

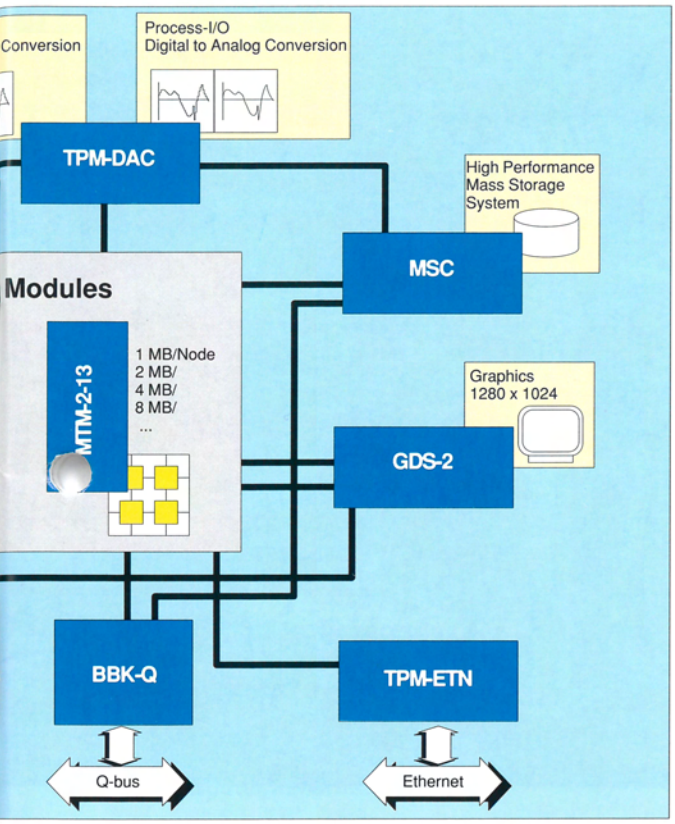
The MultiCluster-1 system unit is identical to the expansion unit, but five of the slots are occupied by an IOS-1 control unit, a floppy and a hard disk drive.

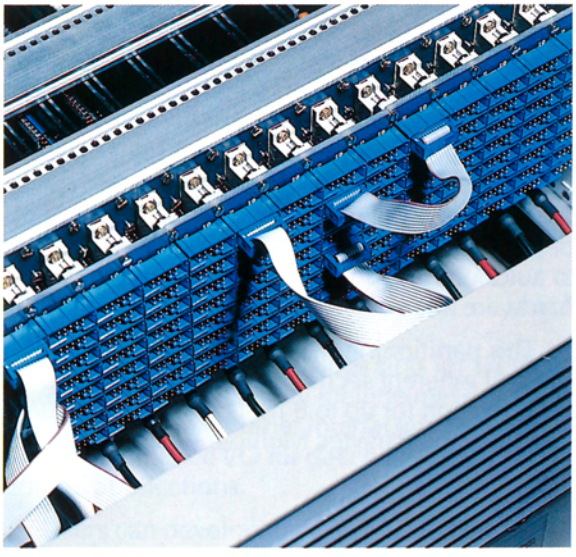
The system unit is well suited for hosted developments using software tools, or for applications.

Standalone applications are supported by the IOS-1 controller module. This integrates mass storage control and terminal interfacing.

Through the IOS-1, a VT100 or VT220 terminal can be connected directly to the system unit. This provides a standalone development workstation or run time front-end for parallel applications.





## The PC Connection

Parsytec provides a unique upgrade route for PC-based Transputer systems. In a typical application, initial development work can be carried out using the BBK-PC adapter attached to an appropriate Parsytec module which occupies a single PC expansion slot.


The demands of some applications may be so great that the PC-based solution is no longer appropriate. This may occur because the PC has insufficient slots, or an inadequate power supply. It may also be that industrial packaging, or standalone operation, is required. In these cases, Parsytec modules can be installed in a MultiCluster rack.

Alternatively, the parallel system in the PC may be expanded simply by connecting the BBK-PC UniLink port to a Parsytec module in a MultiCluster expansion unit.

The insets illustrate the wide range of modules and the easy interconnection scheme provided by Parsytec.

3D Reconstruction of Tomographic Images, GHS Siegen

# MultiCluster-2 Series

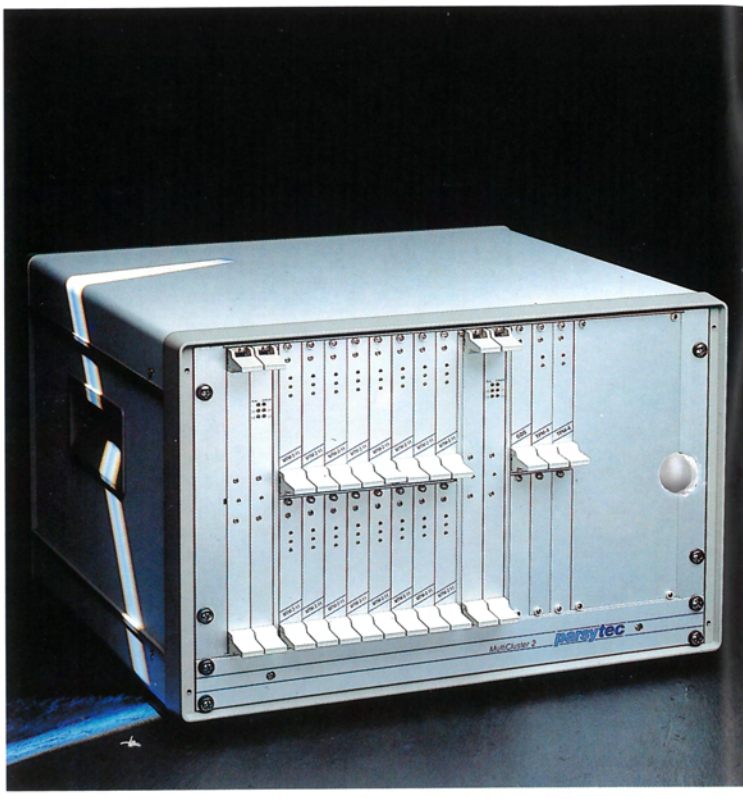
The Multiple Virtual Machine Architecture (MVMA) of the MultiCluster-2 allows users to configure dynamically up to 32 Transputers, under software control, within one basic unit. The system offers a flexible choice of performance (number of processors, processor speed), memory, mass storage, I/O functionality and processor reconfigurability, according to the needs of the application.

## System Topology under Software Control

The system topology can be reconfigured dynamically under software control, using Network Configuration Units (NCUs). Control and communication between the various modules is achieved by passing messages through Transputer links. Since no hard-wired central control bus is involved, there are no limits and there is the maximum freedom in choice of topology.

## Modular Expansion

The MultiCluster-2's MVMA allows initially small systems to be enlarged in a modular and flexible way, thus giving the capability for greatly enhancing their performance and functionality.



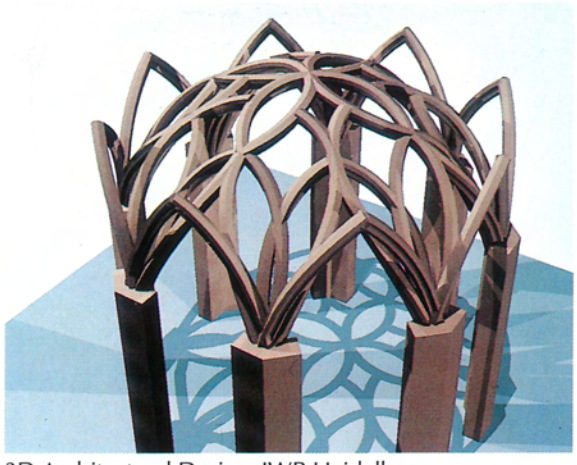

Even when combining two MultiCluster-2 systems, the reconfigurability and multiuser capabilities of the MVMA are retained.

System functionality is further extended through the wide range of Parsytec I/O modules, which allow the user to connect Transputer systems to a wide range of peripheral devices.

## Multiuser Capability

The MVMA of the MultiCluster-2 allows physical partitioning of the Transputer array into autonomous subnets, each with individual hardware and software resources.

This partitioning, with fault-tolerant properties and inherent security, ensures true multiuser operation for up to 8 users. This is a unique feature of the Parsytec Multiple Virtual Machine Architecture.



3D Architectural Design, IWR Heidelberg

## Each user can individually:

- ❑ **Use just as much processing power as required**
- ❑ **Select optimum processor topology for the task**
- ❑ **Choose the type of front-end workstation to be used, and**
- ❑ **Choose the system software to run on the Transputer network.**

## System Configuration

The MultiCluster-2 comprises three functional units: the processing subsystem, the I/O subsystem and the configuration control subsystem.

### Processing Subsystem

The MultiCluster-2 provides 16 slots for Parsytec modules such as the MTM-2 and supports up to 32 Transputer nodes. One or two processors per module and between 1 and 32 MBytes DRAM per node are available.

### I/O Subsystem

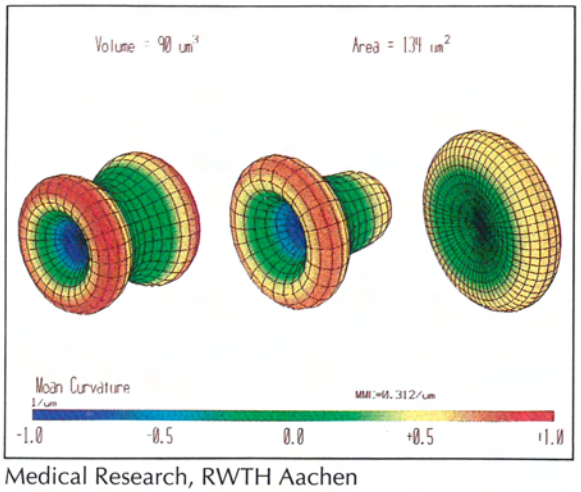
The I/O subsystem provides slots for six Parsytec modules which may include mass storage, graphics and Ethernet interfaces as well as high-performance I/O for data acquisition and control applications.

Users can develop their own special-purpose interfaces for integration with the I/O sub-system using Parsytec prototyping modules.

### Configuration Control Subsystem

Two slots for Network Configuration Units (NCUs) are provided. The number of NCUs required depends upon the number of processors in the system and the degree of reconfigurability required by the application.

The NCU design is based on the use of the Inmos cross-bar switch, the C004. This design provides an advanced switching strategy which causes the propagation delay for a point-to-point connection through the NCU to be no more than that due to a single C004 chip. Each NCU can switch 96 UniLinks and their associated reset signals.

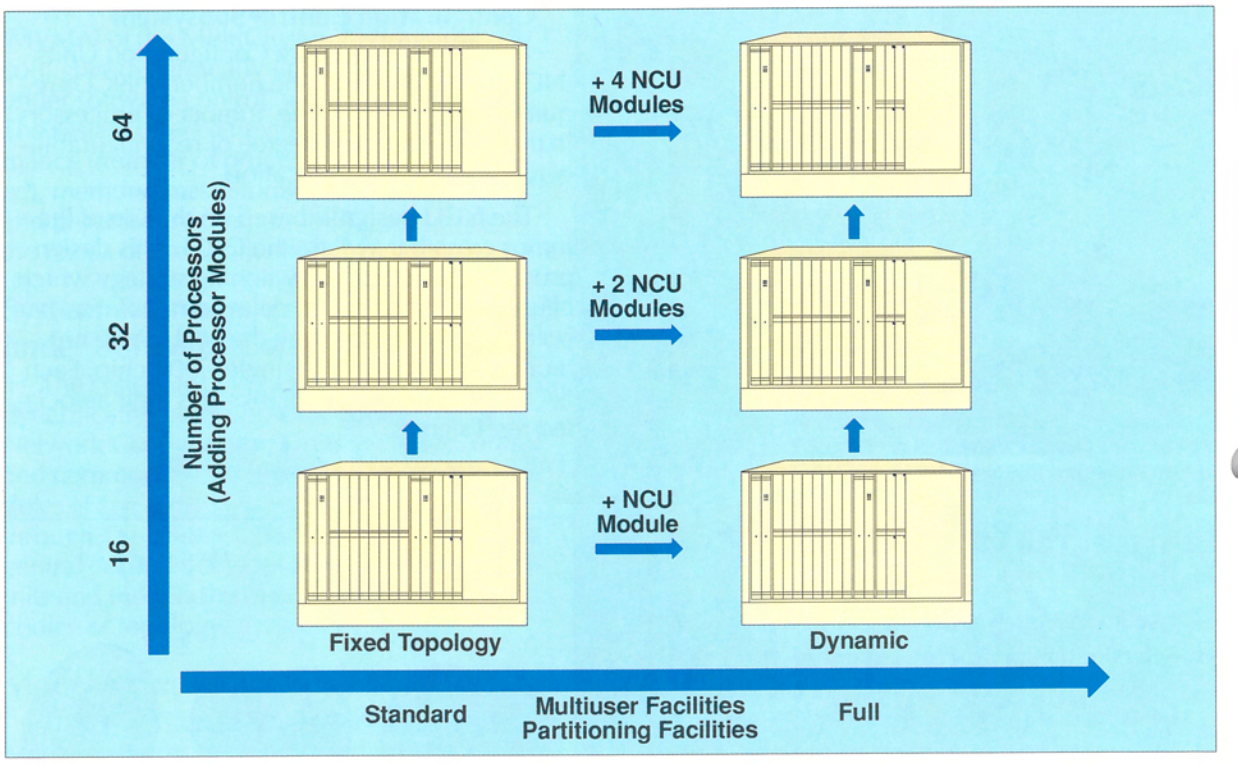



Medical Research, RWTH Aachen

## UniLink Connections

The system unit offers eight external UniLink connectors. These may be used to connect to external Transputers.

Additionally, links are provided to connect two MultiCluster-2 units to form a 64-processor system.




Upgrade Path MultiCluster-2

## Reconfigurability

Different system configurations are available, which can be easily upgraded by adding additional processor modules or NCUs. Two types of reconfigurability can be defined:

### Fixed Topology

In this case no NCUs are used. The node topology is configured by special boards which are plugged into the NCU slots of the system. This offers the user a choice of standard topologies such as mesh or tree structures.

### Full Reconfigurability and Physical Partitioning

To achieve maximal flexibility, the system may have one NCU for up to 16 Transputers and two NCUs for between 16 and 32 processors. In the former case, the single NCU provides a full cross-bar function between all links in the Transputer network.

For configurations with more than 16 processors the links are divided into even and odd groups, with a separate NCU provided for each group.

In both cases the MultiCluster-2 can be fully reconfigured and physically partitioned. With two NCUs it is possible to combine two MultiCluster-2 units to produce systems with up to 64 Transputers. Reconfigurability and multiuser capability are supported by the MultiCluster-2 version of the Network Configuration Manager software.

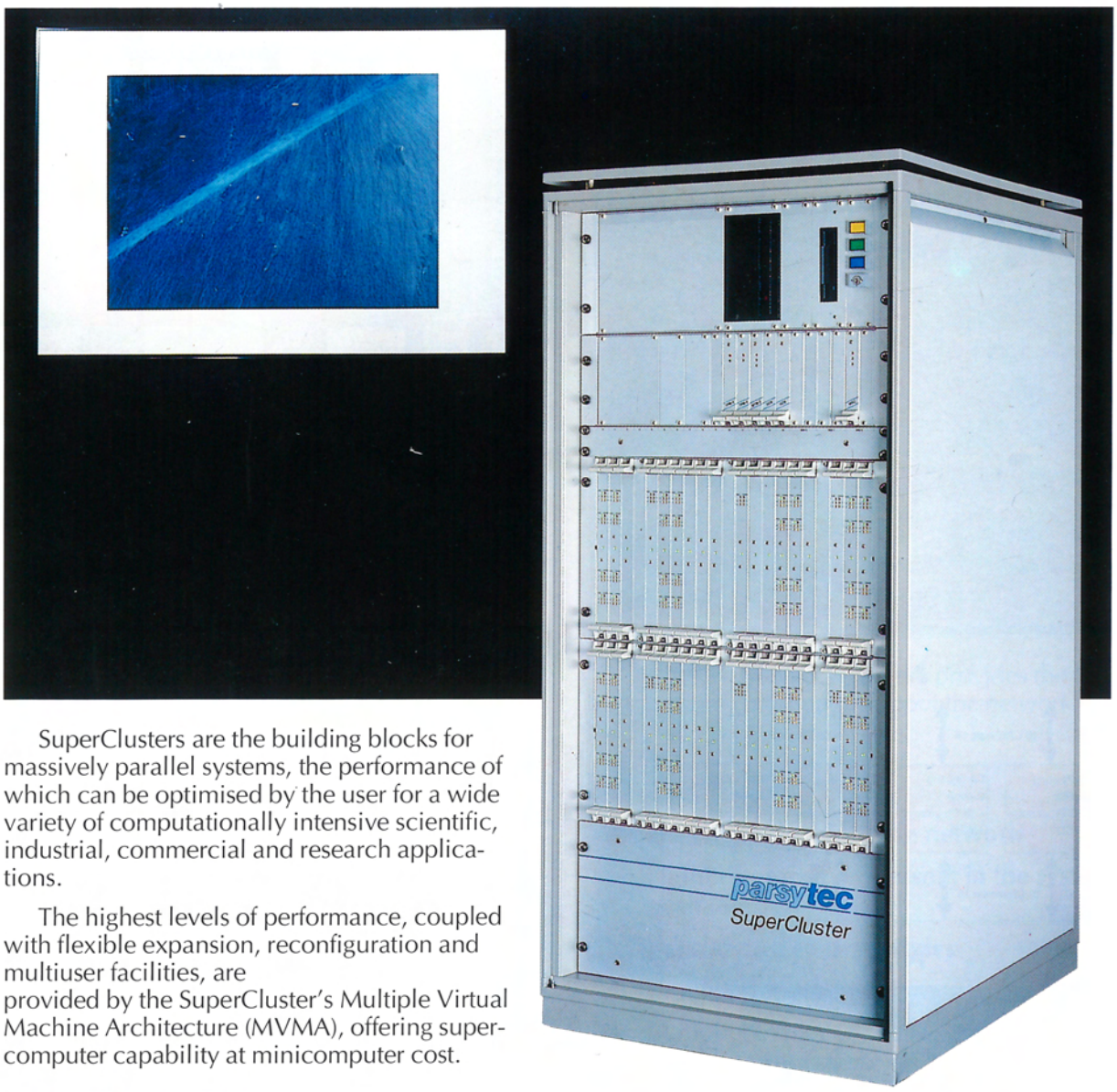
## Host Integration via Bus Bridges or Ethernet

Different workstations and host environments can share the resources of the same MultiCluster-2, each working with its own subnet, physically autonomous yet dynamically reconfigurable. This can be achieved either by using bus bridges or the Ethernet interface provided by the TPM-ETN module.

## UniLink I/O Expansion

As with MultiCluster-1, Parsytec modules provide the MultiCluster-2 system with a full range of expansion capabilities, including Ethernet LANs, SCSI, graphics, serial, parallel and industrial I/O interfaces.

# SuperCluster Series




SuperClusters are the building blocks for massively parallel systems, the performance of which can be optimised by the user for a wide variety of computationally intensive scientific, industrial, commercial and research applications.

The highest levels of performance, coupled with flexible expansion, reconfiguration and multiuser facilities, are provided by the SuperCluster's Multiple Virtual Machine Architecture (MVMA), offering supercomputer capability at minicomputer cost.

## System Architecture

The MVMA of the SuperCluster has a hierarchical and cluster-based design. The lowest level of the system is a computing cluster, which consists of 16 processors. These can be configured to any possible topology by means of a Network Configuration Unit (NCU).

The next level is a pair of clusters connected by an additional NCU, which appear externally as a cluster.

Thus four computing clusters with two additional NCUs form the basic SuperCluster unit, the Model 64. Multiple units again form larger systems. The Model 256 for example has 16 computing clusters which are linked through 12 additional NCUs.

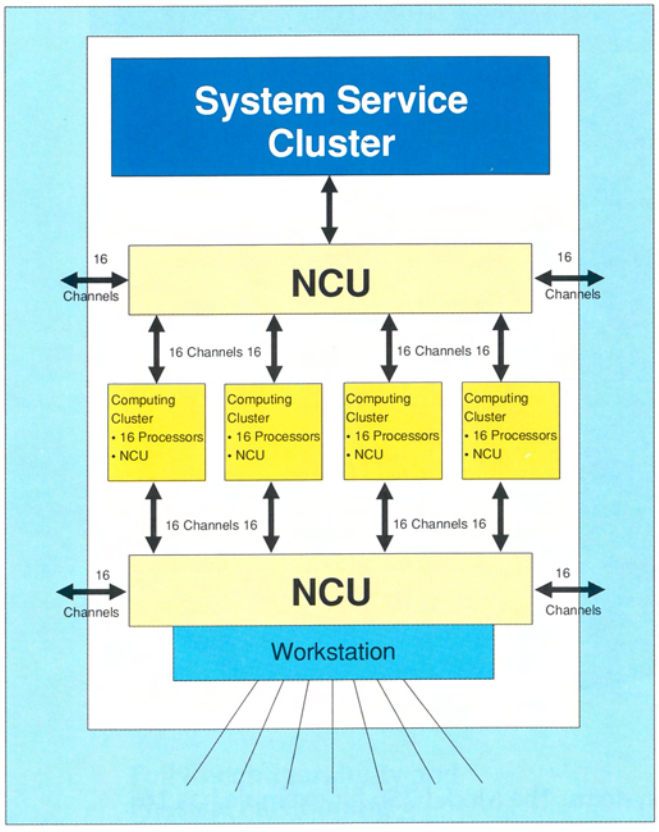
This design provides modular expandability and may incorporate System Services Clusters for parallel mass storage and application-specific interfaces, all of which have the same communications scheme as the application processors.

## Fault Tolerance

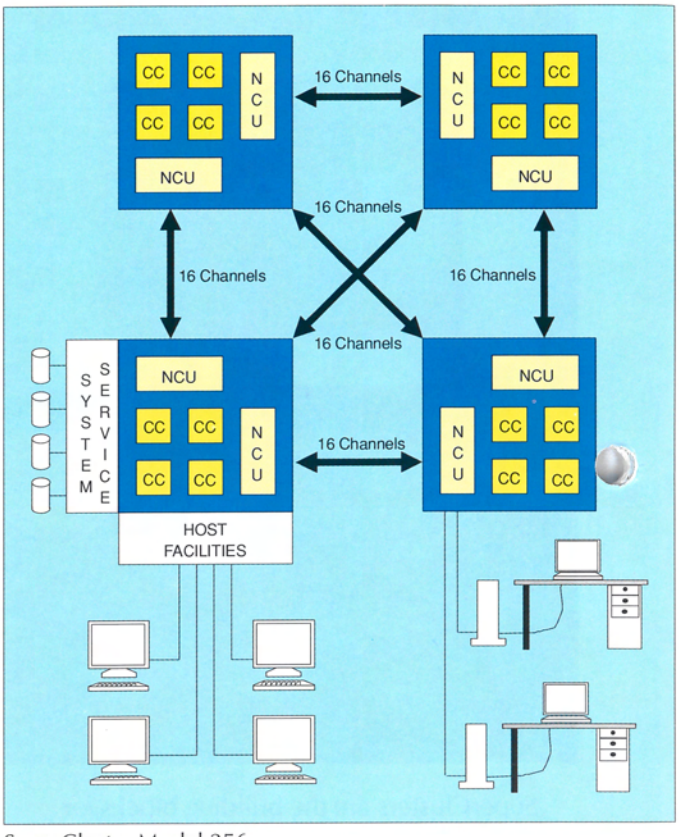
High performance systems, such as the SuperCluster, frequently have to perform complex calculations taking hours or even days to complete.

Such computations may be compromised by errors in the RAM. When system RAM is measured in Gigabytes, the statistical probability of a single-bit error becomes high.

For this reason, the SuperCluster is supplied with error detection and correction memory units, which automatically check and correct bit errors.




System Architecture




SuperCluster Model 256

## Expansion

Each 64-processor SuperCluster has 64 links available for external connection. In this way SuperClusters may be cascaded to build massively parallel systems.

## Reconfigurable System Topology

The SuperCluster uses dedicated hardware, NCUs, for dynamic reconfiguration of the processor topology under software control. As described in the above MultiCluster-2 section, the NCU is constructed from the Inmos C004 crossbar switch and can switch 96 UniLinks.

## Network Configuration Manager

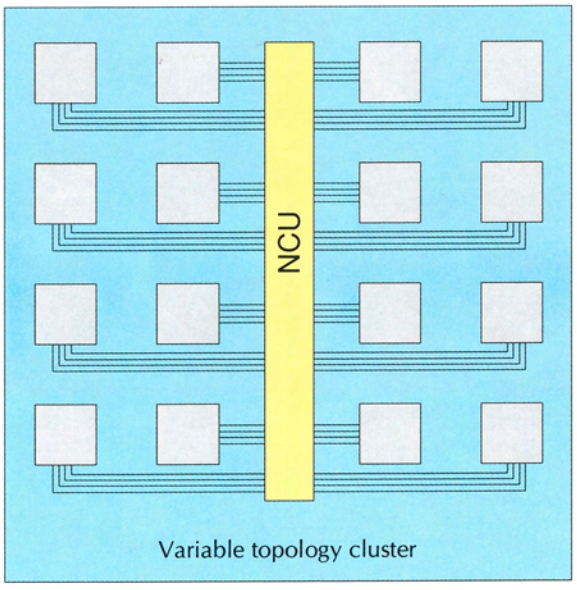
The Network Configuration Manager (NCM) software controls the NCUs and responds to user configuration requests. An important task of the NCM is to establish a partition on which to run user programs.

The SuperCluster's Multiple Virtual Machine Architecture provides complete physical as well as software separation of processor partitions.

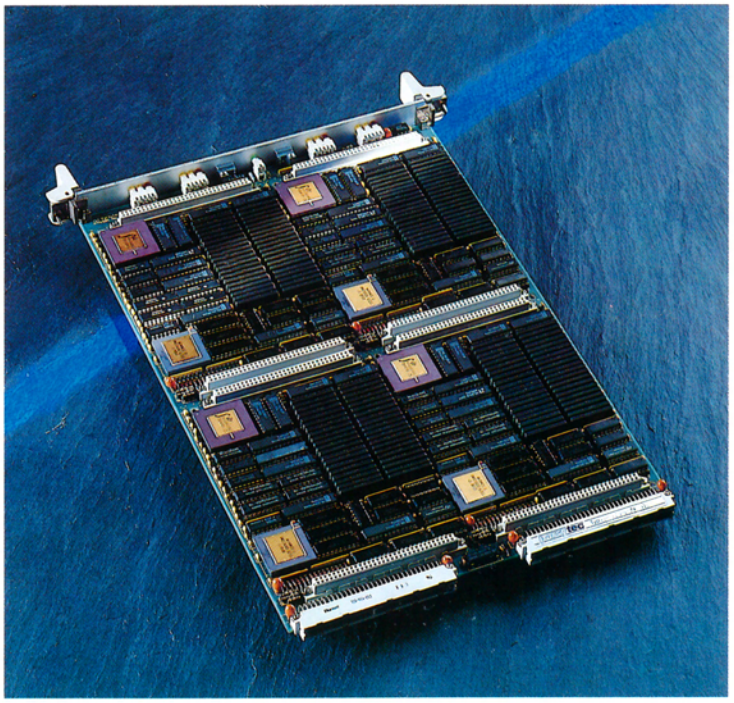
For instance, individual users can reliably and securely reset their processor partition without affecting other system users. This provides the possibility of having different users running several different operating systems.

Resource allocation is simply performed by specifying a number of processors and their interconnection topology.

The necessary information for this is contained in a configuration file defined by the user. Allocation and configuration is automatically performed prior to loading the network.



Variable topology cluster



The NCM STATUS function provides the user with key information about the network, such as:

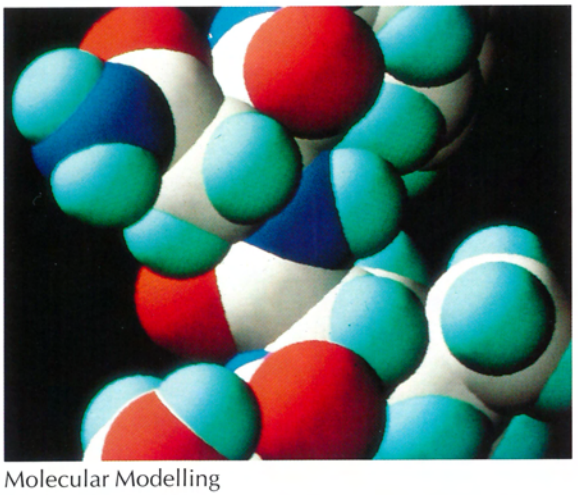
- ❑ **User ID**
- ❑ **User's channel into the network**
- ❑ **Number of free processors in the system available**
- ❑ **Special processor modules**
- ❑ **Processor usage by all users**
- ❑ **Mapping of user processing numbers and physical processors**
- ❑ **Connection information about the switched NCU channels**
- ❑ **Logical and physical representation of user's topology**
- ❑ **Furthermore the system manager may reset user networks (if necessary) and perform processor checks.**

## Multiuser Access

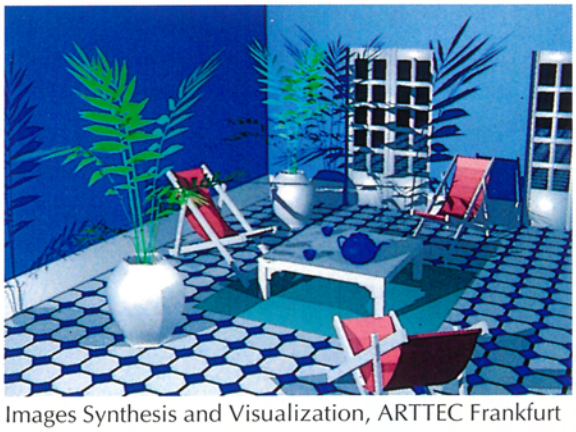
As many as eight workstations can simultaneously access a 64-processor SuperCluster, with each user having his own partition.

The operating system and the development environment can be completely different between users. For example, one user may run a numerically intensive application continuously for several days within one partition, whilst others are developing and debugging their own programs within other partitions. All user partitions are completely independent and may run totally different programming environments and languages.

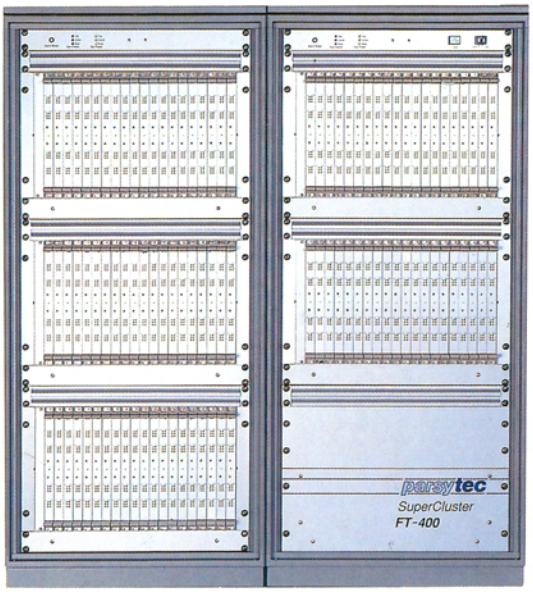
The Network Configuration Manager automatically creates partitions according to the users' requested topology.



Molecular Modelling



Images Synthesis and Visualization, ARTTEC Frankfurt

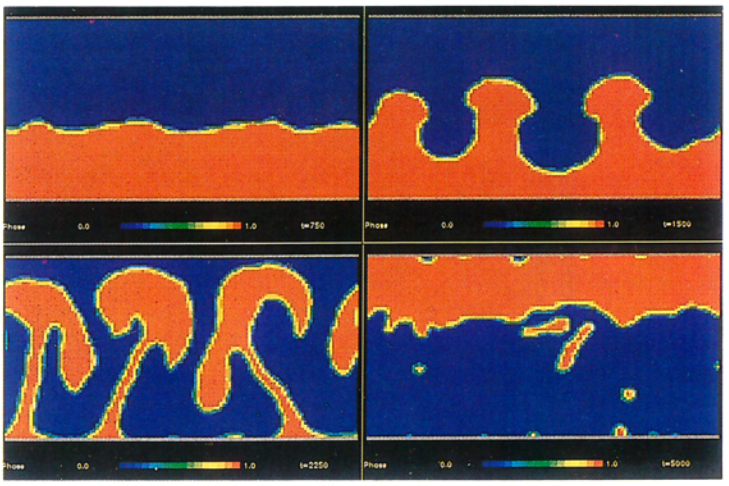



## Remote Access

Software developed on smaller Parsytec systems can be downloaded remotely for execution to the SuperCluster via a UniLink connection or over an Ethernet LAN.

Remote access also enables the use of smaller Transputer networks, for example a MultiCluster-1, to provide data preprocessing or intelligent I/O to the SuperCluster pool.

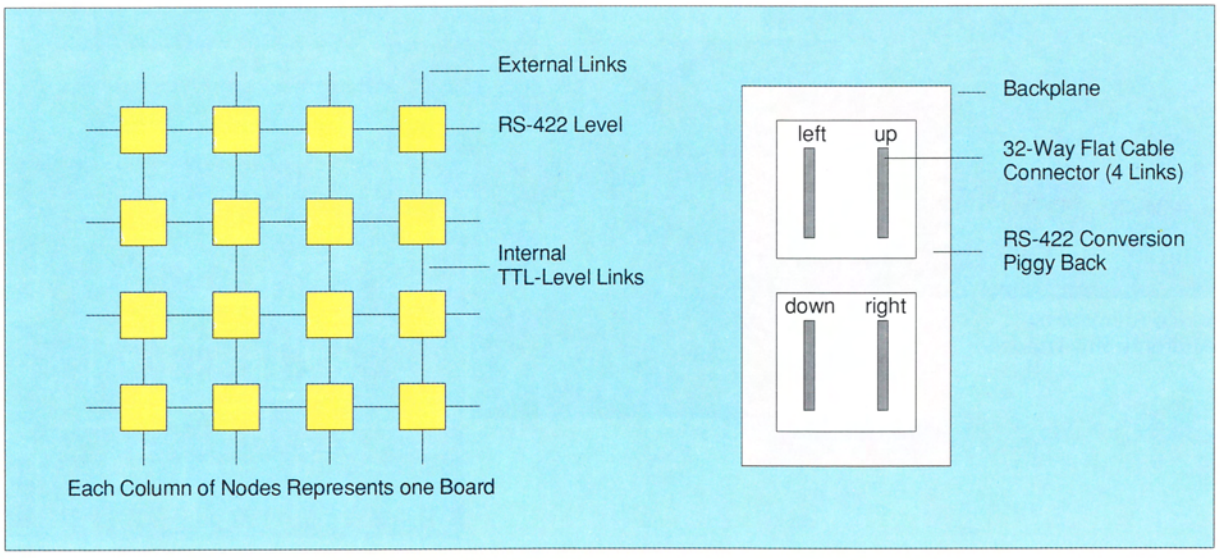
As all Parsytec modules conform to the UniLink RS-422 standard for serial communication, data can be transfered up to 30m. Furthermore, high data rates are possible. For example, 32 UniLinks deliver around 50 MByte/s.



A Rayleigh-Taylor Instability, KSLA Amsterdam

## Ethernet Interface

Placing a TPM-ETN Parsytec module in the System Services Cluster enables remote access to the SuperCluster through Ethernet. This makes it possible to add a Transputer pool to a LAN, or to provide remote facilities for a SuperCluster. All popular media access methods are supported.

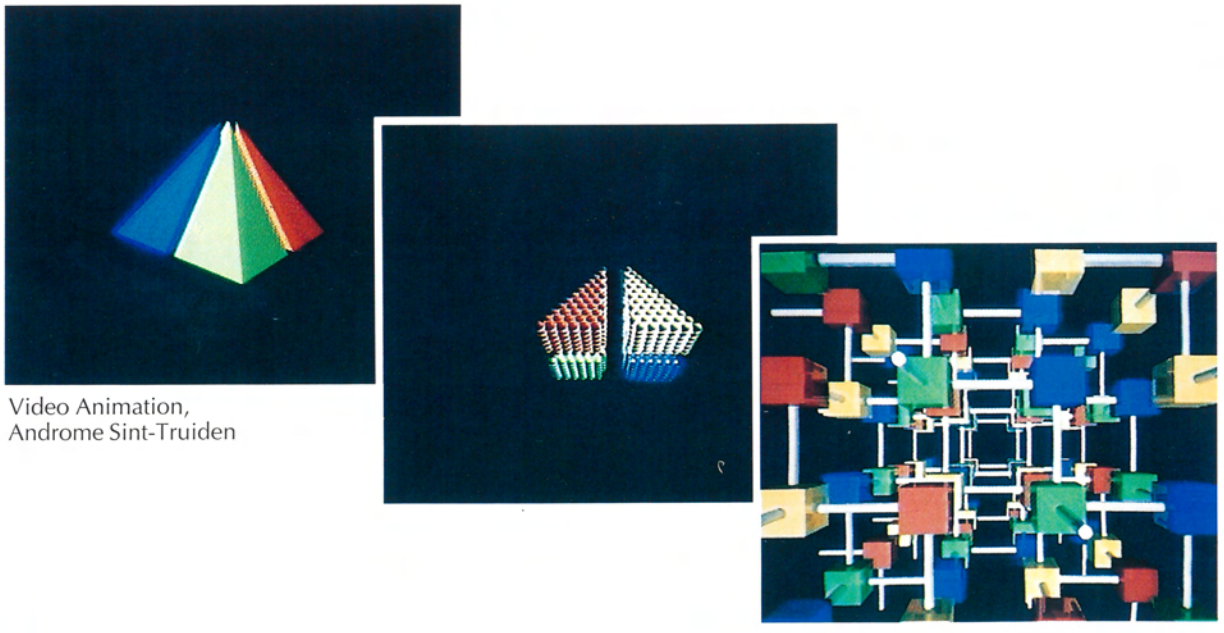


# Summary

| System Type | Max. No. of Processors | Max. Memory per Node | Reconfiguration | | | Dynamic Multiuser Capability |
|---|---|---|---|---|---|---|
| | | | Fixed | Cable | Dynamic | |
| MultiCluster-1 | 20 | 32 MB | | X | | |
| MultiCluster-XP | 30 | 32 MB | | X | | |
| MultiCluster-2 | | | | | | |
| -16 FT | 16 | 32 MB | X | | | |
| -16 NCU | 16 | 32 MB | | | X | X |
| -32 FT | 32 | 8 MB | X | | | |
| -32-2 NCU | 32 | 8 MB | | | X | X |
| -64-4 NCU | 64 | 8 MB | | | X | X |
| SuperCluster-64 | 64 | 16 MB | | | X | X |
| SuperCluster-128 | 128 | 16 MB | | | X | X |
| SuperCluster-256 | 256 | 16 MB | | | X | X |
| • | • | • | | | • | • |
| • | • | • | | | • | • |
| • | • | • | | | • | • |

XP - Expansion Unit • FT - Fixed Topology • NCU - Network Configuration Unit

**Processor clockspeeds are 20, 25 or 30 MHz with the appropriate DRAMs to allow memory access down to 3 cycles.**



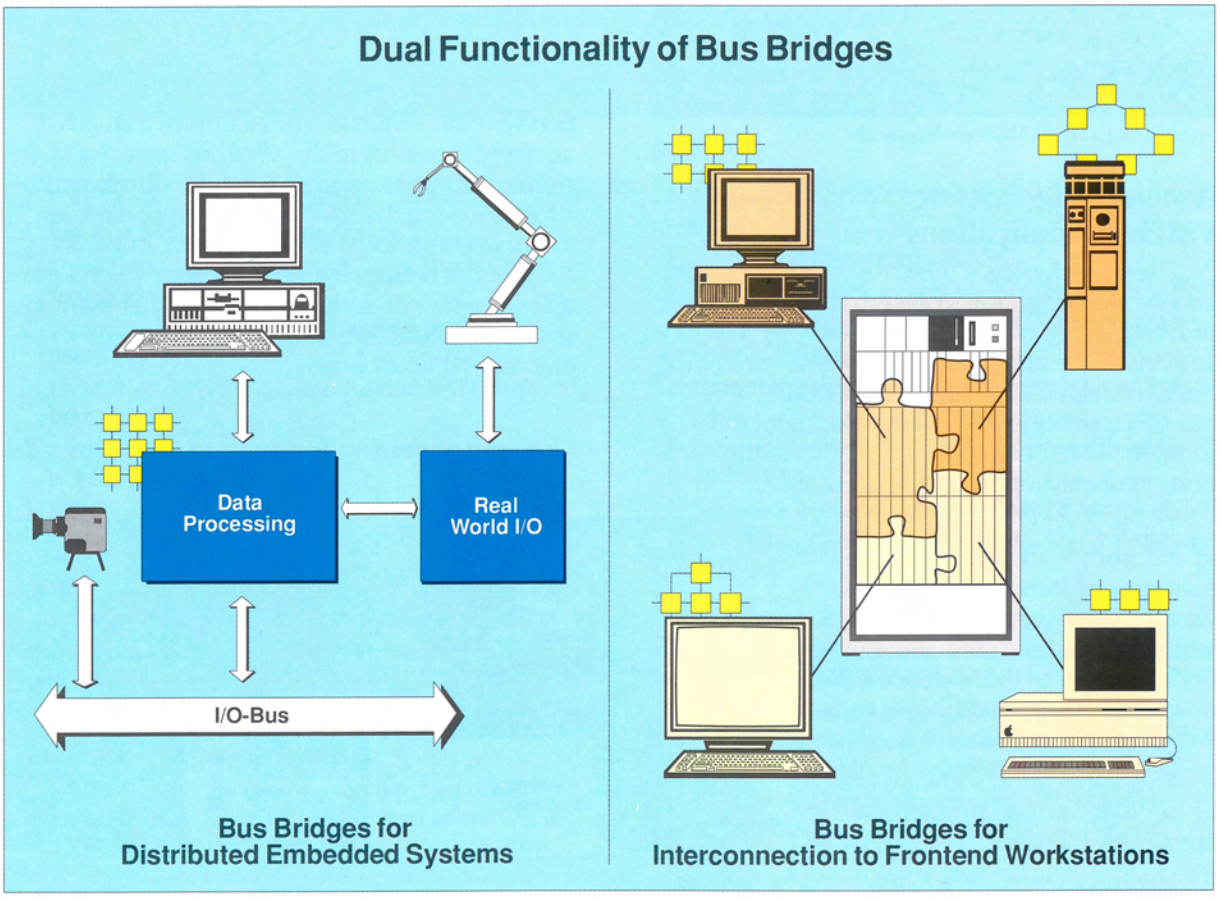
Video Animation,
Androme Sint-Truiden

# Parallel System Hosts

Parsytec Transputer systems support many popular hosts, such as PC, PS/2, Macintosh II, Sun, VAX, VME systems. There is an extensive range of interfaces between Parsytec systems and host machines such as the BBK-PC and the VMTM. Bus adapter modules, integrated into a PC or workstation, enable users to work with a large processor pool, comprising, for example, a MultiCluster-2 or a SuperCluster. Whatever the host, the development environment is the same. All Parsytec systems support the distributed operating system Helios, and the comprehensive development environment MultiTool, an extension of the Inmos TDS. An alternative development environment is offered by the Inmos Toolset, which is available for major hosts.

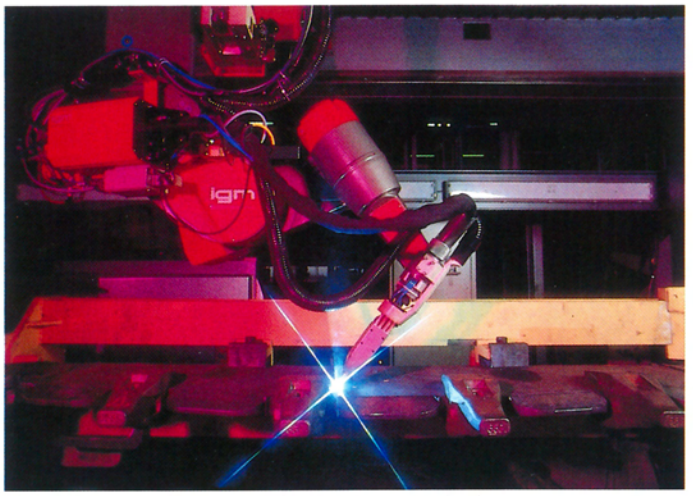
Parsytec offers a wide choice of host system support. For VMEbus systems, there is an intelligent host module, featuring dual-ported RAM to provide very fast data transfer which is not limited by Transputer link speed.

In addition to such intelligent units, there is also a range of slave interfaces, allowing easy access to large Transputer systems.



# VMEbus Systems

Parsytec VMEbus host systems have the advantage of scalable processing power and an extensive range of available hardware for I/O.



Welding Sensor System, IGM Wiener Neudorf

## Accelerating Existing VMEbus Applications

The inset depicts a typical system where processing throughput has been dramatically improved by loading the computationally intensive parts of the application onto Parsytec VMTM multi-Transputer modules. The existing VMEbus CPU, peripherals and development environment have been retained, so that a large proportion of existing software is reusable.

The host CPU can read or write to and from Transputer links via I/O mapped registers. Application software running within this slave network is loaded into the Transputers, under control of the VMEbus CPU, by means of supplied library calls which use these links.

This application software may have been developed in standard languages such as C, FORTRAN or Pascal. The Transputer development system runs under the familiar VMEbus environment of the main CPU, for example OS/9 or UNIX.

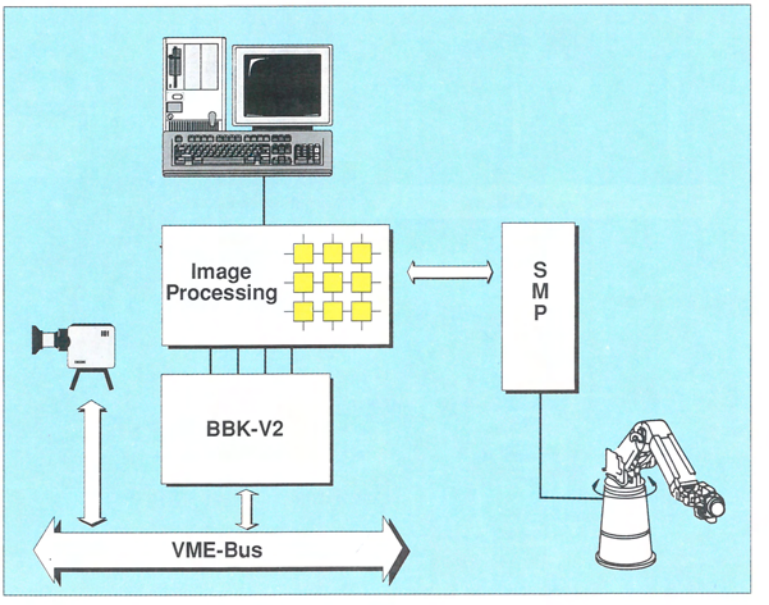
## Transputer as VMEbus Master Processor

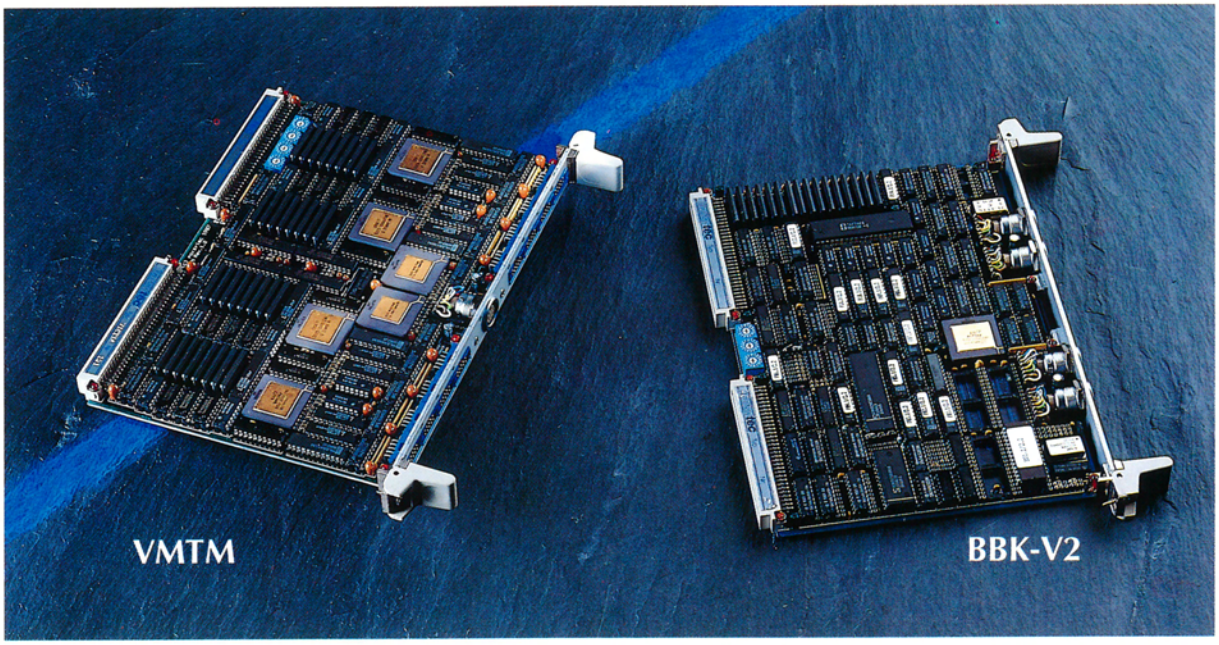
As shown in the figure below, the Transputer can operate as a VMEbus master processor, using a BBK-V2 module, substituting for the conventional bus master. The BBK-V2's Transputer has direct access to the VMEbus and can perform the same functions as a conventional VMEbus CPU.

This structure uses the VMEbus strictly for I/O transfers, and relieves the host CPU of all other communications overhead.

A host CPU is not required for I/O transfer, but because the BBK-V2 can run in a multi-master environment, it can also co-exist with the original VME system's CPU, running existing software.

Easy and efficient scalability does not depend on the VMEbus. For example, instead of adding processors to the VMEbus rack, the system could be expanded to a fully distributed structure, with the VMEbus system continuing to operate as a local I/O subsystem, but with most of the processing power concentrated in a Transputer network. This arrangement would support any number of processors housed in external 19" rack units.






## VMTM

- ❑ **Four 32-bit T800 Transputers**
- ❑ **Up to 4 MByte DRAM per node**
- ❑ **Dual C004 link switches giving software reconfiguration of topology**
- ❑ **Four C012 link adapters allowing multiple users**
- ❑ **Eight on-board UniLinks allowing VMTMs to be cascaded**
- ❑ **Additionally one external UniLink on front panel for local networking**
- ❑ **VMEbus slave with A24/A32, D08 capability**

The VMTM is a four-Transputer processor board with a complete slave interface to the VMEbus on a double-height Eurocard (6U). Included are twin C004 electronic switches allowing the processor topology to be software controlled. Four link adapters allow independent communications channels between the link switch and VMEbus interface. They permit up to four users to run concurrently.

Nine UniLinks are provided on the front panel. Eight are available from Berg connectors permitting several VMTM boards in a VME system to be cascaded. This enables large Transputer arrays to be configured. The ninth UniLink uses a rugged Lemosa-style connector and shielded twisted pair cable. This link can also be configured for compatibility with Inmos links.

## BBK-V2

- ❑ **High-speed bridge between VMEbus and Transputers**
- ❑ **2 MByte dual-ported DRAM**
- ❑ **4 MByte/s block moves supported**
- ❑ **Full VMEbus master/slave capability A24/A32, D08(EO)/D16/D32/UAT**
- ❑ **Comprehensive interrupt generation and handling**
- ❑ **External UniLink for RS-422 communication up to 30m**
- ❑ **Supports Motorola and Intel word access styles**
- ❑ **Standalone operation with additional 1 MByte EPROM**

With its T800 processor, the BBK-V2 operates either as an active master or as a slave interface between VMEbus and Transputer systems.

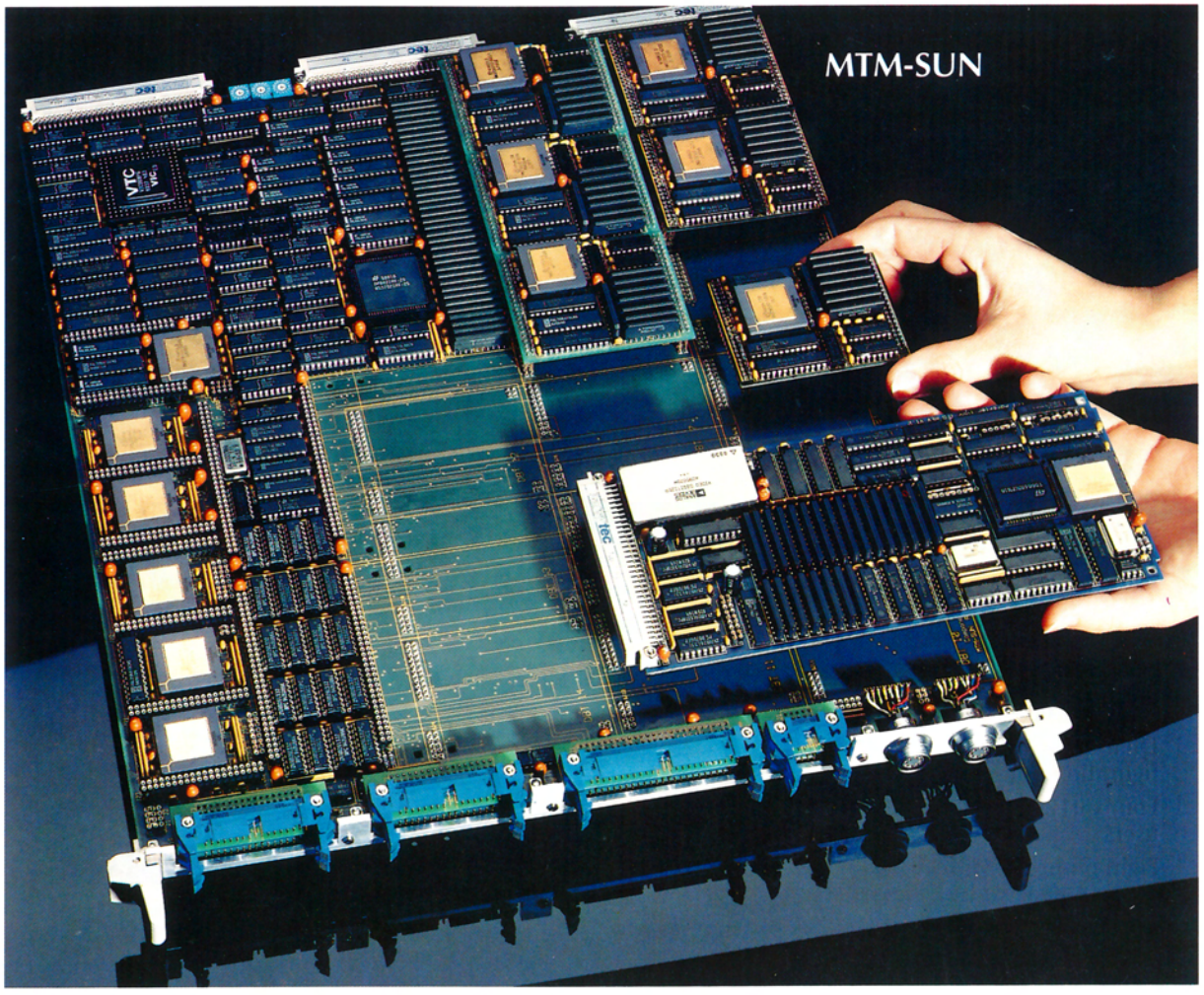
Fast data transfers are enabled by the use of dual-ported RAM, and the board has automatic shift hardware to allow fast block moves at 4 MByte/s.

The BBK-V2 has complete master/slave facilities on the VMEbus, including support for multi-master configurations. Interrupt generation and handling includes all VMEbus levels. A memory-mapped interrupt may be generated from the VMEbus.

An additional data communications port, at 20 Mbit/s over 10m, is provided by a front panel UniLink via Lemosa-style sockets and shielded twisted pair cable.

Software support includes a VMEbus access library and example programs, both supplied with the BBK-V2. It is packaged as a double-height Eurocard (6U).

# Sun Systems




The Parsytec MTM-SUN offers a wide range of processing power and I/O options, all in a 9U single module format. Parsytec also offers the BBK-V4, a 6U bridge between the Sun and external Transputer networks, which fits directly into a SPARC server 330. For 9U slots an adapter is available.

Both modules provide easy access to powerful, re-configurable Transputer system whilst retaining the familiar development tools of SunOS and UNIX.

## MTM-SUN

- ❑ **Parallel processing inside Sun workstations**
- ❑ **From 1 to 16 Transputers using daughterboards and UniLink modules**
- ❑ **Up to 16 MByte DRAM on a single processor node; 16 Transputers can have 4 MByte each**
- ❑ **Two slots for optional I/O, graphics, mass storage control modules**
- ❑ **Dynamic reconfiguration of system topology under software control**
- ❑ **External UniLinks for expansion to large processor networks**
- ❑ **Full VMEbus master/slave capability A16/A24/A32, D08(EO)/D16/D32/UAT**

## Multiple User Support

The MTM-SUN is a versatile high-performance Sun-to-Transputer interface. Designed as a 9U module for Sun workstations, it has complete VME master/slave facilities, including a 32-bit T800 processor and high-speed data transfer using from 4 to 32 MByte of dual-ported memory.

Expansion capability is ensured by space for 15 optional daughterboards and two Parsytec modules.

The MTM-SUN has a Network Configuration Unit (NCU) providing software-controlled hardware reconfiguration to support multiple users. Eight VME link interfaces allow up to eight users to share Transputer resources, including remote use, across Sun Ethernet LANs.

## Single-User/Multiuser

The MTM-SUN could, for example, be configured for one user with nine Transputers and seven further users each with one Transputer. Similary, it could serve eight users with two Transputers each. Multiuser access is supported by the Helios operating system and the MultiTool development environment.

All interprocessor communication is via Parsytec UniLinks. As with the MultiCluster and SuperCluster series, an important feature is the independent determination by each user of the partition topology and operating system. For improved performance, several MTM-SUN modules can be combined in one Sun workstation.

## System Expansion

Expansion is supported by connecting UniLinks to external networks such as the MultiCluster-2 or the SuperCluster system.

Additional interfaces include connections to video input/output signals from Parsytec's TFG (Transputer Frame Grabber), GDS-1, GDS-2 (Graphic Display Subsystems) and to a SCSI-bus from the MSC (Mass Storage Controller). All these I/O options can be readily integrated into the MTM-SUN motherboard. For example, one can integrate 15 single slot daughterboards, or 7 double slot daughterboards or 2 UniLink modules with up to four single slot (two double slot) daughterboards.

The Sun-VMEbus interface supports A16/A24/A32 addressing capabilities, D08(EO)/D16/D32/UAT data types and has full VMEbus interrupter/interrupt handler support. Interprocessor communication is facilitated by bus-compliant mailbox registers.

The MTM-SUN is supplied with configuration software running under the SunOS UNIX operating system.

## Additional Information

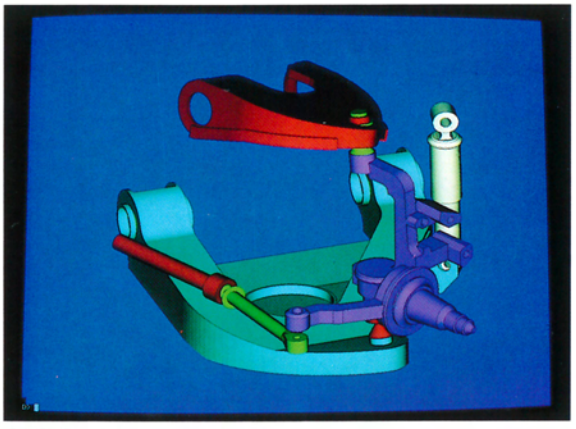
## BBK-V4

- **Four UniLink interfaces to the VMEbus**
- **20 Mbit/s RS-422 UniLink networking**
- **May be run concurrently with other BBK-V4s**
- **Multiuser support for Sun workstations**
- **VMEbus slave with A24/A32, D08 capability**

A cost-effective interface between Transputer systems and Sun workstations is provided by the BBK-V4 bus bridge. This 6U format module has four UniLinks available for connection to MultiCluster-1, MultiCluster-2 or SuperCluster systems.

## SUN-Frame

The SUN-frame adapter allows the 6U VMTM (or BBK-V1, BBK-V2, BBK-V4) to be used in 9U Sun workstations. Five Lemosa connectors are provided on the front panel, one of which may be used for controlling configuration.



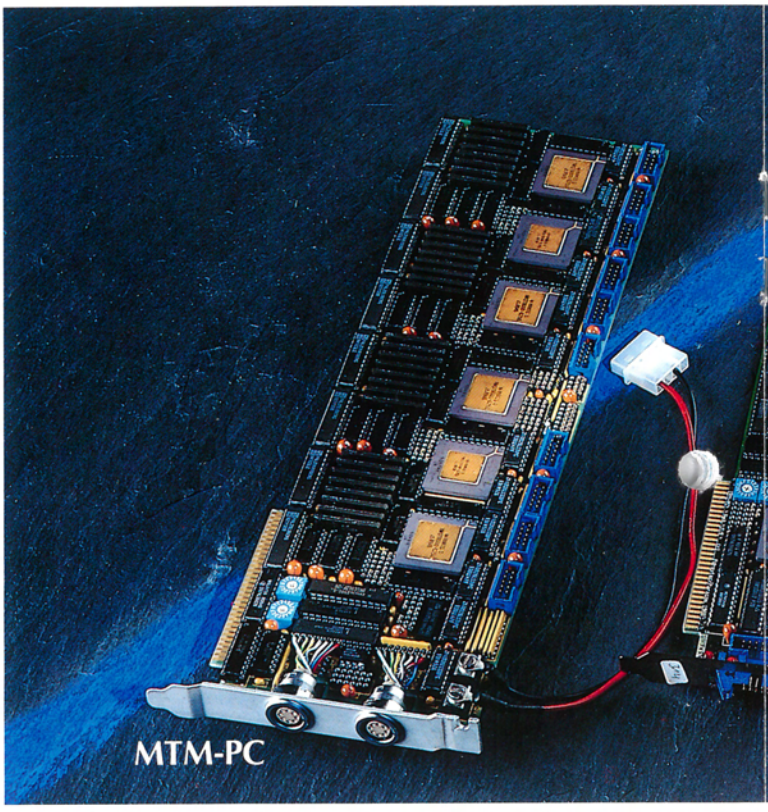
CAD Design

# PC/XT/AT Systems

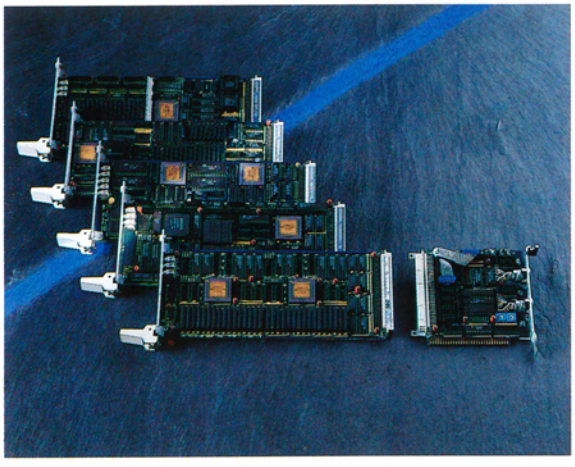
Parsytec's extensive support for one of the most popular desktop development environments is demonstrated by a flexible approach to the IBM PC XT/AT or compatible hosts.

The BBK-PC is a short PCbus adapter for any of the wide range of Parsytec modules. The MTM-PC is a powerful processor module with four Transputers, supporting software reconfiguration of system topology. A single-Transputer module, the TPM-PC, is also available for evaluation and training applications having a variety of I/O modules, processor modules etc. available as daughterboards.

In addition to software support from MultiTool and the Helios operating system, PCs running MS-DOS are supported by a low-cost graphics library, fully compatible with Microsoft C and operational with CGA, EGA and VGA standards.



MTM-PC

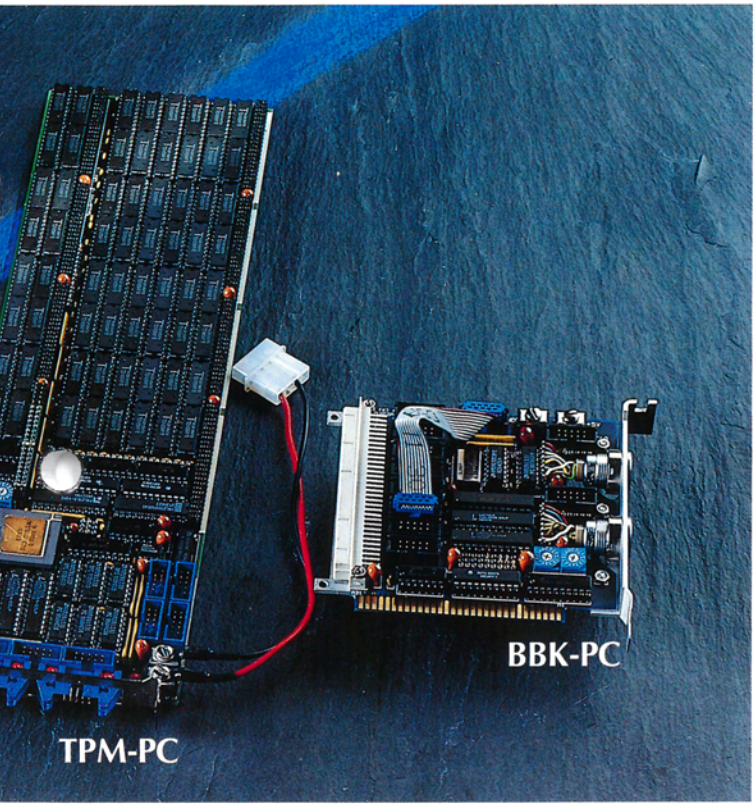


## BBK-PC

- ❑ **Combines with any of the Parsytec modules to form a standard size internal PC expansion card**
- ❑ **Two UniLink ports for connection to external systems and networking**

The same UniLink module can therefore be taken from the evaluation stage, through PC development environments, out onto standalone systems, such as MultiCluster-1, or hosted parallel systems such as MultiCluster-2 and SuperCluster.

The comprehensive set of available UniLink modules (see UniLink section later) means there is a PC board for all Transputer applications.




## MTM-PC

- ❑ **Four T800 Transputers giving 40 MIPS / 6 MFLOPS performance**
- ❑ **Up to 4 MByte DRAM per node**
- ❑ **Dual C004 switches to reconfigure processor topology**
- ❑ **Cascadable with other MTM-PCs to form large arrays**
- ❑ **12 UniLinks for system expansion**
- ❑ **Two RS-422 buffered UniLink ports for networking**
- ❑ **Support for 2 Inmos TRAMs**
- ❑ **Complete software environment with MultiTool and Helios**

The MTM-PC is a multiple Transputer board for IBM PC AT/XT or compatible systems.

Its four Transputers each have 1 or 4 MBytes DRAM and each has four separate communications links, routed through a C004 link switch. A second link switch is used to route analyse/reset lines.

From the link switch, connections are available from Berg connectors for use according to the needs of the application. Each is RS-422 buffered and four of the links can be daisy-chained under software control to join multiple MTM-PCs.

Two UniLink ports are provided from Lemosa connectors on the front panel to allow RS-422 networking up to 30m from the board at 10 Mbit/s.

To ensure compatibility with Transputer systems from other manufacturers, one of these can be configured as an Inmos compatible TTL Link.

The MTM-PC accepts up to two Inmos-compatible TRAMs, sizes 1, 2, 4, or 8, allowing a further 2 Transputers to be included on the board.

## TPM-PC

- ❑ **Single Transputer**
- ❑ **Expandable to four Transputers**
- ❑ **Up to 8 MByte DRAM on host node**
- ❑ **daughterboard option for reconfiguration**
- ❑ **I/O and daughterboards available**
- ❑ **UniLink standard supported**

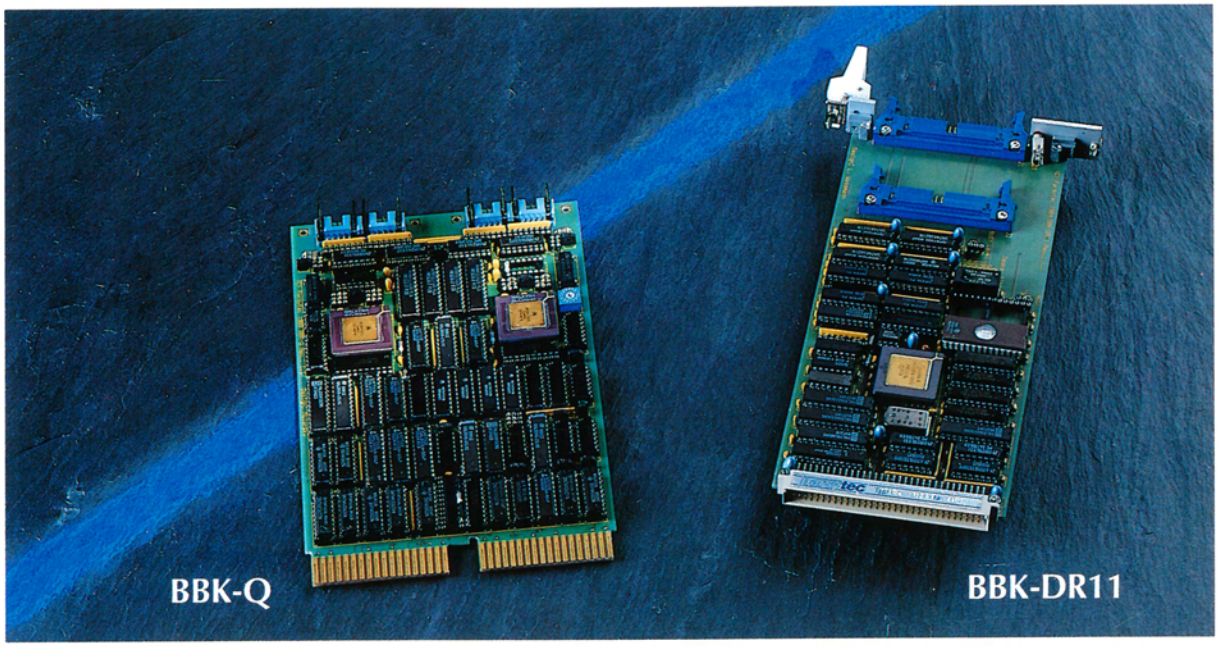
The TPM-PC provides a single Transputer board, ideal as an expandable entry-level system, particularly for evaluation and training. Expansion is via daughterboards, adding additional processors or I/O functions such as RS-232 ports, parallel interfaces, and the IEEE-488 bus.

All serial links conform to the Parsytec UniLink standard, ensuring high noise immunity and fault tolerance.

The TPM-PC is available with software support including a variety of standalone compilers, the Helios operating system and the MultiTool development environment.

Real-Time Emergency Guidance System, Brenk Aachen

# DEC Interfaces




## BBK-Q

- ❑ **250-300 KByte/s Q-bus to Transputer interface**
- ❑ **Two DMA controllers, each with four channels for fast data transfer**
- ❑ **Four bidirectional 20 Mbit/s serial links, configured as UniLink or Inmos links**
- ❑ **Link reset/analyse on individual or global basis**
- ❑ **Multiuser support for up to four concurrent transfers**
- ❑ **Generation of level 4 Q-bus interrupt**

The BBK-Q allows DEC Q-bus systems to be used as front-end interfaces to large Transputer networks.

Data transfer is via the BBK-Q's 20 Mbit/s serial links. The link design allows either the UniLink (individual analyse/reset) or Inmos (global reset) schemes.

The Q-bus interface can operate as a master or slave and is capable of generating interrupts on level BIRQ4.

Software support includes a VAX VMS driver and example programs written in C. The MultiTool development environment supports up to four users on a single BBK-Q. Compilers available include Occam, C, FORTRAN, Pascal, and Prolog.

## BBK-DR11

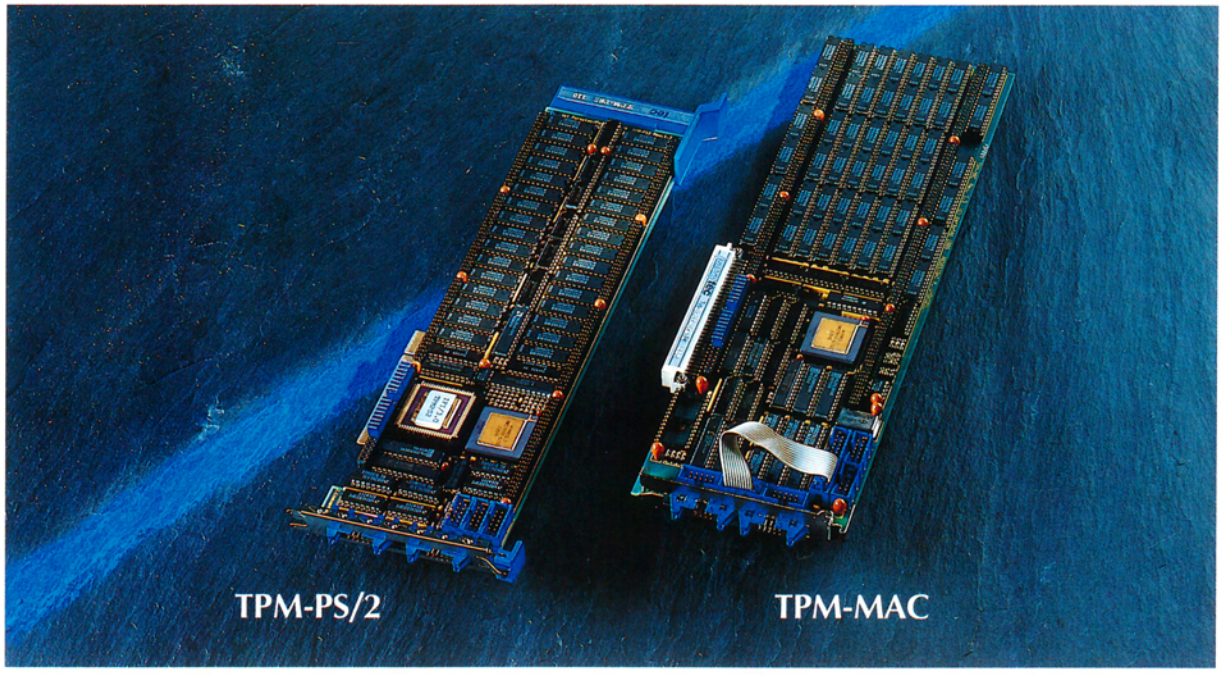
- ❑ **Fast interface between DR11-W or DRV11-W and Transputer links**
- ❑ **T222 Transputer provides interface controller**
- ❑ **High-speed Transputer block move**
- ❑ **Four 20 Mbit/s UniLinks for communication**
- ❑ **32 KByte SRAM for buffering**
- ❑ **Standalone operation with 16 KByte EPROM bootstrap**

The BBK-DR11 board is a high-speed parallel I/O module designed for interfacing a Transputer network to a DEC DR11-W or DRV11-W.

Wait logic automatically synchronises Transputer accesses to the DR11 data port with cycle requests from the DR11 device.

Input and output registers of the DR11 interface can be accessed over a 16 KByte address range, providing very fast block move operations between the parallel ports and the UniLinks.

# PS/2 Bus and Mac-NuBus Systems




## TPM-PS/2

- ❑ **Micro Channel to Transputer interface for IBM PS/2 computers**
- ❑ **Single T800, expandable to four Transputers using daughterboards**
- ❑ **Up to 4 MByte DRAM on host node**
- ❑ **Optional processor reconfiguration under software control**
- ❑ **Three daughterboard sockets for serial/parallel I/O, IEEE-488 interfaces**
- ❑ **UniLink communications conforming to the RS-422 standard**

With up to four T800 Transputers and a maximum of 16 MByte of RAM, (4 MByte on the host node) the TPM-PS/2 can provide 6 MFLOPS of processing power for Micro Channel Architecture systems.

It is configured as a slave subsystem, interfacing between the eight-bit wide PS/2 I/O bus and Parsytec UniLinks. The basic configuration has a single Transputer and up to 4 MByte of DRAM.

The four Transputer links, operating at up to 20 Mbit/s, can be connected to other Transputers, with two links capable of being brought out externally to provide UniLink RS-422 standard communication.

Up to three Transputer, or I/O interface, daughterboards can be added to the TPM-PS/2 to provide additional processors or I/O such as RS-232, IEEE-488.

The module is available with standalone compilers, the Helios operating system and the MultiTool development environment.

## TPM-MAC

- ❑ **NuBus to Transputer interface for Apple Macintosh II**
- ❑ **Up to 6 MByte DRAM on host node**
- ❑ **32-bit T800 with flexible I/O interfaces**
- ❑ **Expandable up to four Transputers**
- ❑ **Optional processor reconfiguration under software control**
- ❑ **Three daughterboard sockets for RS-232, parallel I/O, IEEE-488 or processor expansion**
- ❑ **UniLink interface for external expansion**

Designed to occupy NuBus expansion slots in the Apple Macintosh II, the TPM-MAC provides Transputer interfaces to the host NuBus. The Transputer node is a T800 32-bit processor with up to 6 MByte DRAM.

The interface uses a C012 link adapter to convert the bidirectional serial links into NuBus parallel data streams.

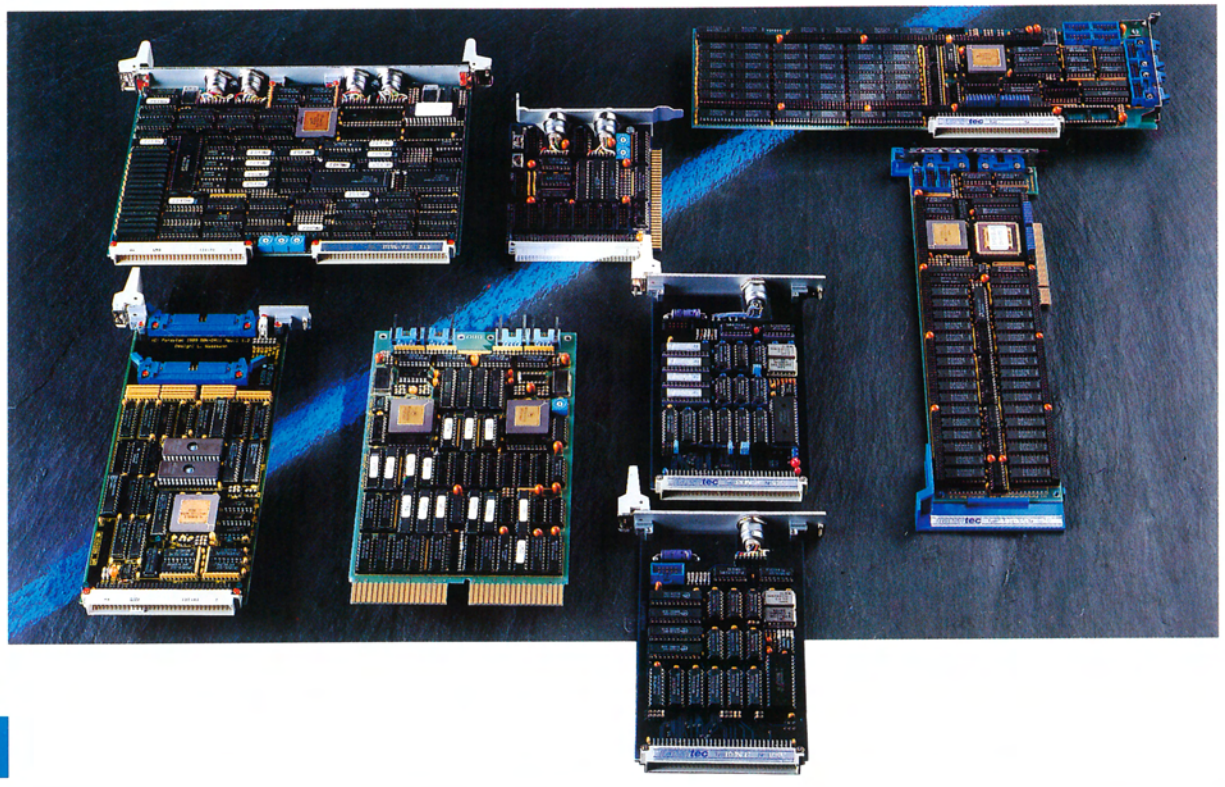
Slots are provided for a DBC electronic link switch daughterboard and up to three further daughterboards. These are used for additional processors, or I/O such as RS-232 and IEEE-488.

All serial links conform to the UniLink standard ensuring complete compatibility with the Parsytec range as well as with RS-422 communications schemes.

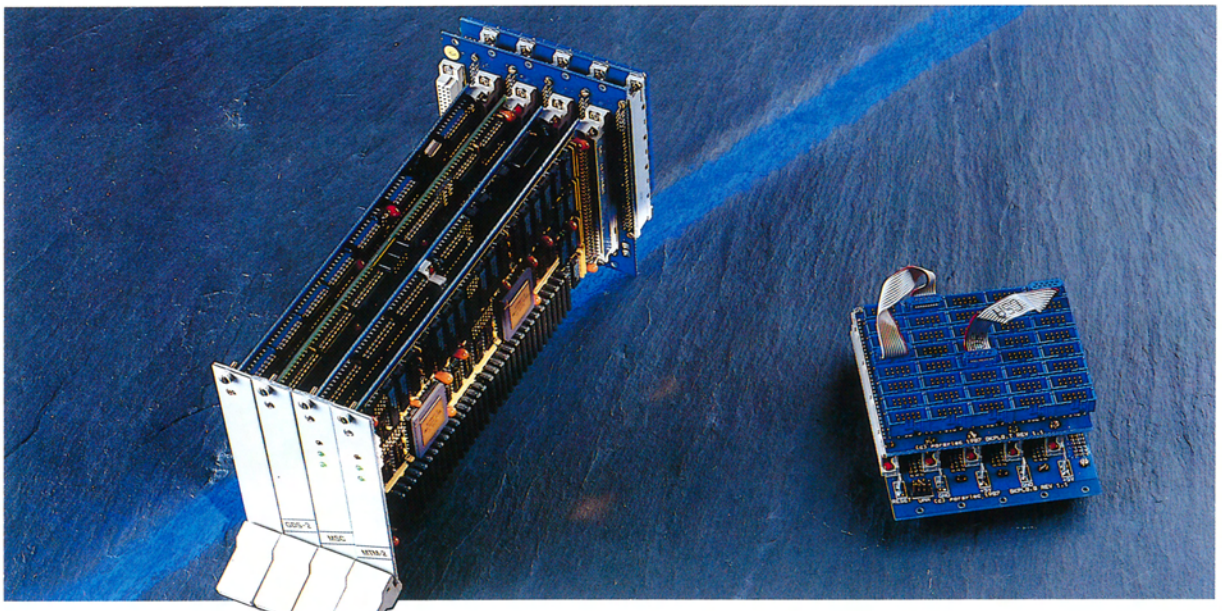
Software drivers are supplied for the Apple OS, and the TPM-MAC is available with standalone compilers, the Helios operating system and the MultiTool development environment.

# Summary

| Host System | Interface to Host | Max. No. of Processors | Reconfiguration Facilities | Max. Memory per Node | External UniLink Connectors | Max. No. of Users |
|---|---|---|---|---|---|---|
| **SUN** | MTM-SUN | 16 x T800 | NCU | 16 MB | 18 | 8 |
| | BBK-V4 | none | — | — | 4 | 4 |
| | VMTM | 4 x T800 | Dual C004 | 4 MB | 9 | 4 |
| | BBK-V2 | 1 x T800 | — | 2 MB | 4 | 1 |
| **VMEbus** | VMTM | 4 x T800 | Dual C004 | 4 MB | 9 | 4 |
| | BBK-V2 | 1 x T800 | — | 2 MB | 4 | 1 |
| | BBK-V4 | none | — | — | 4 | 4 |
| **PCbus** | BBK-PC | none | — | — | 2 | 1 |
| | MTM-PC | 4 x T800 | Dual C004 | 4 MB | 2 | 1 |
| | TPM-PC | 4 x T800 | DBC | 8 MB | 2 | 1 |
| | ADAPT-PC | none | — | — | — | — |
| **DEC** | BBK-Q | none | — | — | 4 | 4 |
| | BBK-DR11 | 1 x T222 | — | — | ( 4 ) | — |
| **PS/2** | TPM-PS/2 | 4 x T800 | DBC | 4 MB | 2 | 1 |
| **Mac-II** | TPM-MAC | 4 x T800 | DBC | 6 MB | 2 | 1 |
| | MTM-MAC | 2 x T800 | Jumper | 8 MB | 2 | 1 |



# UniLink Modules



## Introduction

UniLink modules provide expandability, and wide functionality for Parsytec parallel systems, following the industry-standard extended single Eurocard format (100 x 220 mm).

In addition to single and multi-Transputer processing modules, offered in a range of clock speeds and memory sizes, UniLink modules provide I/O, video and graphics, mass storage control, data acquisition, signal processing and Ethernet. The power of UniLink modules can be expanded by the use of processor daughterboards.

Configured as extended single-height Eurocards, they fit into standard 19'' racks. They may be configured with MultiCluster-2 or SuperCluster systems giving enhanced capabilities. They may also be incorporated as subsystems combined with host interfaces such as the BBK-PC adapter or MTM-SUN bus bridge.

## The Interconnection of UniLink Modules

UniLink modules provide high integrity and robustness for demanding applications, due to the fault tolerance and noise immunity of the UniLink standard.

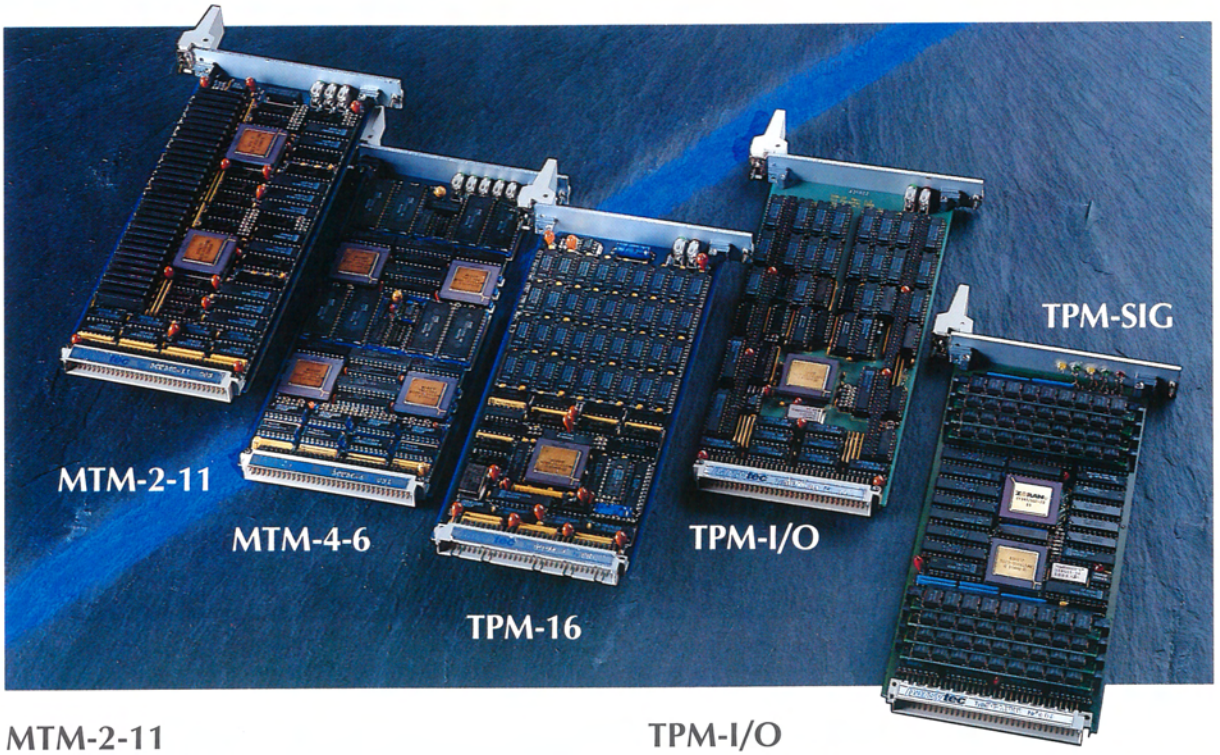
All UniLink modules have a rear-mounted 96-way connector conforming to DIN41612. This can plug directly into a host adapter module such as the BBK-PC or MTM-SUN. Alternatively, it may be attached to a MultiCluster-BP backplane, which provides power and ground connections for all modules in the rack.

The Parsytec adapter makes it easy to configure Transputer networks consisting of UniLink modules plugged into a backplane. It allows UniLinks to be connected between Transputers either on the same module or other modules in the rack. Five slots are provided, each with Berg connectors for eight UniLinks.

External connections to and from UniLink modules, such as remote UniLinks to other systems, or standard buses to local mass storage, are also made via the Eurocard's rear DIN sokket.

UniLink ports on the back panel of the system racks allow connection via Lemosa connectors with host-interface modules. Other external interfaces such as RGB in/out for video may also be connected through the back panel.

# Processor Modules




## MTM-2-11

- ❑ **Two T800 processors**
- ❑ **1 to 8 MBytes local DRAM**

The MTM-2 modules have two T800 Transputers. They are available with 1 MByte (MTM-2-10), 2 MByte (MTM-2-11), 4 MByte (MTM-2-12) or 8 MByte (MTM-2-13) of local DRAM. All 8 Transputer links are RS-422 buffered and brought out to the rear DIN connector as UniLinks.

## MTM-4-6

- ❑ **Four T222 processors**
- ❑ **64 KBytes local SRAM per node**

The MTM-4-6 is a quad-Transputer module, with four T222 processors, configured as a hard-wired 2x2 mesh. Each Transputer node has 64 KByte of local SRAM. Four RS-422 buffered UniLinks are taken to a rear DIN connector. Using jumpers, the remaining four links can be switched freely amongst the Transputers or brought out as buffered UniLinks on the rear DIN connector.

## TPM-16 TPM-32

- ❑ **Single T800 processor**
- ❑ **16 or 32 MBytes local DRAM**

The TPM-16 (32) is a single processor module with 16 or 32 MBytes of DRAM. The four Transputer links are RS-422 buffered and are brought out to the rear DIN connector as UniLinks.

## TPM-I/O

- ❑ **Single T800 processor**
- ❑ **2 MBytes DRAM**
- ❑ **3 expansion sites for I/O daughterboards and one processor daughterboard**

The TPM-I/O has a single T800 Transputer with 2 MByte of DRAM. It provides a UniLink carrier module with three sites for daughterboards. One site can accommodate a DBT processor daughterboard.

Eight UniLink interfaces are provided for external connection, allowing networking at up 20 Mbit/s via the rear panel DIN connector.

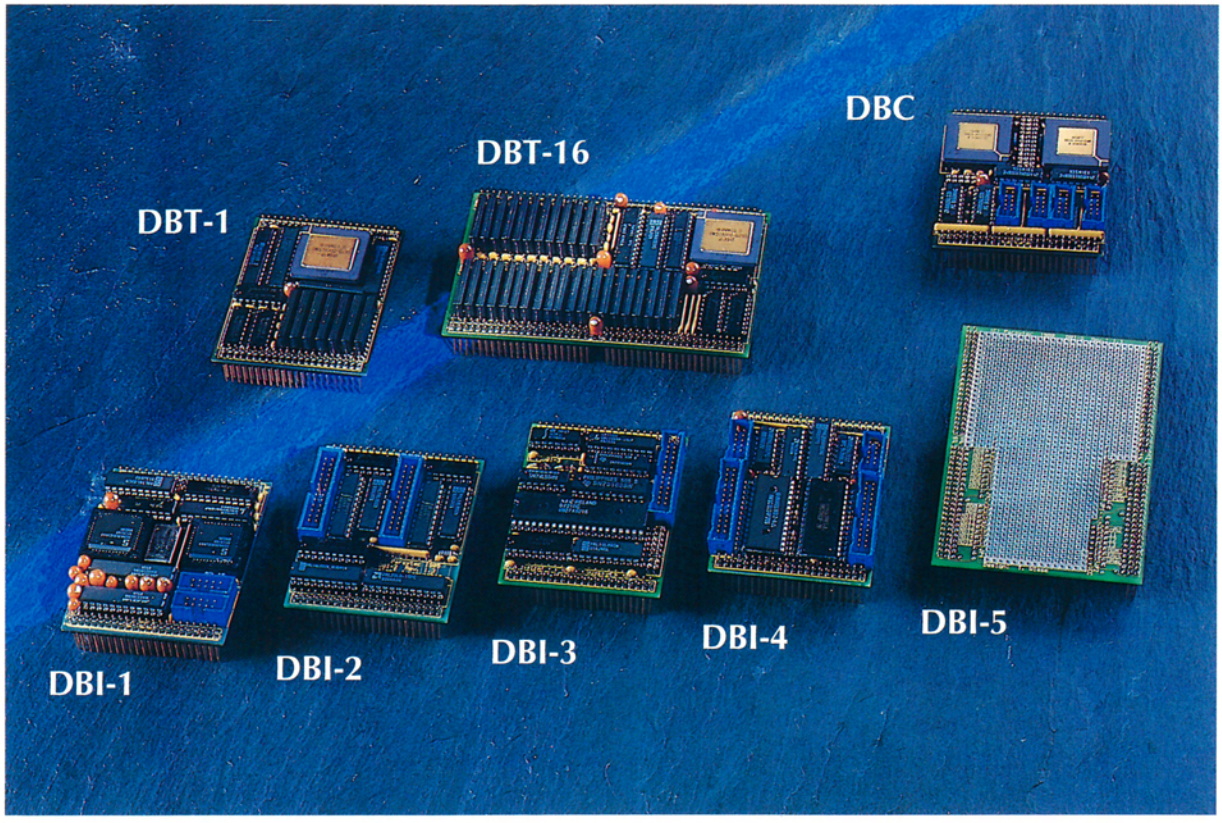
## TPM-SIG

- ❑ **Zoran ZR34325 digital signal processor**
- ❑ **Inmos T800 processor with 4 MByte of local DRAM**
- ❑ **4 MBytes of shared DRAM**
- ❑ **37.5 vector MFLOPS performance**
- ❑ **Supports 16 & 24-bit integer, 32-bit floating-point data (ANSI/IEEE-754)**
- ❑ **DSP software libraries**

TPM-SIG has a Zoran ZR34325 digital signal processor and a T800 32-bit floating-point Transputer. These deliver respectively 37.5 MFLOPS single precision peak vector- and 1.9 MFLOPS scalar performance. Both processors share 4 MByte of DRAM. The T800 also has 4 MByte of local DRAM.

The instruction set directly supports vector, vector-matrix and matrix-matrix operations, polynomial expansion, FIR and IIR filtering, FFTs and inverse FFTs. The module supports 16 and 24-bit integers and 32-bit floating point data (ANSI/IEEE 754). Signal processing libraries are available in Occam, FORTRAN, and C.

# Daughterboards




The Parsytec range of processor and I/O daughterboards is designed to enhance the power and functionality of Parsytec's Transputer systems. For systems accepting UniLink modules, the TPM-I/O motherboard can be used. For other systems, the TPM-PC, TPM-PS/2, TPM-MAC or MTM-SUN motherboards are available.

## DBT-1, DBT-4, DBT-8, DBT-16

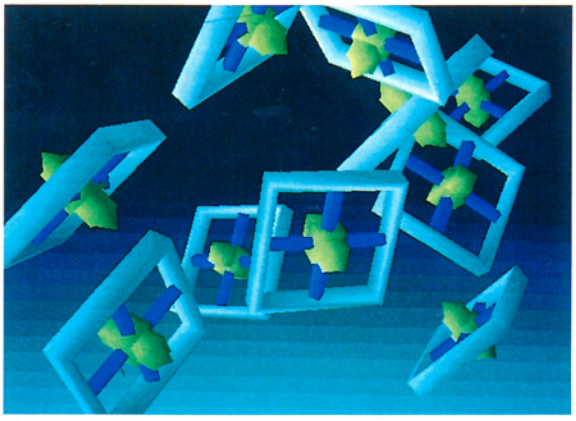
- ❑ **T800 plus 1 to 16 MByte local DRAM**
- ❑ **Occupies 1 or 2 daughterboard site**

The DBT series boards comprise a single Transputer daughterboard occupying one (DBT-1,4) or two (DBT-8,16) daughterboard sites. The T800 is supplied with 1 MByte (4MB, 8MB, and 16MB resp.) of DRAM. Its four links are connected, via the link interconnection slot of the motherboard, to a DBC configuration daughterboard which is required for this series of boards.

## DBC

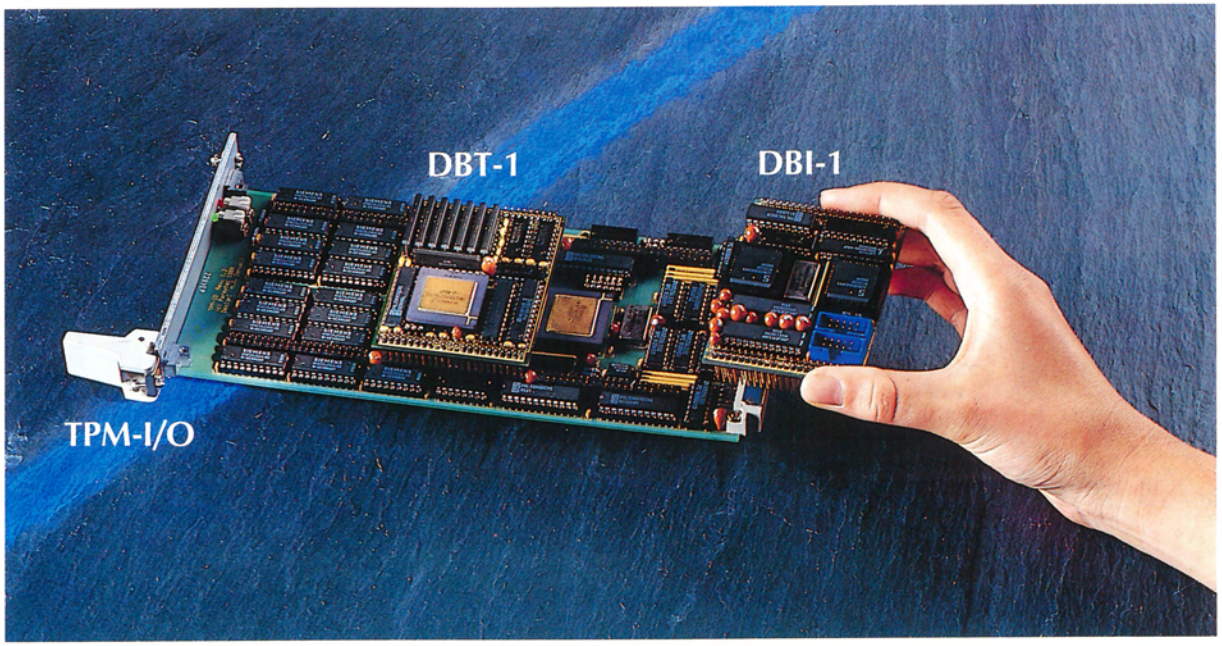
- ❑ **Link configuration for the DBT series of boards**

This electronic link switch configures Transputer links on the motherboard, links on up to three additional daughterboards, and eight external UniLink connections. A TPM-PC together with a DBC and three DBTs acts as an MTM-PC.



Gouraud Shading, VW Wolfsburg

# I/O Daughterboards




## DBI-1

- ❑ **Four RS-232 serial ports**
- ❑ **Data rates from 50 to 38,400 baud**
- ❑ **One daughterboard site required**

The DBI-1 provides four independent RS-232 serial ports, memory-mapped to the TPM series boards to enhance functionality. It occupies a single daughterboard site.

Data rate and format are software controllable. Software support includes versatile C and Occam libraries.

## DBI-2

- ❑ **16 channel digital I/O interface**
- ❑ **Optional Centronics port capability**
- ❑ **One daughterboard site required**

The DBI-2 is a high-speed 16-bit bidirectional parallel interface, memory-mapped to the Transputer section of the motherboard for maximum throughput.

Occupying a single daughterboard site, it supports both handshaking and interrupt-driven I/O. It has a standard Centronics printer port as an option.

## DBI-3

- ❑ **IEEE-488/GPIB interface**
- ❑ **Full Talk/Listen capabilities**
- ❑ **One daughterboard site required**

The DBI-3 is an IEEE-488 interface with full Talk/Listen capabilities. The daughterboard can deal with Service Requests and parallel polling. The data rate is programmable and default addresses are set by jumpers.

The motherboard Transputer accesses GPIB data through eight read and eight write registers on the DBI-3.

## DBI-4

- ❑ **Dual C011 serial link adapters**
- ❑ **Converts serial links to/from parallel**
- ❑ **Provides interface between Transputer and other microprocessor busses**
- ❑ **One daughterboard site required**

The DBI-4 comprises dual Inmos C011 link adapters to convert (Inmos) serial data to bidirectional eight-bit parallel I/O. Occupying a single daughterboard site, it provides two input and two output bytewide data streams from two Transputer links.

These programmable I/O ports can be used between external Transputers, or those on the motherboard or an adjacent daughterboard.

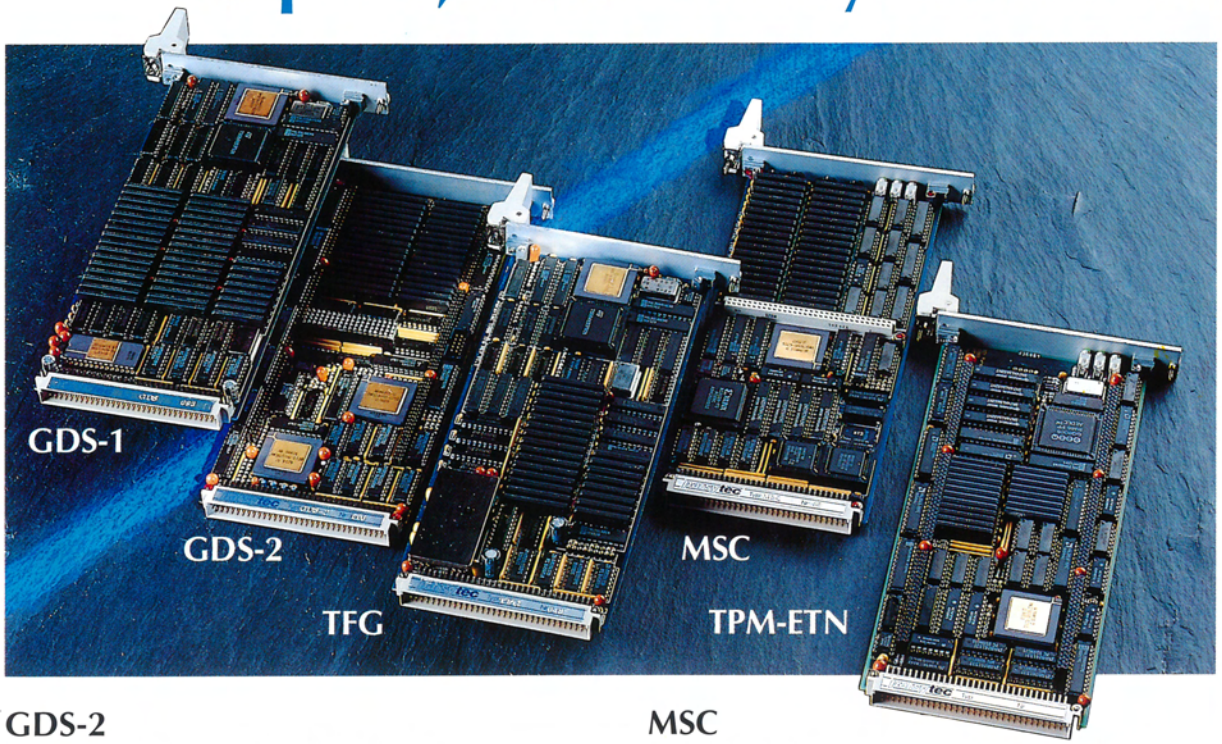
## DBI-5

- ❑ **Prototyping module for custom designs**
- ❑ **Precoded and buffered to Transputer memory map**
- ❑ **Two daughterboard sites required**

The DBI-5 is a daughterboard designed for prototyping and rapid development of custom modules for user-specific applications. Precoded and buffered for Transputer memory-mapped designs, the DBI-5 occupies two daughterboard sites.

All components are on the reverse of the module, leaving the whole upper area available to the user.

# Graphics, Video and System Interfaces




## GDS-2

- ❑ **Up to 1280 x 1024 pixel resolution**
- ❑ **T800 with up to 8 MBytes DRAM**
- ❑ **G300 colour video controller**
- ❑ **Three daughterboard sites for expansion**
- ❑ **XWindow, GKS and CGI supported**

The GDS-2 is a high-resolution graphics board using the G300 colour video controller. The board can display resolutions from 1280 x 1024 with 8-bit pixels to 800 x 600 with 24-bit pixels. Its T800 has 2 MByte of video RAM and 2 or 8 MByte DRAM. Three daughterboard sites are provided and the DB-DMA enables 8 external links to access video RAM (maximum data rate 11 MByte/s). XWindow is supported under Helios. Support is available for GKS, CGI and UTOPIA. For smaller applications the GDS-1 with a display resolution of up to 1024 x 768 pixels and 256 colours is also available.

## TFG

- ❑ **Input/output resolution of 1024 x 512 pixels**
- ❑ **256 colours displayed from G170 CLUT**

The Transputer Frame Grabber is an image processing subsystem providing an input resolution of 1024 x 512 8-bit pixels from a 12.5 MHz analogue signal. The T800 processor has 1 MByte DRAM and 4 standard UniLinks. UTOPIA drivers are available.

## MSC

- ❑ **High performance SCSI/Floppy interface**
- ❑ **Up to 16 MBytes cache DRAM onboard**
- ❑ **Concurrent data over SCSI and UniLinks**

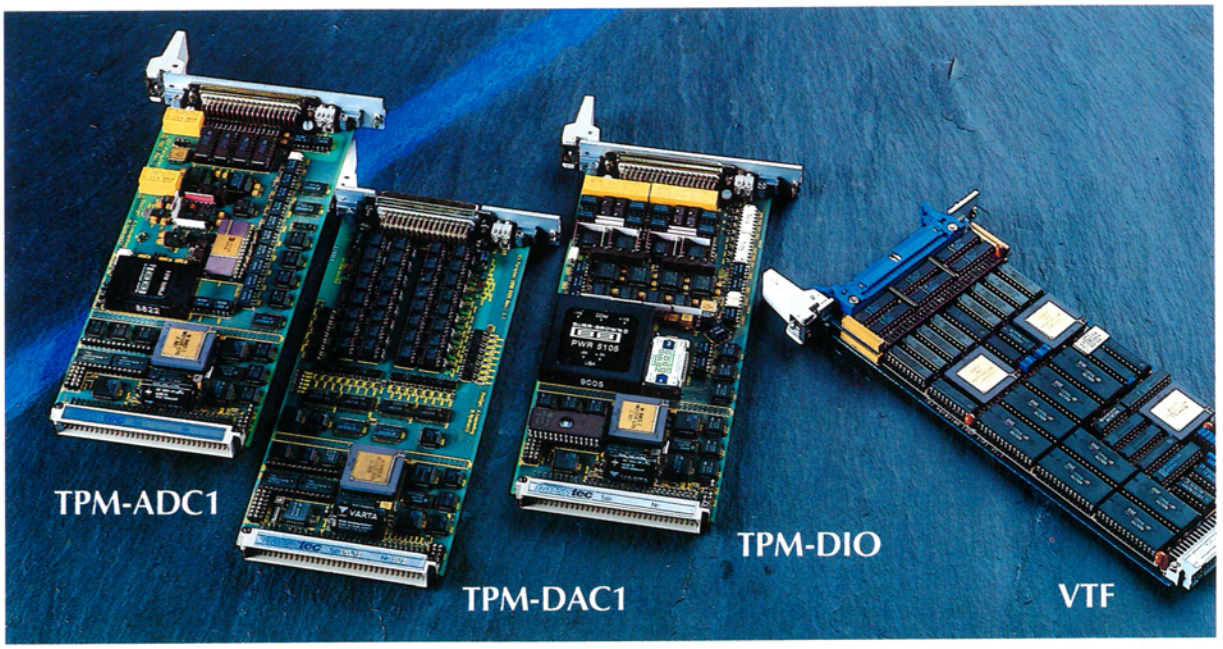
The MSC comprises a SCSI, floppy disk interface and a T800 with 4 or 16 MByte of parity DRAM for use as cache memory. Very high data bandwidth is possible using multiple interfaces. The MSC can perform SCSI bus transfers simultaneously with data transfer over four UniLinks. Hardware drivers support Winchester, floppy, and optical disk drives as well as a variety of tape streamers.

## TPM-ETN

- ❑ **Ethernet interface with up to 8 MBytes RAM**
- ❑ **Conforms to IEEE 802.3 physical and data layer standards**
- ❑ **Supports 10Base5 and 10Base2 media access**
- ❑ **Helios and BSD 4.3 network software**
- ❑ **Three daughterboard sites**

The TPM-ETN is an Ethernet interface with 2 or 8 MBytes of memory, four UniLinks and a T800 acting as an interface controller running TCP/IP protocols. A SEEQ 8005 provides all physical layer and data link layer functions of the IEEE 802.3 standard. The board supports both the 10Base5 thick-wire and the alternative thin-wire Cheapernet 10Base2 media access. Three daughterboard sites are provided. Software support is under Helios. Higher levels in the ISO model have been addressed by porting BSD 4.3 network software to the Transputer.

# Data Acquisition and I/O




## TPM-ADC1

- 16 channel 12-bit A/D converter
- High sample rate of 200 KSPS
- Input ranging under software control
- Local control by isolated CPU section with T222, interrupt control and RTC
- External and internal trigger facilities
- 64 KByte SRAM / 32 KByte (E)EPROM
- Optional S/H for all inputs

The TPM-ADC is a 12-bit A/D converter with multiplexed sample/hold conversion at 200 kHz for 16 single ended channels or 8 differential channels. The system has online software control for individual channel selection. Comprehensive data acquisition functions include multiple trigger and handshake facilities, autoranging and software control of gain/offset. Input ranging is under software control with ranges from ±2.5V to ±10V or from 0-2.5V to 0-10V. Filtering and overvoltage protection are provided. Real-time control is by an isolated CPU section using a T222, incorporating four buffered UniLinks, watchdog timer, real-time clock, interrupt handling capabilities and battery backup.

## TPM-DAC1

- 8 channel 12-bit D/A converter
- 2 microsecond settling time
- Software selectable output ranges
- Output settle to fail-safe on reset or power-down
- Local control by isolated CPU section with T222, interrupt control and RTC
- 64 KByte SRAM / 32 KByte (E)EPROM

The TPM-DAC is a 12-bit D/A converter with a 2 microseconds settling time for eight ground-referenced channels or four differential channels. The system has online software control for individual channels. Output ranges are software selectable in ranges ±5V, ±10V, 0-5V, or 0-10V. Output current capability is 50mA over the whole range. Output registers can be updated simultaneously using either internal or external triggers. Outputs are designed with fail-safe settling to a 0V level in case of power-down, reset or external emergency flag. Real-time control is by an isolated CPU section with a T222, incorporating four buffered UniLinks, watchdog timer, real-time clock, interrupt handling capabilities and battery backup.

## TPM-DIO

- 32 channel opto-isolated digital I/O
- Output short-circuit and thermal protection
- Data readback from output registers
- Local control by isolated CPU section with T222, interrupt control and RTC
- 64 KByte SRAM / 32 KByte (E)EPROM

The TPM-DIO has 32 opto-isolated digital I/O lines organised as two 8-bit input and two 8-bit output ports. Its two I/O sections are separated galvanically to improve noise immunity. Output short-circuit, thermal protection, internal or external trigger capability are provided. Outputs are designed with fail-safe settling at "high-Z" level in case of power-down, reset, or external emergency flag. Output registers have data readback. Real-time control by an isolated CPU section with a T222, incorporating four buffered UniLinks, watchdog timer, real-time clock, interrupt handling capabilities and battery backup.

## VTF

- Two fast 16-bit parallel I/O ports
- T800 with 256K static 35 ns RAM
- Two T222 with 32K CMOS RAM controlling each port

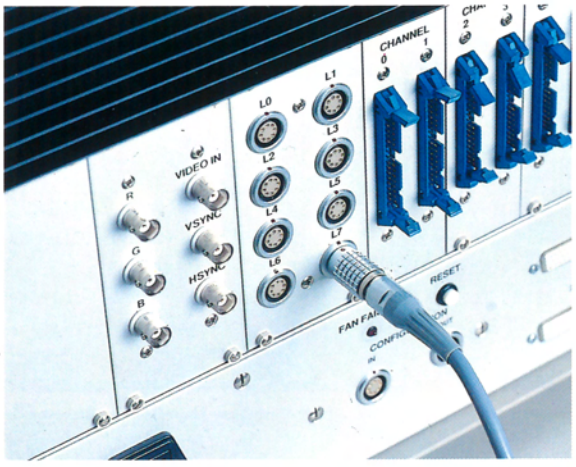
The VTF provides two fast 16-bit parallel interfaces to Transputer systems, each capable of 10 MByte/s (50 MByte/s peak performance) burst mode data I/O. Its three on-board Transputers, a T800 32-bit processor with 256K CMOS RAM and two T222s with 32K CMOS RAM, deliver a total of 30 MIPS. Each T222 controls one of the external parallel interfaces with the T800 providing control and executing applications software. Four external UniLinks are provided.

# Cables and Packaging

## Enclosures

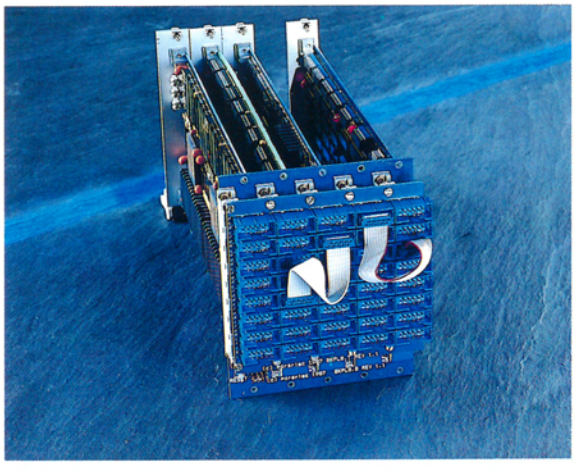
**The MultiCluster-1** system units are provided as robust enclosures 19" wide with 15 slots for UniLink modules in single-height Eurocard format.

**The MultiCluster-2** system unit has two double-height slots for NCUs and 16 single-height slots for UniLink processor modules providing up to 32 Transputer nodes. A further six slots form an I/O subsystem, of which two are dedicated to mass storage control. The rear panel has 8 Lemosa connectors for UniLinks connecting to host systems (e.g. BBK-V2, TPM-PC) and 32 DIN UniLinks for local expansion. It is supplied with power supply, fan unit and cables.




**The MultiCluster/BP** is a five-slot backplane element providing both power rails and an eight channel-per-slot serial connection for UniLink modules. It is designed for operation with MultiCluster-1 units, but may also be incorporated into custom enclosures for specific applications.

By means of the backplane's Berg female UniLink connectors, cables may be used to configure the system link topology.



## Cables and Connectors

A comprehensive range of cables and accessories is available, including twisted pair cables for UniLink connections, backplane ribbon cable links, and adapters such as Lemosa-to-Berg, or BNC cables for video I/O.

| | |
|---|---|
| LNK-1 | A 1.5m cable assembly for UniLinks with Lemosa connectors at both ends. It supports data rates up to 20 Mbit/s |
| LNK-10 | A 10m cable assembly for 20 Mbit/s external links as above. |
| LNK-30 | A 30m cable assembly for UniLinks, supporting data rates up to 10 Mbit/s. |
| LNK-INMOS | A 1m cable assembly to interface between Lemosa connectors and Inmos B004 style modules. |
| LNK-Lemo-Berg | A 2m Cable with a Lemosa male connector and a Berg female connector. |
| BP/LNK | A pack of 10 link cables providing interconnection of UniLink modules inside MultiCluster-1 or backplane. |
| RGB-BNC-Sub-9D | A 2m cable for GDS or TFG comprising three BNC connectors to a Sub-9D connector for RGB output. |
| RGB-Lemo-Sub-9D | A 2m cable for GDS or TFG comprising a Lemosa male connector to Sub-9D connector for RGB output. |
| RGB-Lemo-BNC | A 2m cable for GDS or TFG comprising a Lemosa male connector to three BNC connectors for RGB output. |
| RGB-BNC-BNC | A 2m cable for GDS or TFG comprising three BNC male connectors on both sides for RGB output. |
| TFG-Lemo-BNC | A 2m cable for camera input to TFG comprising two BNC connectors to Lemosa male connector. |
| TFG-BNC-SCART | A 2m cable for TFG comprising four BNC connectors to SCART connector for RGB + sync output. |
| LNK-CONV-4 | A converter box for interfacing four TTL links (e.g. Inmos modules) to UniLinks. |

Additional cable assemblies for power supply, monitor and keyboard interconnection are also available.

# Summary

| Product | Transputers | Memory/Node | UniLinks |
|---|---|---|---|
| **Processor Modules** | | | |
| MTM-2 | 2 x T800 | 1-8 MB | 8 |
| MTM-4-6 | 4 x T222 | 64 KB | 8 |
| TPM-16 | 1 x T800 | 16 MB | 4 |
| TPM-32 | 1 x T800 | 32 MB | 4 |
| TPM-I/O | 1 x T800 | 2 MB | 8 (incl. 1 DBT) |
| TPM-SIG | 1 x T800 | 4 MB + 4 MB | 4 |
| **Processor Daughterboards** | | | |
| DBT-1 | 1 x T800 | 1 MB | 4 (via DBC) |
| DBT-4 | 1 x T800 | 4 MB | 4 (via DBC) |
| DBT-8 | 1 x T800 | 8 MB | 4 (via DBC) |
| DBT-16 | 1 x T800 | 16 MB | 4 (via DBC) |

| Product | Transputers | Function | UniLinks |
|---|---|---|---|
| **I/O Modules** | | | |
| TPM-ADC1 | 1 x T222 | 16 ch 12-bit A/D | 4 |
| TPM-DAC1 | 1 x T222 | 8 ch 12-bit D/A | 4 |
| TPM-DIO | 1 x T222 | 32 ch digital I/O | 4 |
| VTF | 1 x T800, 2 x T222 | Two 16- bit parallel ports | 4 |
| GDS-1 | 1 x T800 | 1024 x 768 graphics, 265 col | 4 |
| GDS-2 | 1 x T800 | 1280 x 1024 graphics, 16M col | 4 |
| TFG | 1 x T800 | 1024 x 512 frame grabber | 4 |
| MSC | 1 x T800 | Mass storage controller | 4 |
| TPM-ETN | 1 x T800 | Ethernet interface | 4 |
| **I/O Daughterboards** | | | |
| DBI-1 | | 4 RS-232 serial ports | |
| DBI-2 | | 16 ch digital I/O | |
| DBI-3 | | IEEE-488 interface | |
| DBI-4 | | Serial link to parallel | |
| DBI-5 | | Prototyping board | |

**Processor clockspeeds are 20, 25 or 30 MHz with the appropriate DRAMs to allow memory access down to 3 cycles.**

# System Software

## Range of Software

A comprehensive range of software is available for Parsytec's parallel systems, from Helios and the MultiTool development environment through familiar programming languages such as C and FORTRAN. System utilities and development support packages for computational mathematics, data manipulation and graphics are also available.

Software support is available for Parsytec hardware in most common environments. Like Parsytec hardware, this has been designed to make full use of existing programming investment whilst maximising the benefits of parallel processing.

Software is available to support every level of application, from evaluation and training on PCs, to massively parallel supercomputers hosted by VAX systems or Sun workstations. It is simple to convert existing code to take advantage of parallel computing.

## Development Support

The distributed operating system Helios, running on the Transputer, is an implementation of the industry standard UNIX. Like UNIX, Helios provides multiuser, multitasking capabilities, whilst offering multiprocessor support. All Parsytec hosts are supplied with server software running in their native operating system such as MS-DOS, SunOS, or VMS.

TDS-compatible development is supported by MultiTool, Parsytec's extension to the Inmos Transputer Development System.

A wide range of system utilities are available, from debugging tools to graphics drivers. Application libraries provide support for complex computationally intensive work such as Computational Fluid Dynamics.

## Languages

Parsytec supports parallel programming languages for applications development in most common environments. Standalone compilers are available for Par.C, Logical Systems C, 3L products and ADA running on IBM PC XT/AT and PS/2 and Sun workstations.

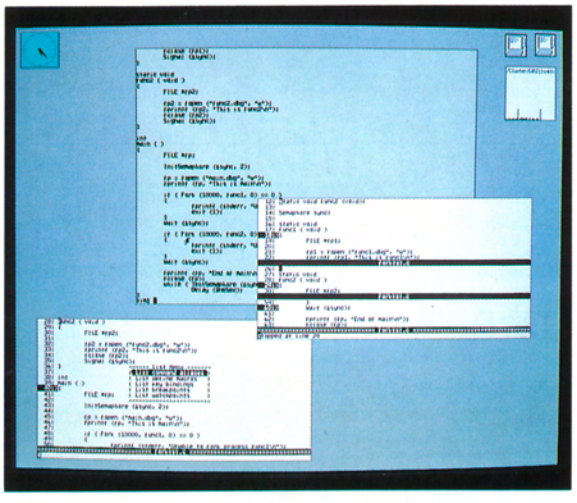
There are Helios compilers for C, FORTRAN, Pascal and Modula-2. The MultiTool development environment supports Occam2, C, FORTRAN, Pascal and Prolog.

# Development Environments

## Helios

Helios provides a multiuser, multitasking environment with a UNIX-like user interface. It is a truly distributed operating system based on the client-server model, communicating with host systems via servers running on a variety of operating systems, including MS-DOS, PC-DOS, SunOS, UNIX and AppleOS. Servers may be distributed across a network of processors and different clients access arbitrary resources by sending device-independent messages to servers.

A number of key industry standards are embodied in Helios. The Helios programming and user interface implements major parts of the proposed POSIX standard for UNIX. Helios compilers all meet existing or proposed ISO or ANSI standards.



To maximize the benefit to users, Parsytec has exclusively supplied an extended version of Helios: Parsytec-Helios includes many improvements and enhancements in functionality and performance, including facilities to manage multi-processor networks of nearly any size.

## Parallel Programming with Helios

Programs may be written in familiar sequential programming languages such as C or FORTRAN, with their parallelism described by a simple high-level language called the Component Distribution Language (CDL).

The CDL allows the user to define simple application specific communication topologies such as farms, pipeline and grids, or systems of arbitrary complexity.

This information is sufficient to enable Helios automatically to distribute the software across multiple processors, transparently to the user.

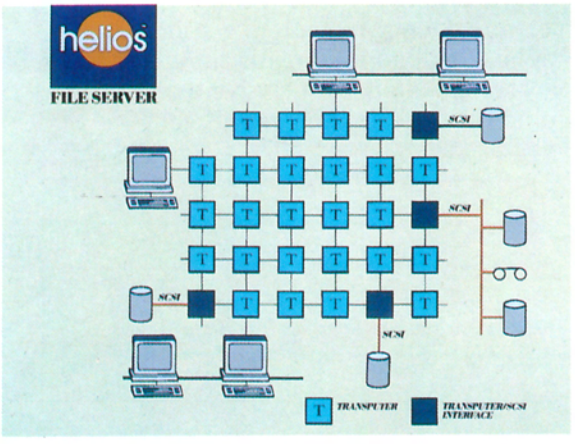
Furthermore, Helios can adapt itself to the number of free Transputers available to the user. This means that program developers do not have to amend their code when the processor topology changes.

Parallel programs developed on a single-Transputer system can be ported unchanged to the optimum multiprocessor configuration in order to gain the highest possible performance.

Helios is available for all major hosts including PC, Sun, and Macintosh II. It is supported by standard programming languages, as well as utilities such as a universal, multi language, parallel source-level debugger and a macro assembler.

## Helios Graphics Interface

The graphics interface for Helios, XWindow System X 11, runs on the GDS-1 or GDS-2 graphics module. Together with the implementation of the proposed POSIX-standard and the usage of ANSI or ISO specified compilers, this ensures that it is easy and straightforward to port software to and from Helios. The XWindow System environment ensures that the user becomes familiar with the system rapidly.



## Helios PC

This is a powerful software development system for use with Transputers attached to PCs, such as the TPM-PC. The package includes the Helios operating system, Helios C compiler, assembler, linker and other tools. The software interface to the PC is an I/O server running under MS-DOS.

## Helios Sun

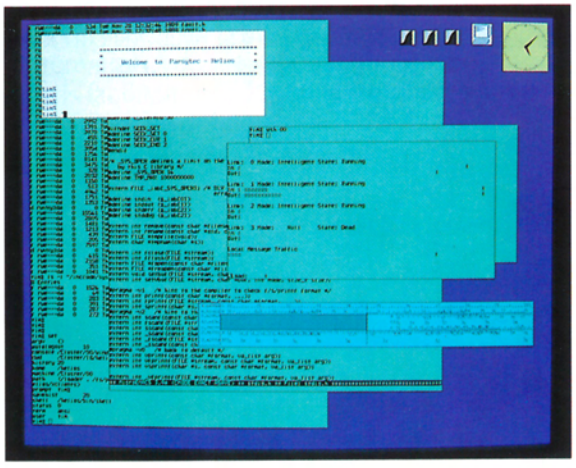
This provides a parallel processing environment for Sun workstations with Transputer systems attached (e.g. the MTM-SUN). This implementation of the Helios operating system is fully integrated into the Sun networking and windowing environment.

Helios may be run from any workstation in a Sun network, not necessarily one that has a Transputer attached. If required, users may run more than one Helios server from the same workstation. Helios sessions run in multiple SunView windows and Helios is controlled using standard Sun icons, menus and buttons.

## MultiTool

MultiTool provides a consistent Transputer programming environment across a broad range of host computer systems.

It is supported by a range of popular development hosts such as the PC/AT, VMEbus OS/9 systems, Sun 3/4 and Apple's Macintosh II.



MultiTool provides a familiar interactive folding editor for program development, compatible with the Inmos TDS. Consistent with the latest TDS versions, it supports the full Occam2 implementation, with features such as usage and alias checking to improve program reliability, diagnostics to aid debugging, and multiprocessing support.

The extended capabilities of MultiTool include the support provided by enhanced libraries, direct access to host computer resources through Occam channels and a consistent development environment for familiar high-level languages other than Occam.
3L's FORTRAN, Pascal and C are currently available to link with Occam in the MultiTool programming environment.

MultiTool also makes it easier to transfer single and multi-processor applications to standalone target systems. Furthermore, investment in existing Inmos and compatible modules and software is preserved when migrating to MultiTool, which supports both Parsytec and Inmos hardware.

## Occam 2 Toolset

This is a cross-development system for IBM PC, Sun or VAX, supporting machine code, Occam2 and mixed language (C, FORTRAN, Pascal) applications. Simulation and source-level debugging aid applications development. The toolset is readily used with project management and source control utilities.

The Occam2 Toolset can produce code for any Transputer device, even networks of mixed Transputer types. It supports multiuser platforms, allowing programmers to work in parallel, with source and binary files compatible across PC, Sun and VAX hosts.

# Languages

## Standalone Compilers

### The Par.C System (Parsec)

This provides extensions of standard C to take full advantage of parallel programming: PAR to start concurrent processes; CHANNEL to enable communication between processes; and SELECT to wait for the first of a number of defined events.

Programming is aided with automatic stack management and unrestricted multi-Transputer file I/O. Full ANSI runtime libraries include fast optimised maths routines for T8xx Transputers.

The Par.C System uses a network analyser, whilst booting, to pass all hardware information to the program as variables. The software can be made to adapt itself automatically to the available hardware resources each time it is started. Native and cross system versions are available. In addition to the standalone version of Par.C there are also versions available to run it under Helios and MultiTool.

### C (Logical Systems)

This is a C compiler conforming to the ANSI standard. LSC is available as a pure standalone cross compiler with a loader for Transputer networks. The compiler has been highly optimised and has an extended library to support Transputer computation and communications.

### ADA (Alsys)

Validated by the US Government Ada Joint Program Office, the Alsys compiler allows distributed ADA applications to be implemented by linking with Occam (Toolset required). The compiler includes specific optimisation routines amongst its development tools.

ADA is supplied with a Multi-Library Environment to aid distributed programming and development. A key advantage of both ADA and Parsytec Transputer-based systems is that programming and development effort can be allocated to teams working simultaneously on the same system. A cross compiler is available for VAX-hosted systems and a native compiler for PC hosts.

## Standalone and MultiTool Compilers

### Parallel C (3L)

This is a full implementation of the K&R specification, including additional language and library features from the ANSI standard. Programs can be linked with Parallel Pascal and FORTRAN.

The language has parallel programming support with ability to create multi-threaded tasks dynamically. In addition, C routines can access host PC facilities through MS-DOS.

### Parallel FORTRAN (3L)

This product fully implements ANSI X3.9-1978, with language extensions and additional tools to support parallel programming. It includes support for multi-threaded tasks, access to communications links and timer channels.

Object code is compatible with 3L Parallel C and Pascal as well as Occam, enabling mixed-language programming. In addition, FORTRAN routines can access host PC facilities through MS-DOS.

### Parallel Pascal (3L)

This compiler is a full ISO 7185 implementation with all the language extensions and software tools needed to write multi-Transputer parallel applications.

Optimised for either T4 or T8, the compiler takes advantage of Transputer-specific hardware facilities. In addition, Pascal routines can access host PC facilities through MS-DOS.

## Helios Compilers

### C

This C compiler conforms to the ANSI standard. It is fully integrated with Helios, and C programs can access system and parallel programming facilities through Helios system calls.

For mixed language programming, C code can be linked with assembler, FORTRAN and other languages. Run time libraries based on the emerging POSIX standard mean compatibility with UNIX. Over 100 library functions, including support for multithreading within tasks are provided. The generated code is compatible with the Helios source debugger.

### FORTRAN 77

This product is a FORTRAN 77 compiler to ANSI X3.9-1978, and includes all standard intrinsic functions and I/O operations.

FORTRAN programs can make any Helios system call, giving access to system and parallel programming facilities. Code can be linked with programs written in assembler, C and other languages. The generated code is compatible with the Helios source debugger.

### Pascal (Prospero)

This ISO standard compiler has language extensions to allow direct use of Transputer capabilities such as parallel execution, inter-process communication and floating-point arithmetic.

Rapid development is ensured by fast one-pass compilation, whilst execution times benefit from global optimisation techniques. Debugging is facilitated by Probe, a supplied source-level symbolic debugger.

## Modula-2 (Rowley)

This is a fast, compact two-pass compiler generating high-specification programs running on the Transputer under Helios.
Rowley Modula-2 conforms to Wirth's edition 3 of the language, and anticipates the emerging BSI and ISO standards.

The compiler is fully integrated with Helios and includes extensions to make full use of the parallelism of multi-Transputer networks. Helios system calls can be made from Modula-2.

## MultiTool Compilers

### Occam

This compiler generates highly efficient object code and fully exploits the parallel processing capabilities of the Transputer. Configuration tools are included to allow processes to be mapped to any network of Transputers with minimal software changes.

### Prolog

This product implements the Prolog language according to the specification of Clocksin and Mellish, based on the concepts of restricted AND parallelism and the Warren Abstract Machine interpreter.

The compiler automatically parallelises existing Prolog code, providing explicit parallel rules. The compiler's runtime system transparently supports dynamic reconfiguration of Transputer systems.

### 3L Parallel C,<br>3L Parallel FORTRAN,<br>3L Parallel Pascal

These 3 MultiTool compilers are described in detail in the section "Standalone and MultiTool Compilers".

## System Utilities

### Helios File System

This product is a Transputer-based disk filing system for use with Helios. Based on the Berkeley Fast-File System (BSD 4.2 onwards), it offers high-performance data storage for Helios systems independent of the host machine.

### MultiTool Server

This server running under Helios allows Occam2 code to be developed and run on 'naked' nodes in the normal MultiTool manner.

### XWindow

The XWindow System is an implementation of version X 11 on UniLink graphics modules. Support is provided using the Parsytec GDS-1 and GDS-2 graphics cards and there is a package which allows the native Sun XWindow driver to be used with Helios.

### Computer Graphics Interface

**CGI-2D:** 2-dimensional

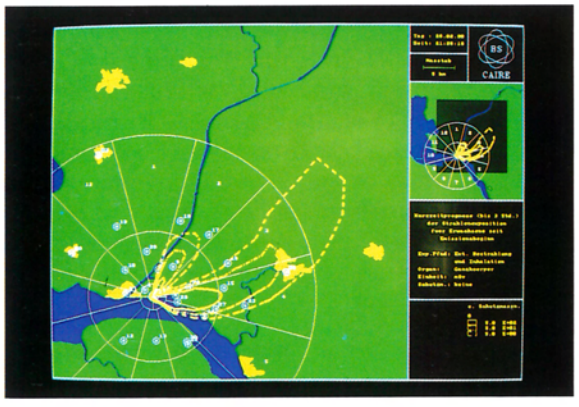
**CGI-3D:** 3-dimensional

### Graphical Kernel System

**GKS-2D:** 2-dimensional

**GKS-3D:** 3-dimensional

Existing applications such as editors, CAD systems, and process control systems are easily integrated with the industry standard graphics systems CGI and GKS. Both standards are available for two- and three-dimensional operations. Using an XWindow driver these tools can easily be integrated into the Helios environment. Language bindings are available for Helios-C and FORTRAN.



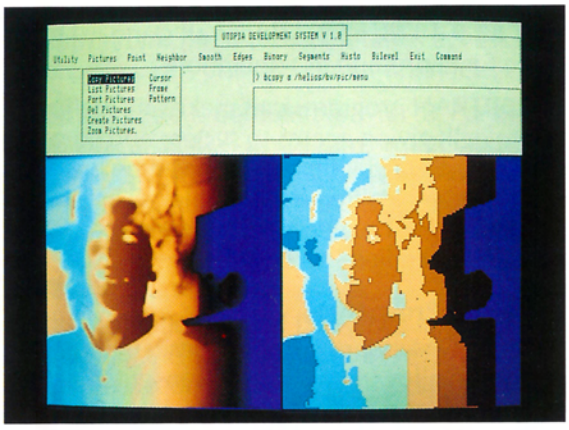

## Development Support

### UTOPIA

**U**nix-oriented **TO**ols for **PI**cture processing **A**pplications is a consistent and hardware independent programming environment for the rapid development of image processing systems.

Its open architecture has a multilayer shell structure aimed at improving the portability of image processing software, by offering an open and consistent development environment for a wide range of hardware from different manufacturers.

Standard types of algorithms can be directly integrated into systems and quickly modified to suit specific applications. The shell model of UTOPIA eliminates the need to change algorithm implementation for new Transputer network topologies or for special-purpose hardware such as digitizers and frame stores.




Running under Helios, UTOPIA fully supports distributed multiprocessor and multitasking. Drivers and servers are currently available for the Parsytec TFG frame grabber, GDS-1 and GDS-2 graphics display sub-systems. UTOPIA is supplied with libraries of device drivers and applications, including more than 100 image processing routines.

### AMPP Assembler Macro PreProcessor

AMPP has been produced to help software developers to write more compact and clear code under Helios. Programmers can write in a high-level macro notation, which AMPP converts to assembly code.

A library of more than 30 macros supporting procedure, structured programming and data structuring is provided, together with all the facilities required for creating new macros. Helios system calls are available to permit intercalling between assembler and high-level languages such as C and FORTRAN.

### Helios Source Debugger

This product is a source-level symbolic debugging tool with an extensive range of available commands. It displays source code in windows for each concurrent Helios task. Tasks can be individually single stepped, traced or run to breakpoints, allowing users to investigate interactions between parallel tasks. It also supports multithreaded tasks. When a fork is encountered, the debugger window automatically splits to show both processes.

Comprehensive facilities are provided to evaluate expressions, providing type and scope information. The debugger may be run on its own separate processor in a system running under Helios. Modules written in C, FORTRAN 77 and Modula-2 can be examined.

### Tbug

Tbug is a source-level debugger for 3L parallel compilers, running standalone on MS-DOS or SunOS hosts. It handles concurrent processes, displaying them in multiple windows. The debugger runs on a separate processor from the application, allowing the program execution to be observed and controlled statement by statement.

### TNT-XRF

This product is a tool for analysing MultiTool generated code. It can provide information for improving and optimising Occam code. It generates sorted lists of all user-defined names (channels, variables etc.) as well as a line-numbered program listing with indentation. It assists the programmer by warning of uninitialised variables and identifying variables declared but not used.

### TNT-PFY

This product is a real-time performance analyser running under MultiTool. It displays relative and absolute CPU time for each process and provides a summary of all internal communications, including the number of communications and the number of bytes transferred across global channels. System performance can be improved significantly by highlighting communication and computation bottlenecks in Occam programs and taking appropriate action.

### Topexpress Vector Library (VecLib)

The Topexpress Vector Library contains over 100 single precision, double precision and complex vector primitives, written in optimised T800 assembler.

VecLib routines can be called from Helios C and FORTRAN, 3L FORTRAN, 3L C or Occam. Included with the library is an executive which maximises performance by dynamically loading library code into on-chip RAM.

### Topexpress Mathematical Procedure Library (MathLib)

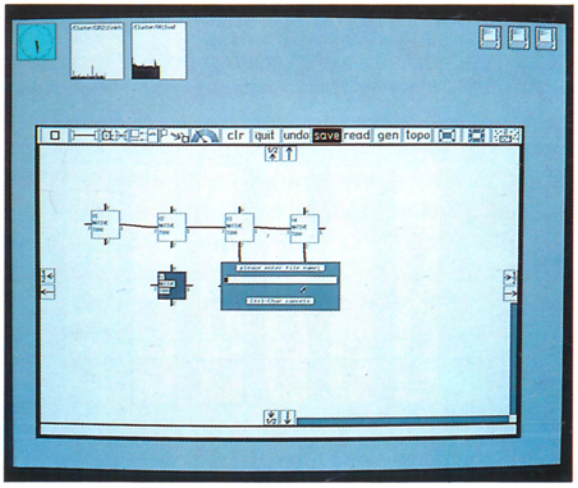
The Topexpress Mathematical Procedure Library comprises over 50 numerical algorithms important for scientific and engineering applications. The procedures are numerically efficient, having been optimised for the T800 Transputer using assembler where necessary, and are available in single and double precision versions.

The routines include matrix procedures, sparse matrix solvers, eigenvalue/eigenvector procedures, FFTs, Bessel, gamma, Legendre and error functions, sorting, optimisation, curve fitting and polynomial finding procedures.

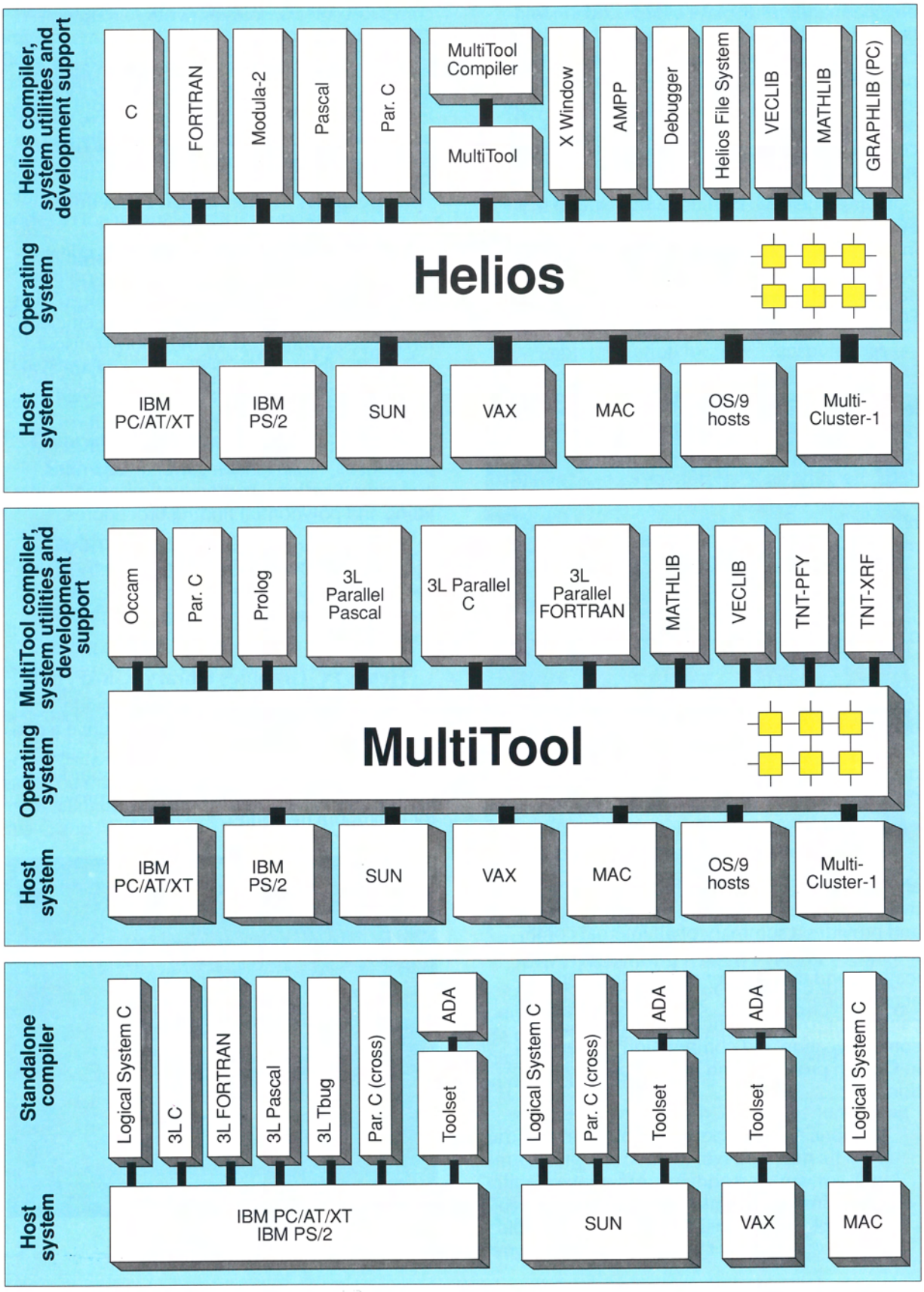
Running under Helios C and FORTRAN, 3L C, 3L FORTRAN and Occam, the library includes an executive which can maximise performance by dynamically loading code into on-chip RAM.

### Helios PC Graphics Library (GRAPHLIB)

The Helios PC graphics library provide Transputer applications programs to drive a range of standard PC graphics cards. The package works with CGA, EGA, and VGA standard modules. Source code for Microsoft C is provided for maximum flexibility.



# Summary


Helios compiler, system utilities and development support
C
FORTRAN
Modula-2
Pascal
Par. C
MultiTool Compiler
MultiTool
X Window
AMPP
Debugger
Helios File System
VECLIB
MATHLIB
GRAPHLIB (PC)
Operating system
Helios
Host system
IBM PC/AT/XT
IBM PS/2
SUN
VAX
MAC
OS/9 hosts
Multi-Cluster-1
MultiTool compiler, system utilities and development support
Occam
Par. C
Prolog
3L Parallel Pascal
3L Parallel C
3L Parallel FORTRAN
MATHLIB
VECLIB
TNT-PFY
TNT-XRF
Operating system
MultiTool
Host system
IBM PC/AT/XT
IBM PS/2
SUN
VAX
MAC
OS/9 hosts
Multi-Cluster-1
Standalone compiler
Logical System C
3L C
3L FORTRAN
3L Pascal
3L Tbug
Par. C (cross)
ADA
Toolset
Logical System C
Par. C (cross)
ADA
Toolset
ADA
Toolset
Logical System C
Host system
IBM PC/AT/XT
IBM PS/2
SUN
VAX
MAC

# Technology based Services

## Successful Application - Parsytec's Technology Services

With more than 5 years experience in the design and supply of high performance parallel systems, Parsytec has built up a unique and wide-ranging parallel processing expertise. To match the rapidly growing world-wide demand and to make this expertise readily available to our customers, Parsytec established daughter companies in major areas including Germany, USA, UK and Eastern Europe.

The focus of these technology based service companies is the distribution and technical support of Parsytec systems and software. Hardware integration and custom software development are among the services offered by Parsytec Anwendungen GmbH in Germany, Parsytec Inc (formerly Paracom Inc) in the U.S. and Parsytec Ltd. in Great Britain. Furthermore, distributors give local support in most European countries, the Far East, Australia, and Africa.

These technology services form a significant part of our product portfolio and constitute an area of our business which we are systematically enlarging.

## Projects

In areas including design, system development and integration, implementation of applications, installation and commissioning of equipment, Parsytec has years of specialist experience in parallel processing. For all or part of a project, Parsytec's technical skills can complement the user's own resources.

## Project Management

Extensive experience in large-scale projects enables Parsytec to contribute significantly to your development work. Our expertise is confirmed through our participation in major projects such as an ESPRIT programme to design new generation parallel systems.

Parsytec has available experienced project management specialists, who can help you to meet the most stringent project deadlines. For instance, Parsytec has collaborated with two other companies to develop a monitoring system for a nuclear power plant. With the involvement of Parsytec, the 18-month project was completed on time and within budget.

## Custom Engineering

For specific customer requirements, Parsytec can also develop hardware and software, integrating them to provide complete solutions. This service is directed at the OEM market. Parsytec has designed and manufactured interfaces to connect customers' own hardware to Parsytec systems. An example of this has been the development of a prototype monitoring system for process control, which will be manufactured in high volumes by the customer. Bespoke software developments such as the porting of software tools to Silicon Graphics systems and to Motorola UNIX V systems have been undertaken.

## Specialist Contract Programming

Parsytec's team of programmers has successfully undertaken a wide range of contract projects, which range from the implemention of parallel and distributed algorithms, to the development turnkey software complete with user interfaces. Whether the requirement is for a single programmer working as part of the customer's development group, or for a complete software team dedicated to a project, Parsytec can fit the bill. As an example of this we have implemented a complex signal processing and data analysis system for a customer. This system has a sophisticated user interface and has reduced the turnround time for analysing a data set from 20 minutes to less than 30 seconds.

## Consultancy

### Systems Integration

Parsytec have extensive experience accross a wide range of Transputer systems and applications. Consultancy clients have the ideal partner for analysing system requirements and finding the most appropriate integration strategy. With expertise varying from real-time industrial systems to computationally intensive scientific applications, Parsytec can contribute significantly to the task of systems design and integration.

### Feasibility Studies

An important part of Parsytec's technology based services is the use of feasibility studies to evaluate the most appropriate parallel technology for specific applications. For example, Parsytec has successfully completed a task to evaluate the applicability of transputers to industrial tomography (see inset).

### Benchmarks

Parsytec can also run standard or application specific benchmarks for evaluation purposes. Since the performance of parallel systems is highly application specific, traditional benchmarks may not be appropriate. Parsytec has considerable expertise in designing benchmarks that are relevant to real problems and actual parallel applications.

### On-site Evaluation Projects

To meet the needs of individual customers, Parsytec can tailor an evaluation package comprising: the loan of an appropriate system including hardware, software and interfaces; technical advice and system design; prototyping support; and short training courses. This service provides a low risk, low cost approach to verifying the effectiveness of a parallel solution.

## Application Packages

Help is available to select the most appropriate third-party software. Parsytec can assist vendors in porting standard applications packages and libraries onto Parsytec hardware and software systems.

## Quality Control

### Application

Computer tomography i.e. the reconstruction of high-resolution images from multiple projections.

### Requirement

To reduce computation time to allow online quality control, whilst minimising the number of Transputers to reduce costs.

### Parsytec's Approach

Existing sequential code was rewritten in Occam and optimised. Parsytec evaluated the customer's algorithm to identify the best parallel strategy. With a pipeline chosen as the most appropriate topology, parallel code was then implemented and optimised accordingly.

### Result

The customer originally estimated that 120 Transputers would be necessary. Parsytec demonstrated that a 32-Transputer system would meet the customer's requirements.This saved around $100,000, an order of magnitude more than the consultancy fee involved.

## Training and Education

The use of parallel machines requires the development of new methods of programming. Parsytec's training and education programme shows how these new methods are simple and intuitive.

### Training Courses

Parsytec holds regular courses in programming languages, such as the Par.C System and Occam, and development environments, such as Helios and MultiTool. As well as Parsytec's training facilities in Aachen and Chicago, local technical support is also available for advice on the best ways to develop customer's parallel systems skills. Furthermore, Parsytec can provide an on-site education programme according to specific customer requirements. By using modular course materials, even the training of small groups with specialized needs becomes cost effective.

### In-Project Training

Parsytec can make a significant contribution to projects by providing expert assistance at project inception. Participating in the development of a parallel application is a good

opportunity for a customer's technical staff to learn practical parallel programming skills. Working alongside experienced programmers and system specialists, staff gain a valuable insight into the capabilities of Transputer based systems.

### Customer Training

Every large Parsytec system comes complete with all the training necessary to exploit its multiuser, reconfigurable facilities to the full. Users learn how to define, configure and maximize the performance of their optimum virtual machine, while network managers are taught how the physical machine can provide all the resources users demand.

## Simulation System

### Application

Real-time simulator for a car manufacturer

### Requirement

To provide real-time performance, the customer needed to reduce the execution time of a sample simulator module to less than 200 microseconds.

### Parsytec's Approach

Existing FORTRAN 77 source code was compiled to run on Transputers. A first trial of the sequential differential equation program resulted in a 2 millisecond execution time.
FORTRAN code was then converted to Occam so that low-level instructions could be parallelised. The partially parallel algorithm was optimised to run on a single Transputer, then the full parallel program was ported to a three-Transputer system.

### Result

Parallelisation and other optimisations resulted in a cycle time of 192 microseconds. The prime goals of the project had been achieved.

### Awareness Seminars

Parsytec's parallel technology awareness seminars are aimed at senior management and project leaders so that they can gain a full understanding of the benefits of parallel systems.

### World-Wide Local Support Centres

The world-wide Parsytec and distribution network gives rapid, reliable pre- and post-sales technical support from local centres in over 15 countries, including Australia, Benelux, France, India, Japan, Scandinavia, UK and USA.

A dedicated team of technical specialists is always available by telephone to solve applications and system configuration problems, as well as queries on Parsytec hardware and software.

### Maintenance

Parsytec parallel modules are easy and quick to replace in the rare event of system failures. Unlike conventional sequential systems, parallel computers may continue to function while replacement modules are in transit. With rapid module replacement by Parsytec, immediate call-out is less urgent. Nevertheless, there is the assurance of worldwide support from local technical centres. Critical systems can benefit from the guarantee of a very low down-time at a minimal cost.

## Nuclear Power Plant Monitoring

### Application

Data monitoring, calculation and display of atmospheric pollutants in a nuclear power station.

### Requirement

System integration, including colour graphics display, and the development of a network, fore forecasting algorithms to predict toxic cloud growth and dispersal.

### Parsytec's Approach

Collaborating with two other companies, Parsytec provided project management as well as technical consultancy. We devised numerical algorithms for interpolation and simulation, providing system integration and networking.

### Result

The 18-months project met all performance, cost and time goals. The system is now operational.

# Worldwide

**Distributors in:**

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