inmos®

DEVELOPING

WITH THE

TRANSPUTER

The Transputer Family

- Powerful single chip processors
- Multiprocessing made simple
- Scalable performance
- Extensive software support
- Modular system design
- Reduced system cost

The transputer family is a range of 16 and 32-bit microprocessors supported by peripheral products and software and hardware development tools. The transputer is firmly established as the industry standard for parallel and multiprocessing, as well as being a powerful single chip processor. It is designed into a wide range of embedded systems and high performance computing applications.

This brochure describes the first generation transputer family, launched in 1985, and includes the IMS T225, IMS T400, IMS T425, IMS T426 and IMS T805 products. The second generation IMS T9000 family is described in detail in the IMS T9000 family brochure.

The transputer not only offers low system cost for single processor designs, but also offers a unique multiprocessing capability which allows the easy construction of modular systems with multiple transputers. This capability is derived from the transputer's fast on-chip serial communications links that overcome the bus bottleneck and shared memory constraints of other microprocessors. The performance of a transputer-based system is totally scalable because the processing bandwidth increases linearly as more transputers are added.

Software written in any of the standard languages such as C, C++, ADA or occam can be executed sequentially on a single transputer; the transputer's serial communications links and hardware scheduler allow the same program to be distributed as a series of processes over a network of transputers.

This gives designers the flexibility to build systems with unlimited performance and the ability to build a range of integrated products with processing power tailored to suit the cost/performance requirements of the end user.

The transputer family is supported by a complete range of software cross-development tools for Sun and PC hosts which enable customers to bring product to market ahead of the competition. Compilers for ANSI C, C++ and occam are available, along with a wide range of standard software debug tools with special software support for message routing, profiling and performance optimisation.

For prototyping the target system, the modular *i*q systems range of TRAMs (TRAnsputer Modules) has been developed to plug into motherboards for PC and VME based systems. Full details are given in the *i*q systems Product Overview.
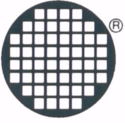
Transputer Architecture

First generation transputers share a common architecture that gives software portability between any member of the family.

The microcoded CPU executes over 170 instructions , including single cycle instructions and application specific instructions e.g. 2D block move and CRC. It combines the advantages of RISC and CISC machines, giving peak performance of 30 MIPS. T8 series transputers also have an integral 64-bit IEEE 754 floating point unit, giving a peak 4.3 MFLOPS performance.

Instruction codes can vary in length and the CPU can fetch up to 4 single byte instructions simultaneously. The instruction queue is double buffered and can pipeline 4 instructions simultaneously, keeping the CPU fully loaded and effectively decoupling the execution times from the memory speed.
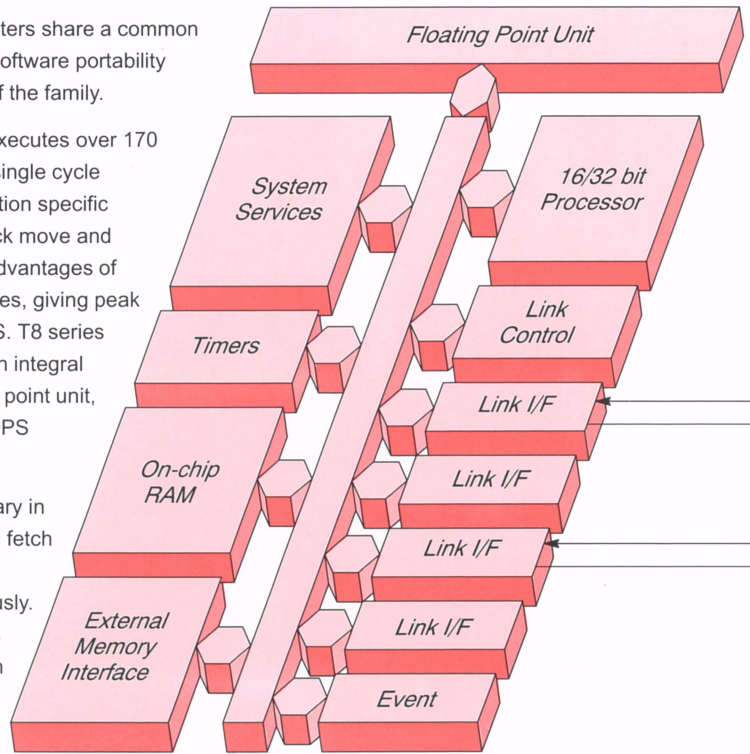

Generic block diagram of transputer

2Kbytes or 4Kbytes of on-chip single cycle SRAM speeds up program execution and allows programs to run without external RAM.

The highly configurable external memory interface addresses 4Gbytes on the 32-bit processors and 64Kbytes on the 16-bit machines, and connects the transputer to external memory with minimal external support components.
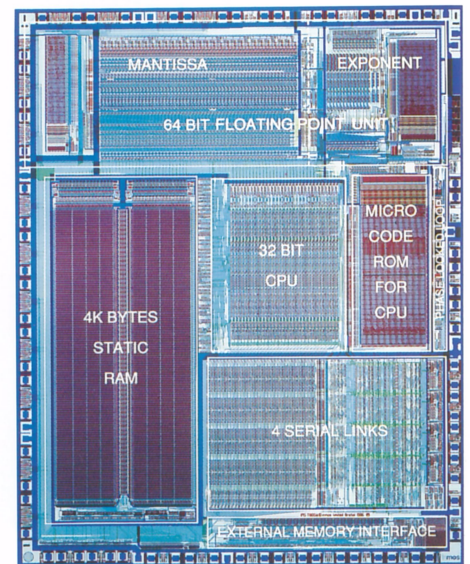
Each transputer has 1µs and 64µs hardware timers.

The event logic provides an asynchronous handshake between an external event and an internal process and can be used as an interrupt. Context switching is fast - 630ns on a 30MHz transputer - because there are only a small number of registers needing to be saved. This is important for task switching and interrupt latency.
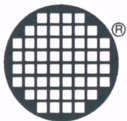
System services include an external 5MHz clock that drives an on-chip PLL for all clock speeds. Booting is from ROM or serial link. Reset/Analyse halts the transputer for debugging. Error indicates, for example, divide by zero, arithmetic overflow and so on.
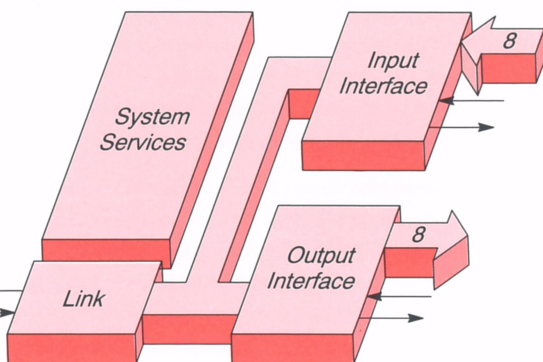

IMS T805 die

IMS C011 link convertor

The links are bidirectional 2 wire serial links running at 5, 10 or 20 Mbits/s. They act as DMA channels for multiprocessor communications between transputers or with link adaptor chips to communicate with external peripheral components such as A/D convertors and graphics or SCSI controllers. Peripherals can also be mapped into the memory interface of the transputer.

The links are available as ASIC cells so that users can easily develop their own interfaces using semicustom technology.
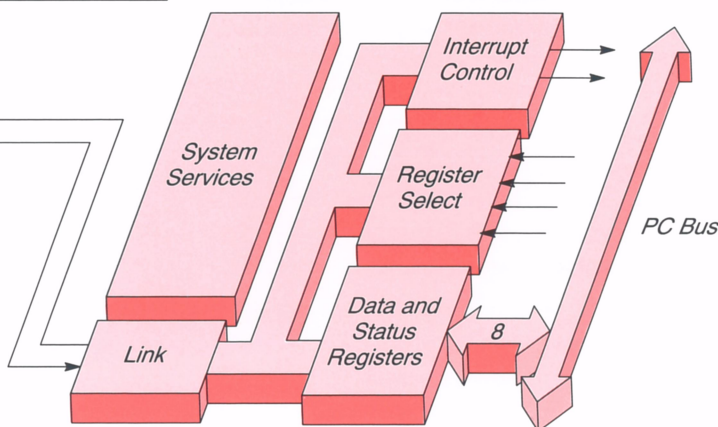
IMS C012 link to parallel bus

Transputer products and peripherals					
Family	**Part**	**Internal memory (Kbyte)**	**Number of 20Mbit/s links**	**Speed options (MHz)**	**Package options**
T2 (16 bit)	IMS T225	4	4	20, 25, 30	68 PGA/PLCC, 100 QFP
	IMS T225M	4	4	20	68 PGA, 100 CQFP, Mil Std 883
T4 (32 bit)	IMS T400	2	2	20	84 PGA/PLCC, 100 PQFP
	IMS T425	4	4	20, 25, 30	84 PGA/PLCC, 100 QFP
	IMS T426	4	4	20, 25	100 QFP. Parity on data bus.
T8 (32 bit + 64 bit FPU)	IMS T805	4	4	20, 25, 30	84 PGA/PLCC, 100 QFP
	IMS T805M	4	4	20	84 PGA, 100 CQFP, Mil Std 883
T9 (32 bit + 64 bit FPU)	IMS T9000	16	4x100Mbit/s	40, 50	208 CLCC
Peripherals	IMS C011	Link to I/O convertor/parallel bus			28 DIL/SOJ
	IMS C011M	Link to I/O convertor/parallel bus			28 DIL/LCCC, Mil Std 883
	IMS C012	Link to parallel bus			24 DIL
	IMS C004	32 way crossbar			84 PGA
	IMS C004M	32 way crossbar			84 PGA Mil Std 883
	IMS C100	Link convertor 20 to 100Mbit links			100 QFP
	IMS C104	Router			208 CLCC
For details of IMS T9000, IMS C100, IMS C104 refer to IMS T9000 family brochure.					

Simple Single Processor Systems

The transputer has been specifically designed for low system cost. This is achieved by high on-chip integration, low pin count, low cost packages and reduced board area and cost because of the minimal external support requirements.

A single transputer can be used as an autonomous processor, since it has CPU, memory and communications links on-chip. In the majority of systems, program size dictates the use of external memory. The external memory interface is user programmable to DRAM, VRAM, SRAM, EPROM, EEPROM and flash ROM. A DRAM controller is included on the transputer. A single transputer system with 16 Mbytes of DRAM is the size of a standard credit card.

Transputers have low pin count - 68 to 100 pins - and need only four signal layer PCBs. The range of packaging includes low cost surface mount options. Power consumption is typically less than 1W; an IMS T400 has typical power consumption of 450mW.

A single 5MHz clock is all that is required to drive the transputer CPU and links, removing the need to route high speed clocks. Transputers can boot from ROM or serial link, eliminating the need for external ROM.

The serial links offer reliable communications; only a 2 wire twisted pair is required for transmission up to 30cm with no external drivers. Links can be used for debugging the final system.

An example of a single processor system is the IMS B437 Compact Display TRAM which integrates an IMS T805 with 1 Mbyte of VRAM and an IMS G332 Color Video Controller. The transputer acts as a controller for the system and can run software such as CGI libraries supplied by INMOS. The IMS G332 CVC is programmable for displays up to 1024 x 1024 and up to 16 bits per pixel, supporting very high resolution images.
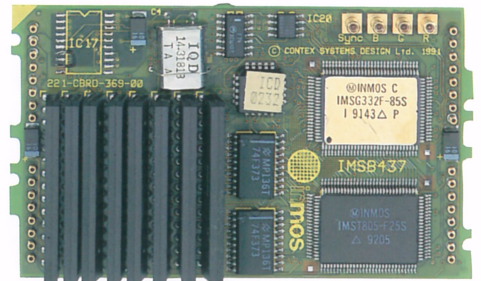
IMS B437 Compact Display TRAM
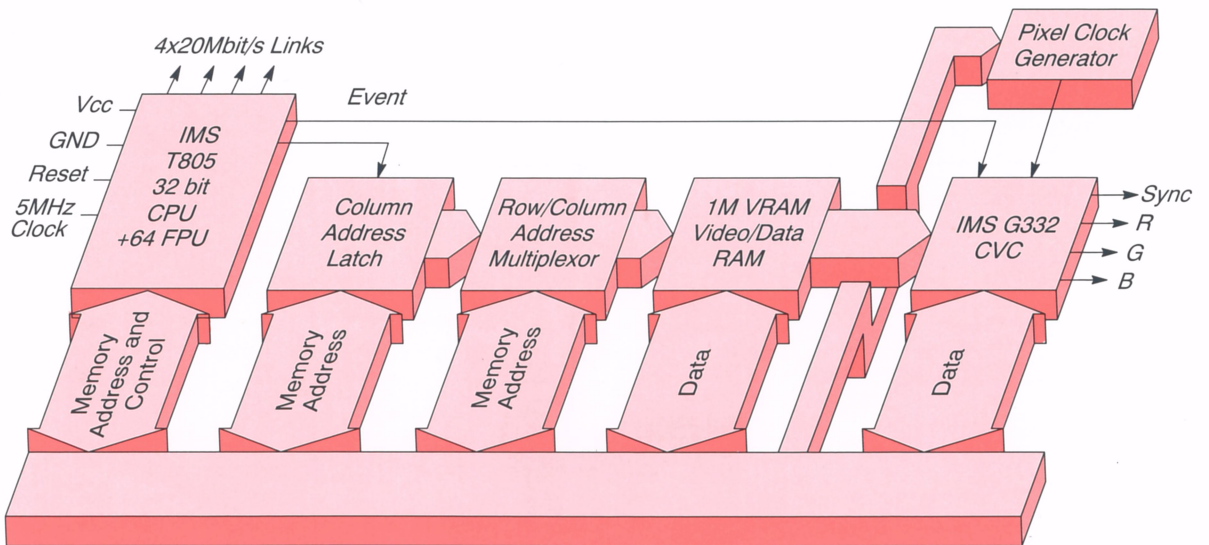
*Graphics control system using IMS T805 processor and IMS G332 CVC*

Simple Multiprocessor Systems

The transputer's architecture has been designed for multiprocessing, with communication links and a hardware scheduler. The hardware scheduler allows the transputer to switch rapidly between software processes running on a single transputer.

Software programs can be written as a series of interacting processes that communicate via channels. On a single transputer these processes are timesliced and communicate through the memory of the transputer. On multiple transputers these processes can be allocated to separate transputers and run concurrently. Communication takes place via the serial links which are DMA channels memory mapped into the transputer. In ANSI C, a series of libraries support this programming activity and the occam language features parallelism and communications as high-level language constructs.

Serial links are simple 2-wire connections requiring no glue logic, no snooping logic or bus arbitration. Standard bus architectures used for connecting conventional microprocessors limit realistic scalability to a small number of processors in a system. The upper limit for transputer scalability is rarely achieved, with current production systems using many thousands of transputers.

For building multiprocessor systems the IMS C004 32 way programmable crossbar switch provides full duplex communications between any member of the first generation transputer family. The IMS C004 is able to route from any of its 32 inputs to any of its 32 outputs. A control/configuration link is provided to allow an external processor to configure networks as required by the user.
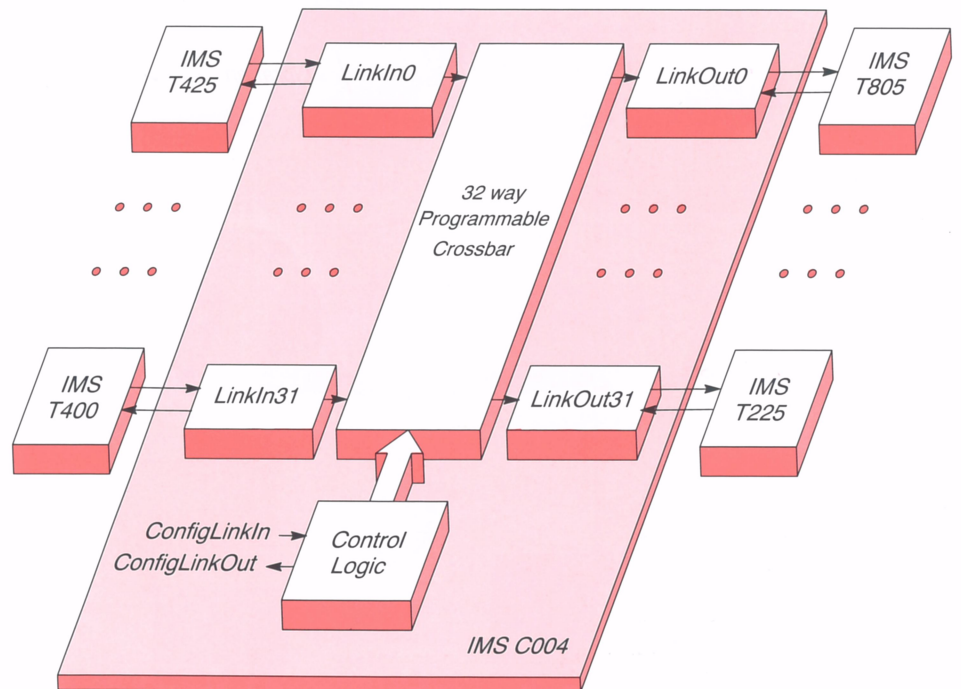
Multiprocessor system using an IMS C004 crossbar switch

Developing with the Transputer

INMOS transputer development software has been designed around the concept of a set of compilers and tools known as a Toolset running on a host machine and targeting a development environment based on the *i*q systems range of TRAMS and motherboards.
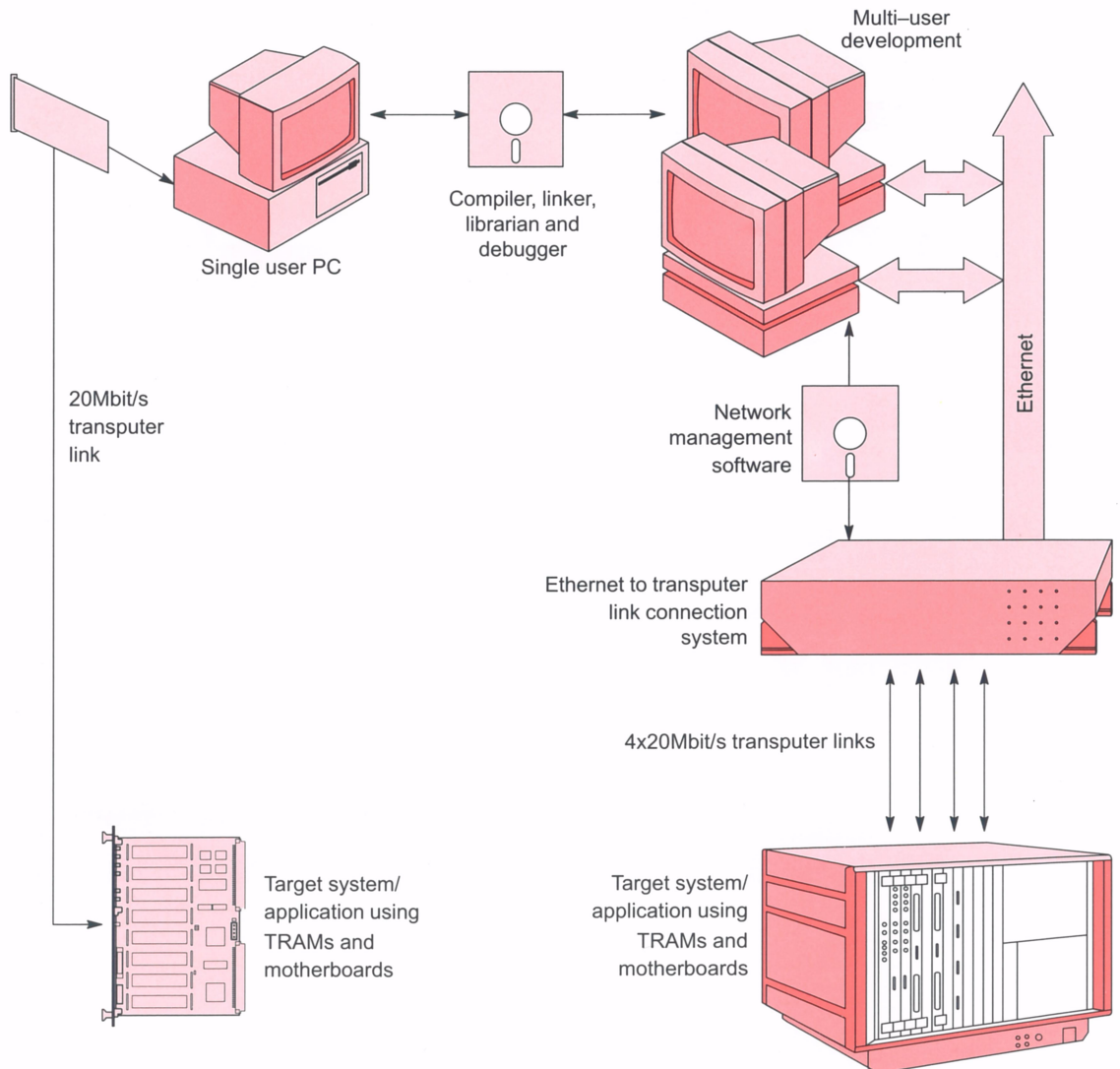
There is also extensive 3rd party support, a list of which is available in the Transputer White Pages.

INMOS provides compilers for the most commonly used languages such as ANSI C, C++ and occam. These are available on industry standard hosts such as PC and Sun workstations. Full support tools and a comprehensive set of functions are supplied with the compilers giving I/O and a full ANSI C run time system.

INMOS has developed a server technology which interfaces between the transputer network and the host operating and file systems.

For debugging, interactive tools offer breakpointing, single stepping, and post mortem debugging. Toolset options include sophisticated profiling and performance analysis tools.

The target system can be a customer's own design or it can be prototyped using the range of *i*q systems TRAMS and motherboards, allowing designers to demonstrate product concepts without investing in custom hardware up front. The Toolsets all support multiprocessing and multitasking.

Single user PC

Compiler, linker, librarian and debugger

Multi–user development

20Mbit/s transputer link

Network management software

Ethernet

Ethernet to transputer link connection system

4x20Mbit/s transputer links

Target system/ application using TRAMs and motherboards

Target system/ application using TRAMs and motherboards

Software Programming Model

Programs written in ANSI C, C++ or occam are compiled to object files (TCOFF - Transputer Common Object File Format). Mixed language facilities are supplied with the Toolsets and assembly language inserts can be made for speed-critical sections. Library functions supplied by INMOS or the user can be linked into the program and the file configured to run on a single processor or network of processors. The program is automatically distributed over the transputer network.

Bootstrap code for booting from link or external ROM is supplied by INMOS and the bootable file run on the target hardware. This software can then be run with the debugger and profiler for testing and performance evaluation.


Target system/application using TRAMs and motherboards
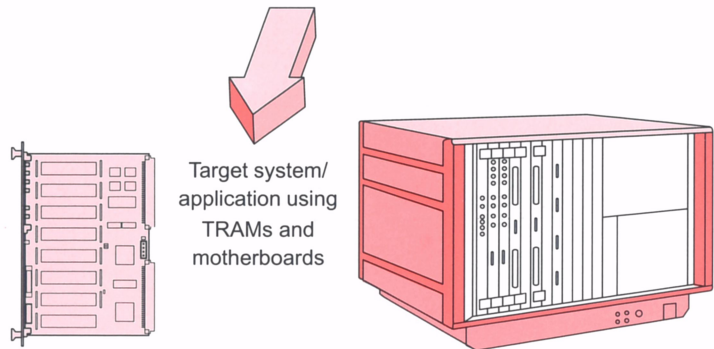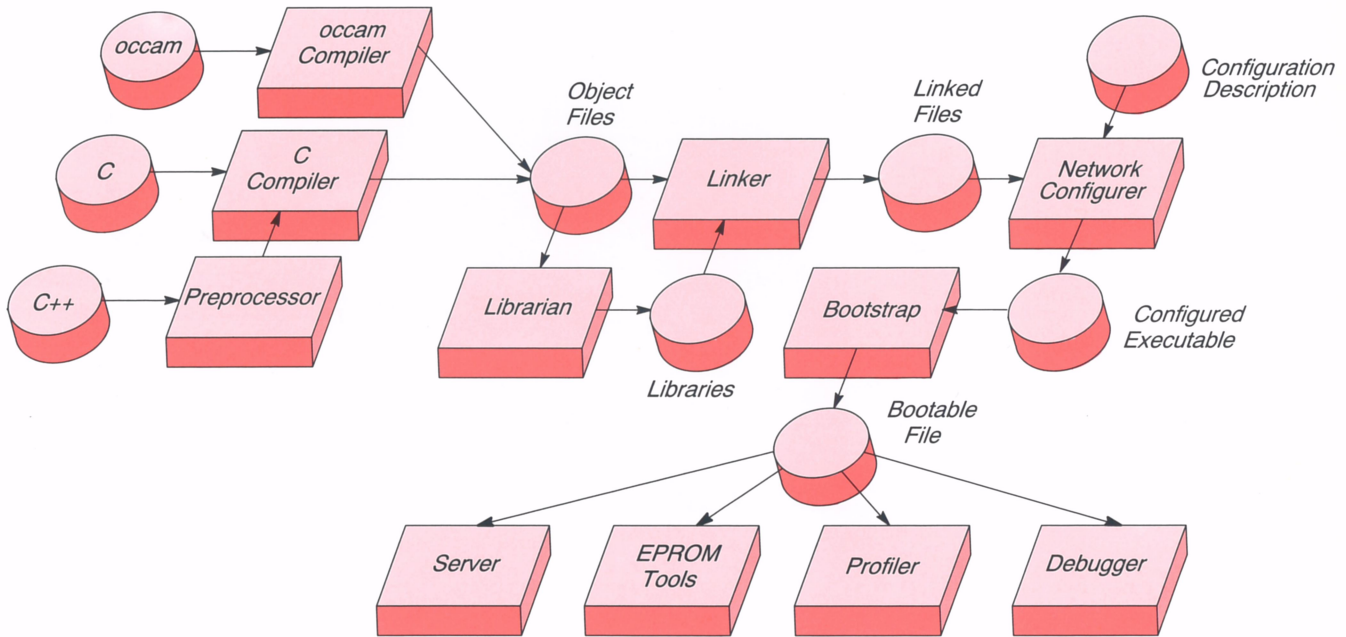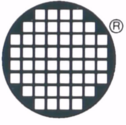
Software Development Products

Software Toolsets contain the following tools and run on the host computer (PC or Sun 4 compatible) :

- Compiler and libraries
- Linker and librarian tools
- Configuration for multiprocessor networks - optimized message routing
- Bootstrap tools
- Basic interactive debugger for single/ multiprocessor programs (breakpointing and single stepping)
- ROM programming support tools
- Transputer memory interface design tool
- Mixed language programming support
- Server technology allowing transputer programs access to host operating system facilities
- Code/data placement control
- Program/hardware cross reference mapping

The INQUEST package contains a windowing debugger and performance optimisation tools. It is compatible with all the Toolsets described above and offers:

- Windowing operation (OSF/Motif and Microsoft Windows 3)
- Single stepping of transputer instructions and source statements (with threads)
- Conditional/Programmable breakpoints and watchpoints
- Source or assembly level views
- Programmable command language
- Program interrupt and restart facilities
- Percentage of time executing each procedure
- Percentage of time at high priority for transputer
- Idle time analysis for transputer
- Percentage of time in each process
- Utilisation of network over time - displays an interactive chart.
- Remote download for booting over network
- Access to host O/S
- Integration of user supplied host services
- Distributed access to services
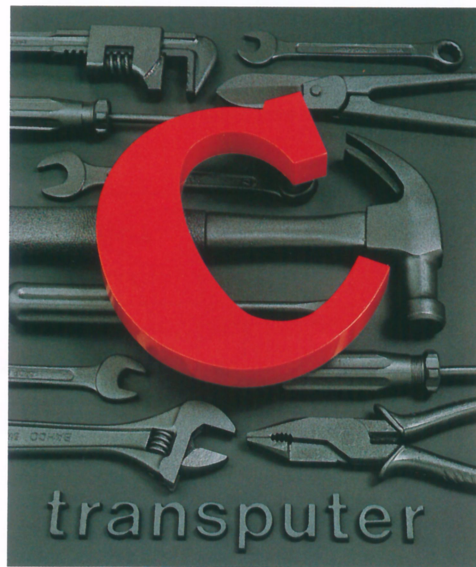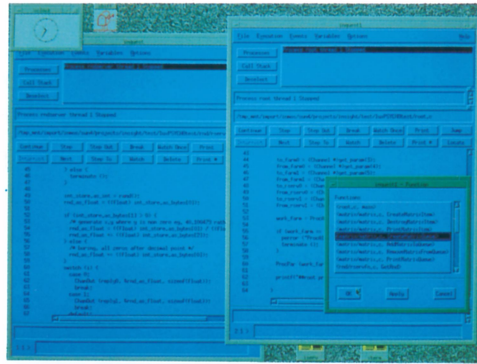
ANSI C

INMOS ANSI C Toolsets are validated using the Plum Hall C Validation Suite and certified by the British Standards Institute.

The following additional features are provided :

- Standalone and inline assembly language
- Inline functions for channel I/O and access to CRC, bit manipulation and memory block transfer instructions
- Source to bootstrap and startup code
- Libraries for transputer process creation and communications

Optimizations in the compiler include :

- Branch chaining, return chaining
- Peephole optimizations
- Workspace allocation, workspace colouring
- Common subexpression elimination
- Loop invariant code motion
- Dead code/redundant store elimination

```
/* Example Program */
#include <process.h>
#include <misc.h>
#include <stdlib.h>

/* Define prototypes for process functions */
void fmux (Process*, Channel*, Channel*,
          Channel *[], Channel *[], int);
/* process, hostin, hostout, in, out, no_workers */
void fwkr (Process*, Channel*, Channel*, int);
/* process, in, out, worker_id */

/* Main program */
int main(int argc, char *argv[], char *envp[],
         Channel *in[], int inlen,
         Channel *out[], int outlen)
{
    int i;
    /* Declare processes and channels */
 Channel *hostin, *hostout, *wkr_in[3], *wkr_out[3];
    Process *mux, *wkr[3];

    /* Allocate Channels */
    hostin=in[1];
    hostout=out[1];
    for (i=0; i<3; i++) {
        wkr_in[i]=ChanAlloc();
        wkr_out[i]=ChanAlloc();
    }

    /* Allocate Processes */
    mux=ProcAlloc(fmux, 0, 5, hostin, hostout,
        wkr_in, wkr_out, 3);
    for (i=0; i<3; i++)
        wkr[i]=ProcAlloc(fwkr, 0, 3,
            wkr_in[i], wkr_out[i], i);

    /* Start the processes running in parallel */
    ProcPar (mux, wkr[0], wkr[1], wkr[2], NULL);
}
```

Example C program

C++ Preprocessor

The C++ Toolset, developed by Glockenspiel in conjunction with INMOS, implements C++ to the latest specification. The C++ Toolset works with the INMOS ANSI C Toolset.

occam 2

Established in 1982, occam 2 is a high level language being used for applications in real time control, imaging, communications and high performance computing. It is designed to express concurrent algorithms and how they are implemented on a single processor or a network of processors.

occam describes an application as a series of processes that communicate via channels. This makes a program simple to define, and allows a system with many separate functions to be built with a modular design. A set of interacting processes can be grouped as a single program for development purposes, allowing programmers to work on small manageable sections of the system.

occam can provide a degree of security not available to languages such as ANSI C. It is backed by formal methods and mathematical proof techniques. It supports structured concurrent programming and includes sophisticated error checking at compilation reducing, debug time and the risk of time dependent errors in the system. It makes an ideal language for system specification and behavioural description and, since it is easily mapped to hardware, it may also be used for hardware specification.

Since the development of occam and the transputer are closely related, they provide an efficient combination which can also be mixed with other languages such as C and assembler.

```
TIMER clock:
INT hours, minutes, seconds, date:
PROC update.time (INT now)
  INT new.now, delta:
  SEQ
    clock ? new.now
    delta := new.now MINUS now
    now := new.now
    ... increment time/ date values
:

VAL one.hour IS ticks.per.second * 3600:
INT now:
BOOL running:
  ... Initialise
  WHILE running
    ALT
      -- wait for a timeout
      clock ? AFTER now PLUS one.hour
        update.time (now)
      ALT i=0 FOR users
        request[i] ? command \
          SEQ
            PAR
              update.time (now)
              response[i]! REQUEST.REGISTERED
            CASE command
              read.time
                response[i]!hours, minutes,
                  seconds, date
              ... handle other requests
```
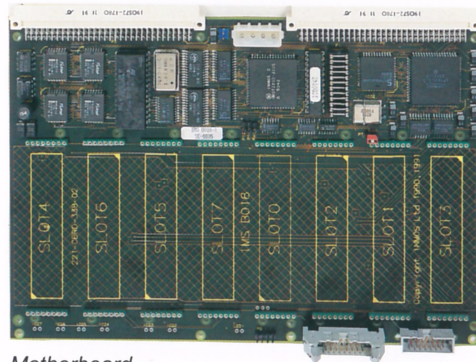
Example occam program
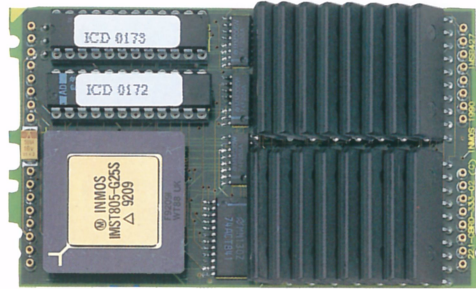
Compute TRAM

Application TRAM

Motherboard

Development Hardware

Transputer target systems can be constructed from hardware building blocks called TRAMs. TRAMs can be either compute TRAMs (combining a transputer and memory) or application specific TRAMs (interfacing a transputer to application hardware), e.g. graphics, image processing, Ethernet, or SCSI. Each TRAM is a self contained unit which uses the transputer serial links to interface to the outside world. This is an industry standard interface with many third party suppliers providing a wide range of additional functions to the INMOS products.

TRAM modules plug directly into TRAM motherboards such as PC/AT or VME bus format cards. TRAM motherboards provide a number of slots into which TRAMs can be fitted with the ability for the user to configure the network as required.

Prototyping and System Building

TRAMs and motherboards offer a cost effective way of constructing prototype and production systems. These products are sold under the brand name *i*q systems, and allow demonstration of the feasibility of an application without building custom hardware.

*i*q systems products offer a modular upgrade path as new TRAMs become available. Products can be customised without complex hardware redesign.

The IMS T9000 Family

The IMS T9000 will be available in TRAM module format for existing motherboards. In addition a new higher performance range of motherboards and modules will exploit the faster link and processing performance of the IMS T9000.

Using *i*q systems to Construct a Target System

In order to develop any microprocessor based system it is necessary to build prototype systems for debugging and for demonstration to potential customers. This job is made simple by the modular architecture of *i*q systems products.

Image Processing and Display System

A basic image processing system requires video capture, processing of the image or a region of interest and display of the processed image. This system could be assembled on a single 6U VME format card from off the shelf *i*q systems components.

The IMS B429 Image Processing TRAM takes programmable resolution images in real time and perform 1 or 2D filtering using specialist IMS A110 image processing hardware. The TRAM can capture grey scale images at up to 20 frames/s and three frame buffers perform several filtering functions on the image prior to display.

The Image Processing TRAM is supplied with software libraries with common filtering functions such as image capture, display and convolution software.

Using 3 of the 4 transputer links the image can be transferred to the IMS B437 Graphics Display TRAM which will display the image on a VGA type display. Software support for the graphics TRAM includes CGI libraries.

Additional TRAMs could be added to the system such as an RS232 TRAM for mouse control and a Flash ROM TRAM for booting the system.
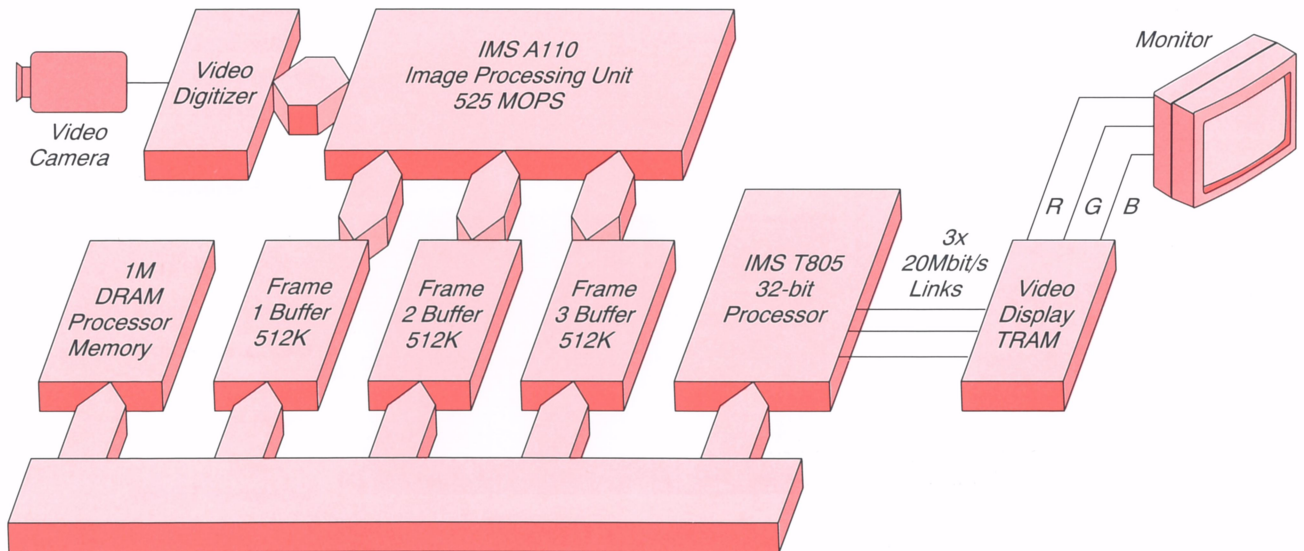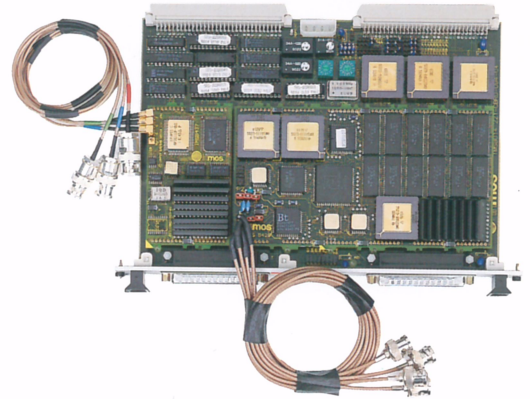

Image processing and display system

Toolset Software

Building a PC Based Development System

The benefits of the modular development system make it possible to customise the development environment. Below is an example of a basic single processor development system based around a PC.

Software
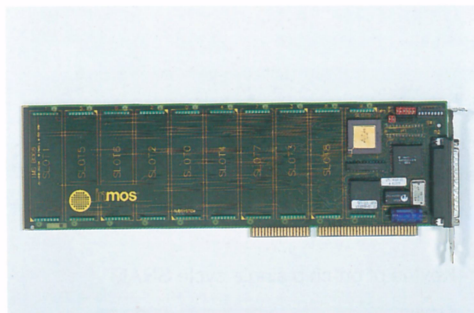
Choice of ANSI C, C++ or occam 2 Toolsets

Software programs are compiled on the host PC and then downloaded to the target hardware for debugging. The server allows the user to make use of host facilities such as PC filing, screen, keyboard and DOS system functions.

Hardware

The target hardware can be installed inside the PC using the IMS B008 PC motherboard. Alternatively the motherboard can be used as a gateway to an external system using a 20MBit/s transputer link for communication.

Transputers can be booted via the serial link, eliminating the need to program an EPROM for the target system.

PC Motherboard

A range of compute TRAMs are available with different speeds and sizes of memory. A 2Mbyte DRAM TRAM is recommended to start development. Further TRAMs can be added later as required.

PC Motherboard

- 10 slots
- 200Kbyte/s interface to host
- Software / hardware configurable
- External link interface for chaining additional motherboards or connection to customer's own hardware.
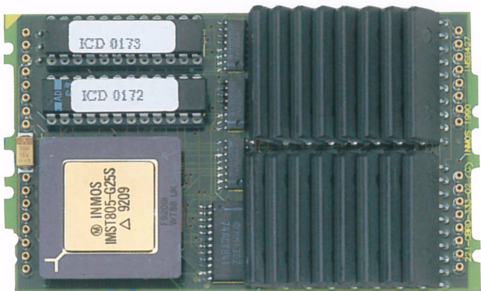
Compute TRAM

- Choice of transputer e.g. IMS T425 or IMS T805
- 2 Mbytes 4 cycle DRAM
- Size 2 module
- Subsystem port for local control of transputer network

2Mbyte TRAM

Building an Ethernet Based Development System

For groups of programmers working on a project INMOS recommends the use of networked development systems. Using an ethernet network, developers can share a transputer target system.

The key to this environment is the IMS B300 Ethernet to Transputer Gateway which uses a standard TCP/IP protocol connection to provide access for up to four separately controlled and bootable networks of transputers. Data transfer is transparent to the user, and socket libraries interface programs over the TCP/IP Ethernet.

Software running on the IMS B300 and host manages the control and allocation of the central transputer resource amongst the users.

Software

- Choice of C, C++, and occam 2.

- Software is compiled on the host and downloaded to the target via the Ethernet connection. Hosts can be PC or Sun compatible systems.

- Connection manager software allocates the requested target hardware configuration, automatically searching for available transputers.

Hardware

- IMS B300 Ethernet to Transputer Gateway
  - Standard IEE802.3 Ethernet interface to transputer links.

- IMS B250 VME Rack
  - Provides 12 slots for 6U VME boards such as IMS B014, IMS B016 VME master/slave board or other industry standard board.

- IMS B019 Differential System Port Board
  - Buffers 4 transputer links via RS422 compatible drivers connecting the IMS B250 and the IMS B300.

- IMS B014 VME Motherboard
  - 6U size board, takes up to 8 size 1 TRAMs.

- Compute TRAMs
  - Choice of transputer and memory sizes. Typical starter system may include four 8Mbyte DRAM modules with IMS T805 transputers.

- Cables
  - INMOS supplies a range of cables.
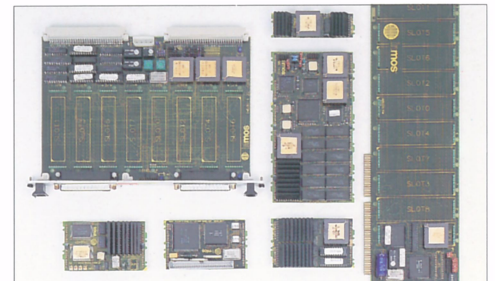

Software

Ethernet to Transputer Gateway

VME Rack

Range of TRAMs

Further product details are available in the Transputer Databook, *i*q systems Product Overview and the *i*q systems and Transputer Development Systems Databook. Contact your local sales office or distributor for further information.

inmos®

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