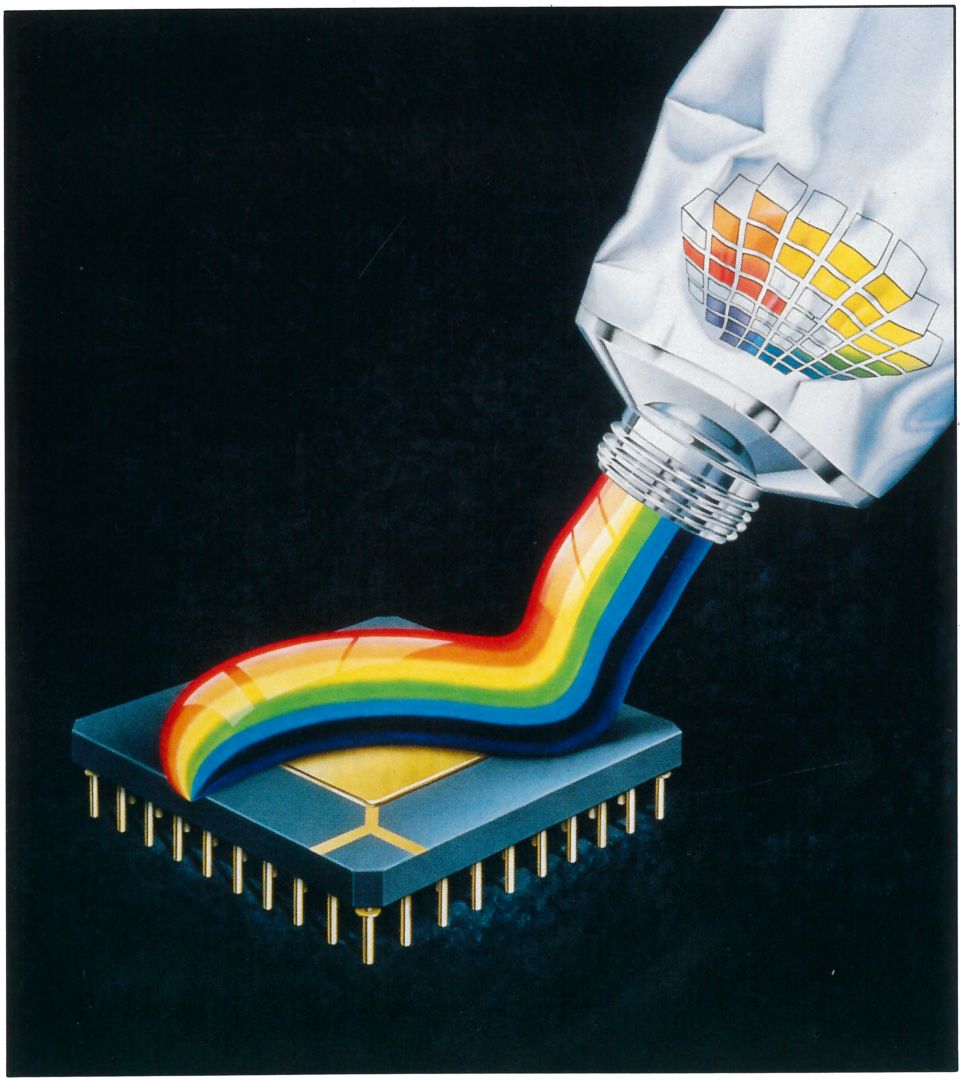
inmos®

Color Video Controllers



IMS G300
IMS G332
IMS G364

SGS-THOMSON MICROELECTRONICS

INMOS is a member of the SGS-THOMSON Microelectronics Group

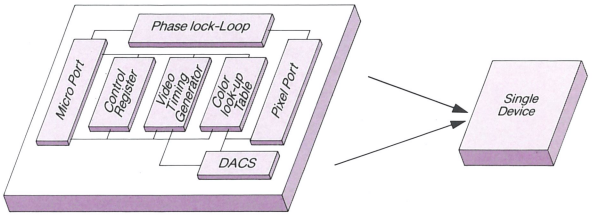
The INMOS Color Video Controllers

Following the success of INMOS Color Look-up Tables comes a new range of Color Video Controllers to support the ever-growing need for improved graphics systems.

The graphics market is demanding higher resolutions, faster drawing speeds, and upgradable drawing algorithms. This new range of CVCs is designed to meet these requirements and to maintain INMOS' position at the forefront of graphics technology.

The Philosophy

Functional integration, interface flexibility, application programmability . . . . all on the graphic designers wish-list, but never before available on a single chip. Until now. With the ability to interface to any microprocessor, and the programmable flexibility to switch in software for use with any monitor, the INMOS Color Video Controllers set new standards in medium and high resolution graphics control.



The Range

In 1989 INMOS launched the IMSG300 Color Video Controller to support screen resolutions as high as 1280 x 1024 pixels and variable pixel depths of color upto 24 bits. By building on this architecture INMOS has introduced two new powerful devices, the IMSG332 and IMSG364.

As well as having all the functionality of the IMSG300 as shown below, the new devices also include an on-chip 64 x 64 pixel color cursor and the ability to support interleaved serial port accessing. The G332 is so named because of its 32 bit multiplexed pixel port; likewise the G364 has one which is 64 bits wide making both devices ideal for supporting screens upto 1280 x 1024 pixels.

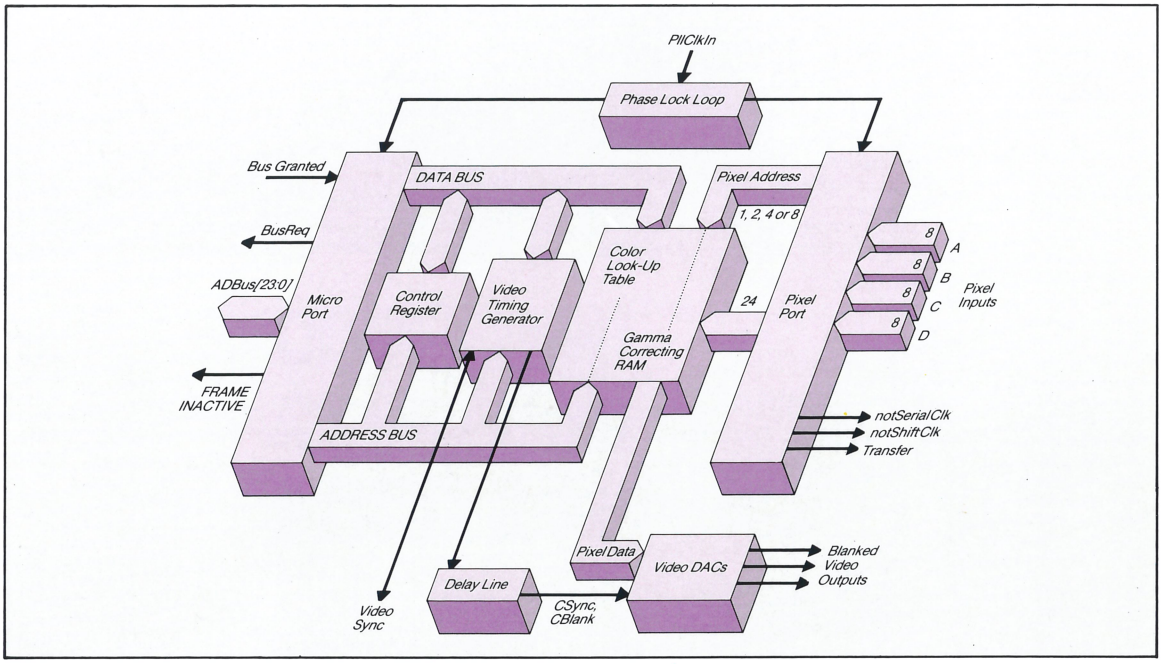
The INMOS range of CVCs support high resolution graphics in pseudo color (1, 2, 4, 8 bits/pixel), true color (15, 16 bits/pixel) and full color (24 bits/pixel), from VGA 640 x 480 to 1280 x 1024 pixel screen sizes.

The Architecture

IMS G300

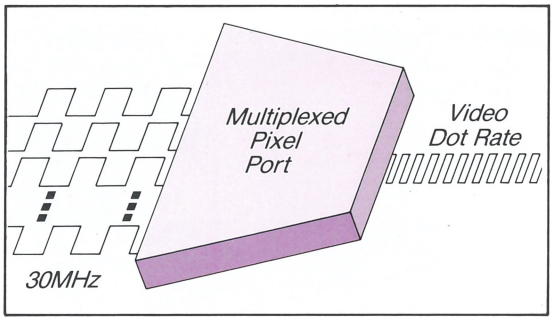
Features

- 66, 85, 100 and 110 MHz video rates.
- 1, 2, 4 and 8 bits/pixel in pseudo color.
- 24 bits/pixel in gamma corrected color.
- Four byte-wide multiplexed pixel inputs.



Multiplexed Pixel Ports

To achieve the very high video rates required by high resolution graphics the CVCs use 32 and 64 bit wide multiplexed pixel ports to interface to the bit map memory. Pixel multiplexing minimises the signal rate external to the CVC so keeping the frequency down to rates which can be driven comfortably by todays VRAMs and TTL drivers. The CVC internally serialises these pixels up to the full video rate.

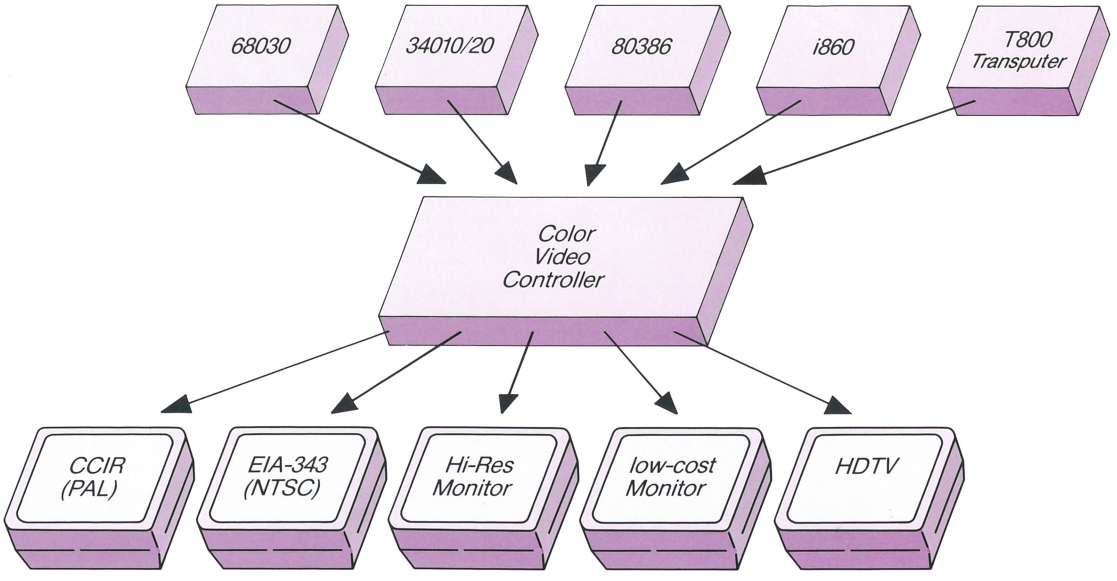


Video Timing Generator

The architecture of the CVCs is simple and straightforward; all register locations are memory mapped with no special cycles necessary to program them.

The video timing generator is a programmable finite state machine which is programmed by loading a number of timing parameters which describe both screen and bitmap format. Most of the parameters are completely independently variable giving enormous flexibility to the system. The resolution of the video timing generator is one quarter that of the individual pixels, hence scan lines are defined in multiples of four pixels.

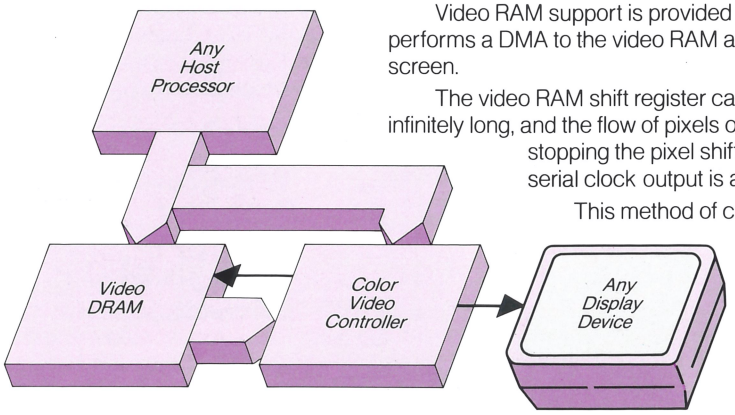
The video timing generator can handle both interlaced and non-interlaced screens in any aspect ratio over a frequency range of 100MHz. It can be configured to free run, providing composite or separate sync, or to lock onto an external synchronising source which may be another CVC, giving the potential for multiple, synchronous video systems. In either mode, it supplies composite blank to the video DACs, and it is capable of supplying them with tesselated or plain composite sync when in internal (master) mode. EIA 343 (NTSC) and CCIR (PAL) television standards are also supported.



Micro Port

The micro port is a bidirectional 24 bit interface which can be configured to operate in 24 bit wide word mode and 8 bit byte mode (G300 only). It consists of a multiplexed address and data bus with several control signals and is used for programming both the video timing generator screen description registers and the Color Look-up Table. To the programmer it appears simply as a block of memory occupying a small amount of address space.

Video RAM Support



Video RAM support is provided by a screen refresh mechanism which performs a DMA to the video RAM and allows seamless mid-line update of the screen.

The video RAM shift register can be made to behave as though it is infinitely long, and the flow of pixels onto the screen is controlled by starting and stopping the pixel shift clock at appropriate times. A continuous serial clock output is also provided for system synchronisation.

This method of control divorces the screen line length from dependence on the video RAM shift register length, allowing for very long display lines without extra multiplexing and for efficient use of memory irrespective of screen dimensions.

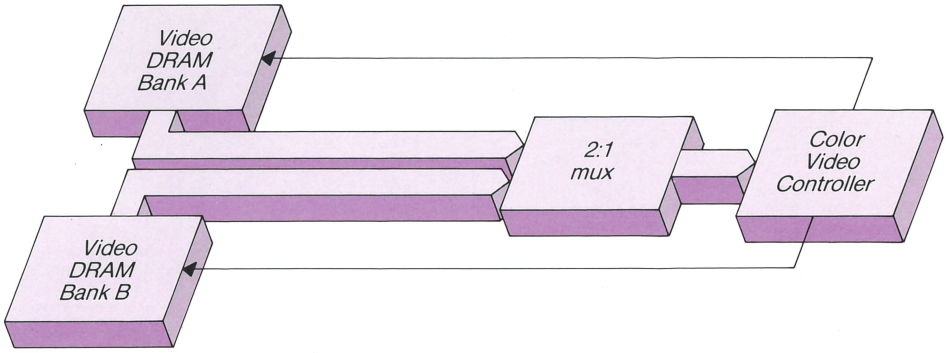
'Waltz'

– dancing teapots.

A 1K x 1K pixel screen showing ray traced images with anti-aliasing run on the IMS G300 and IMS T800.

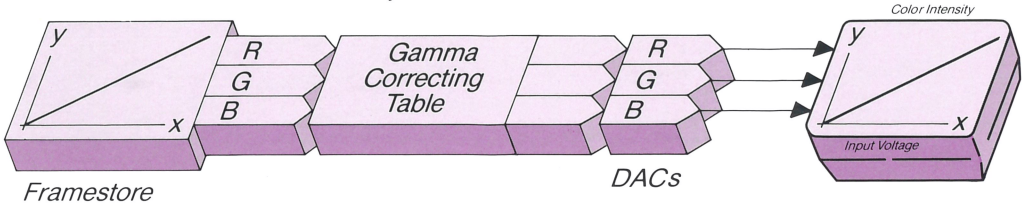
Interleaved Operation

The G332 and the G364 also have an interleaved mode which allows two banks of video DRAMs to be used, each running at half the frequency required when using one bank. The 32 bits of data are loaded alternately from each VRAM bank, enabling the devices to be run in true color and full color at high video frequencies.



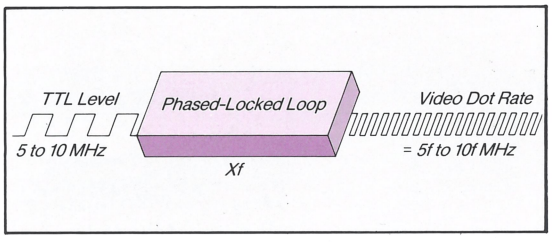
Color Look-up/Gamma Correcting Table

The Color Look-up Table (CLUT) is a 256 location by 24 bit RAM and it can be used in two ways. As well as being used as a CLUT for pixel addresses in pseudo color, the RAM can also be used as a mapping RAM for "gamma correction". This effect is caused by the non-linear properties of both the eye and the monitor phosphor. This feature of gamma correction is especially useful in color critical applications such as desktop publishing and studio graphics.



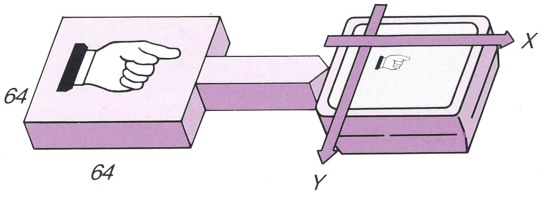
Phase-Locked Loop

All the CVCs integrate a phase-locked loop. This allows the part to be driven from a low speed clock in the 5–10 MHz range and to be internally multiplied by a user-specific factor to achieve the required high frequency video rates. The fact that there are no video rate digital signals on the board leads to easier and cheaper pcb design, as well as aiding in compliance with RFI emissions regulations; the programmability means any screen can be driven by a single crystal under the control of the applications software.

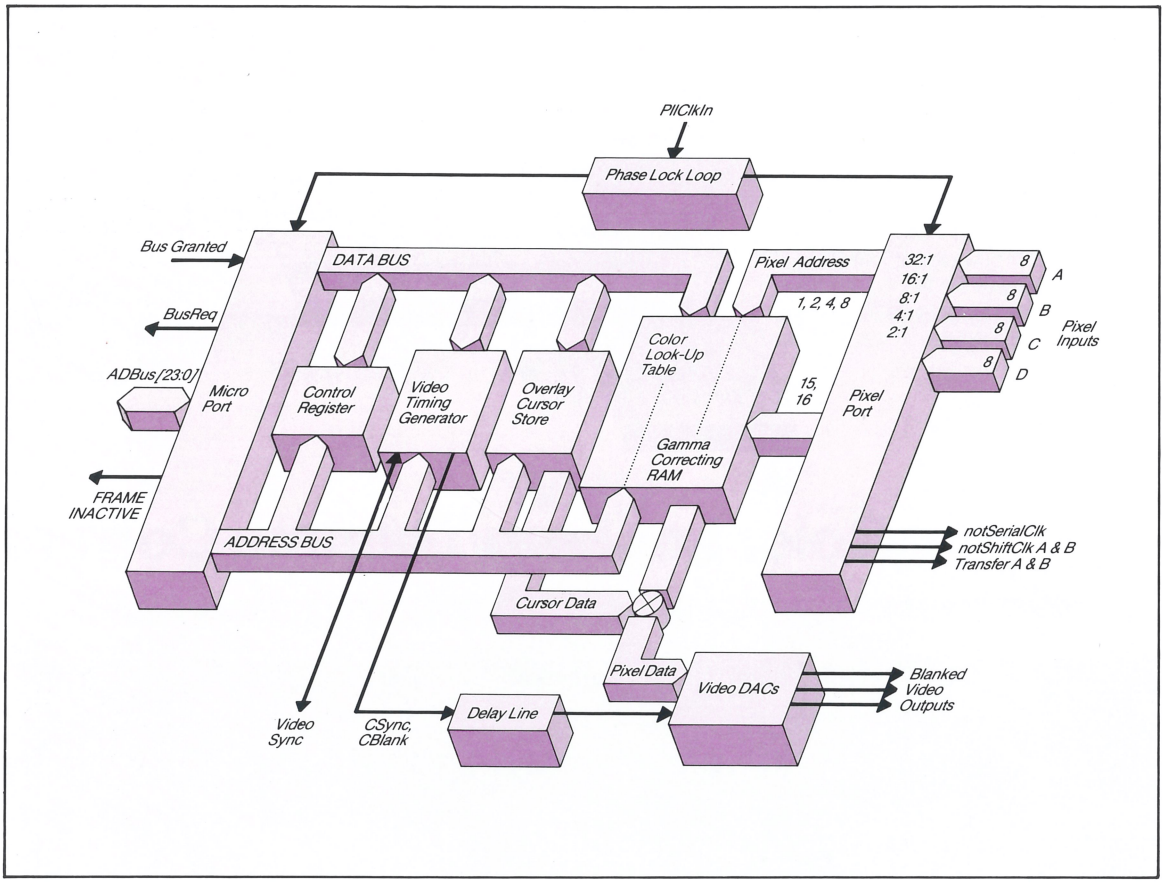


Cursor Store

The G332 and G364 both have an on-chip cursor store which consists of a 64 x 64 x 2 bit RAM. The cursor position is held in a single 24 bit register as an X-Y location relative to the top left of the screen (making it independent of monitor choice). The position defined is that of the topmost, leftmost pixel of the cursor. The 2 bit cursor pixels address a 3 location by 24 bit CLUT, i.e. 3 colors 24 bits deep and one transparent allowing any shape cursor to be used.



IMS G332

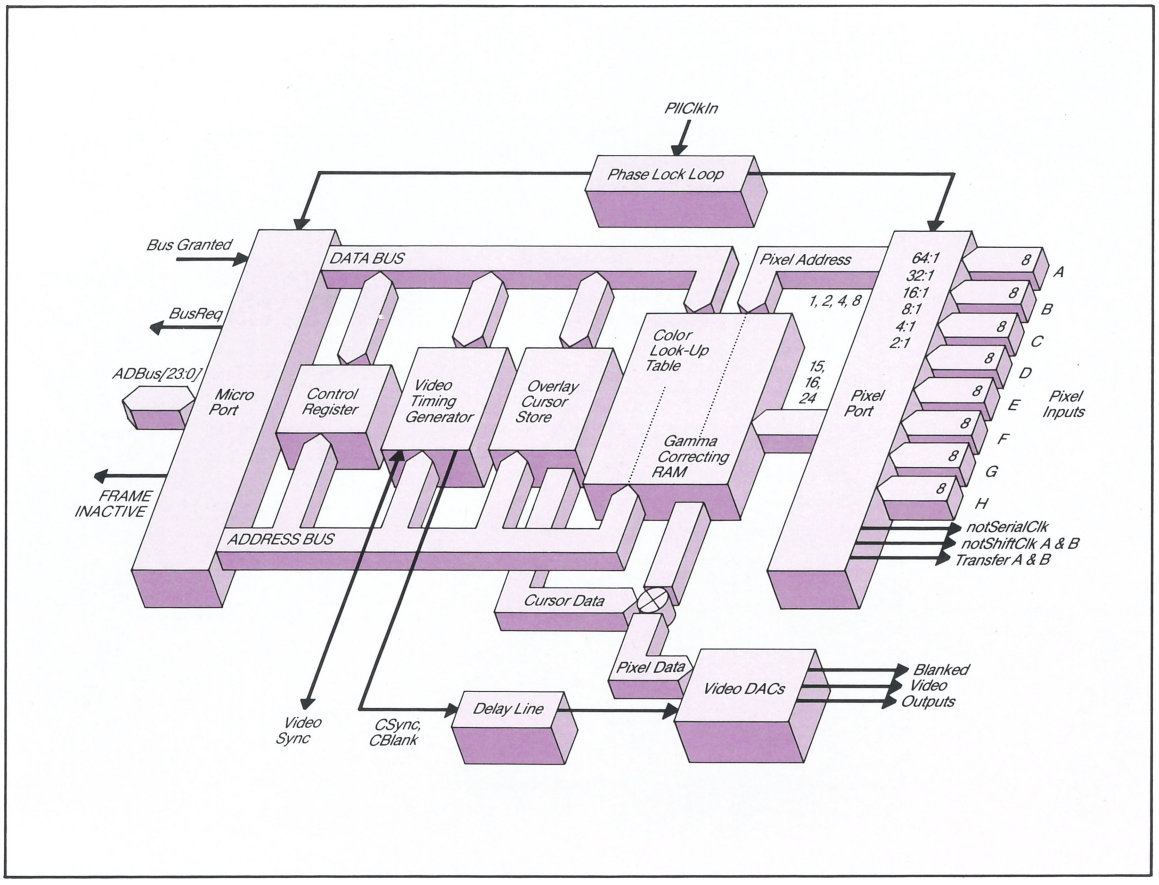


Features

- 85, 100, 110, 135* MHz video rates.
- 1, 2, 4 and 8 bits/pixel in pseudo color.
- 15 and 16 bits/pixel in gamma corrected color.
- 32 bit multiplexed pixel port.
- Interleaved and non-interleaved operation.
- 64 x 64 x 3 color cursor.

** Available 1991*

IMS G364



Features

- 85, 100, 110, 135* MHz video rates.
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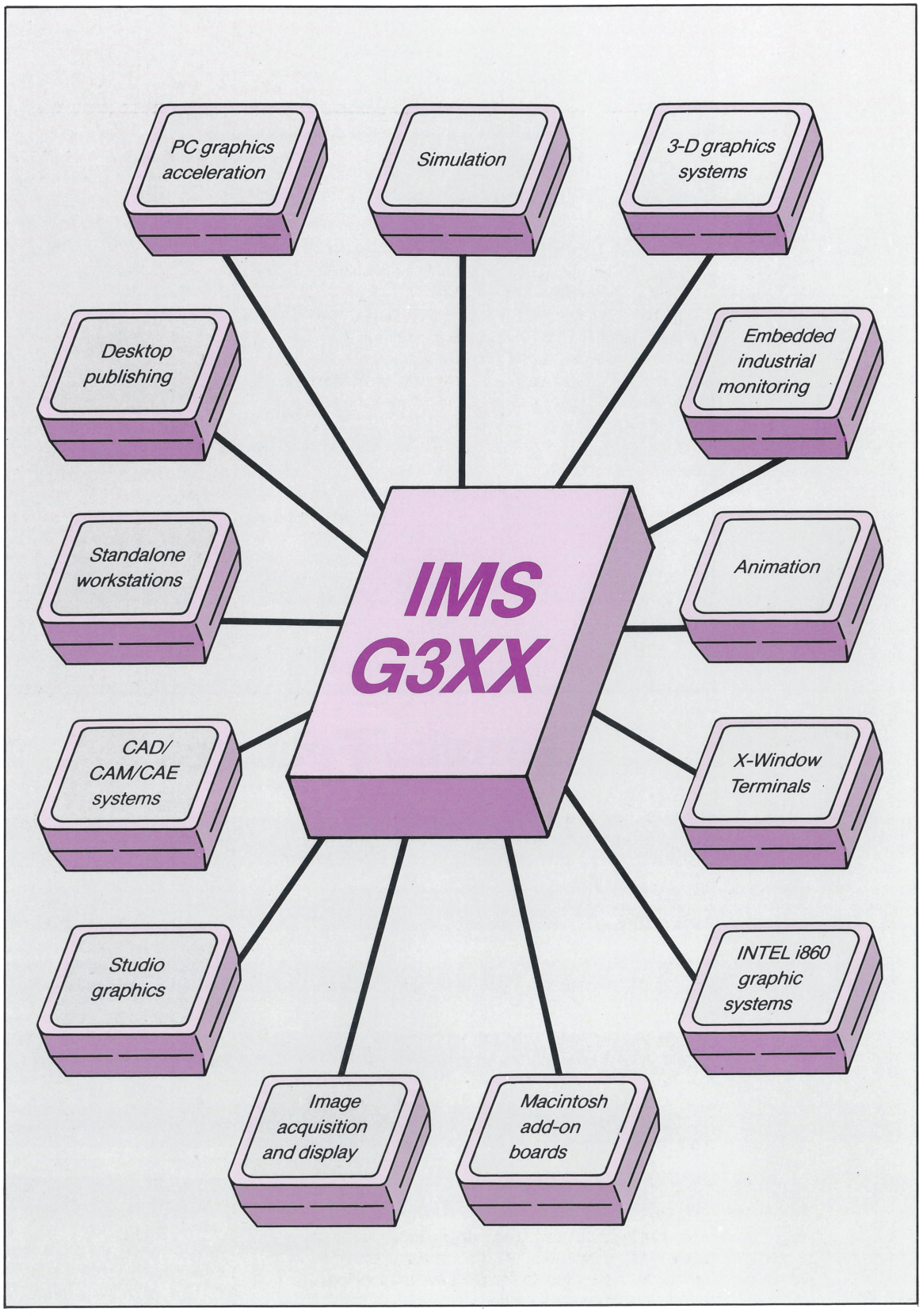
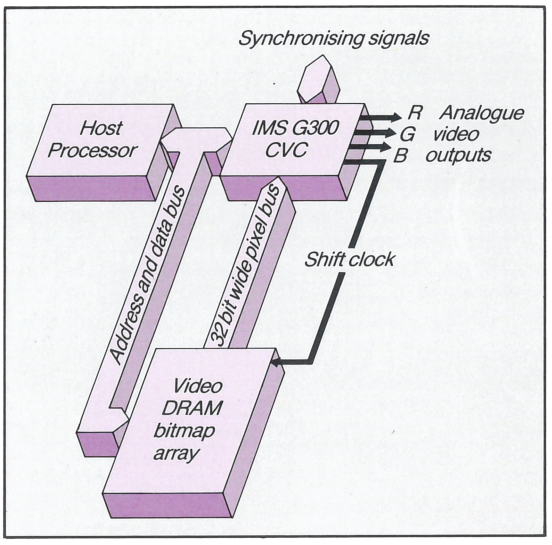
- 15,16 and 24 bits/pixel in gamma corrected color.
- 64 bit multiplexed pixel port.
- Interleaved and non-interleaved operation.
- 64 x 64 x 3 color cursor.

** Available 1991*

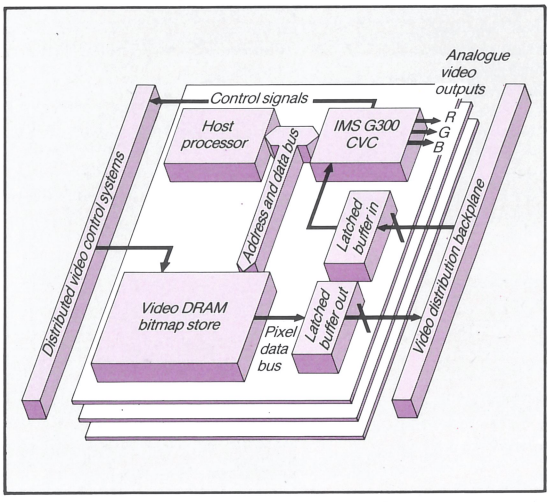
CVC Application Areas





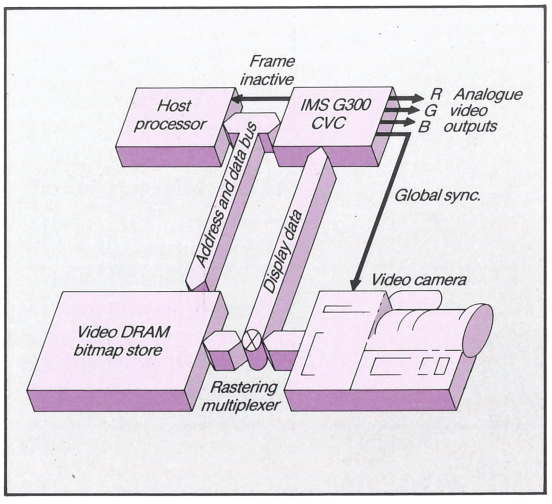
The CVCs reduce overall system costs by virtue of their high level of integration whilst at the same time allowing considerably enhanced functionality.

A basic graphics system using a CVC has a very low chip count, typically less than five packages in addition to the processor and the RAM arrays. The effect of this is to reduce the complexity of the graphics subsystem to the level where it no longer dominates the entire system.



Applications such as standalone workstations, simulation and animation need the ability to farm out complex drawing tasks and to merge multiple pages of screen data in order to meet the heavy demands on both drawing and bitmap bandwidth made by such systems.

The CVC can be configured as either master or slave by the application software so that multiple, synchronous arrays of CVCs can be constructed. Since all video data is kept down to TTL compatible rates, graphics data distribution can become just another back plane operation and expanding graphics power is simply a matter of plugging in another standard graphics card.

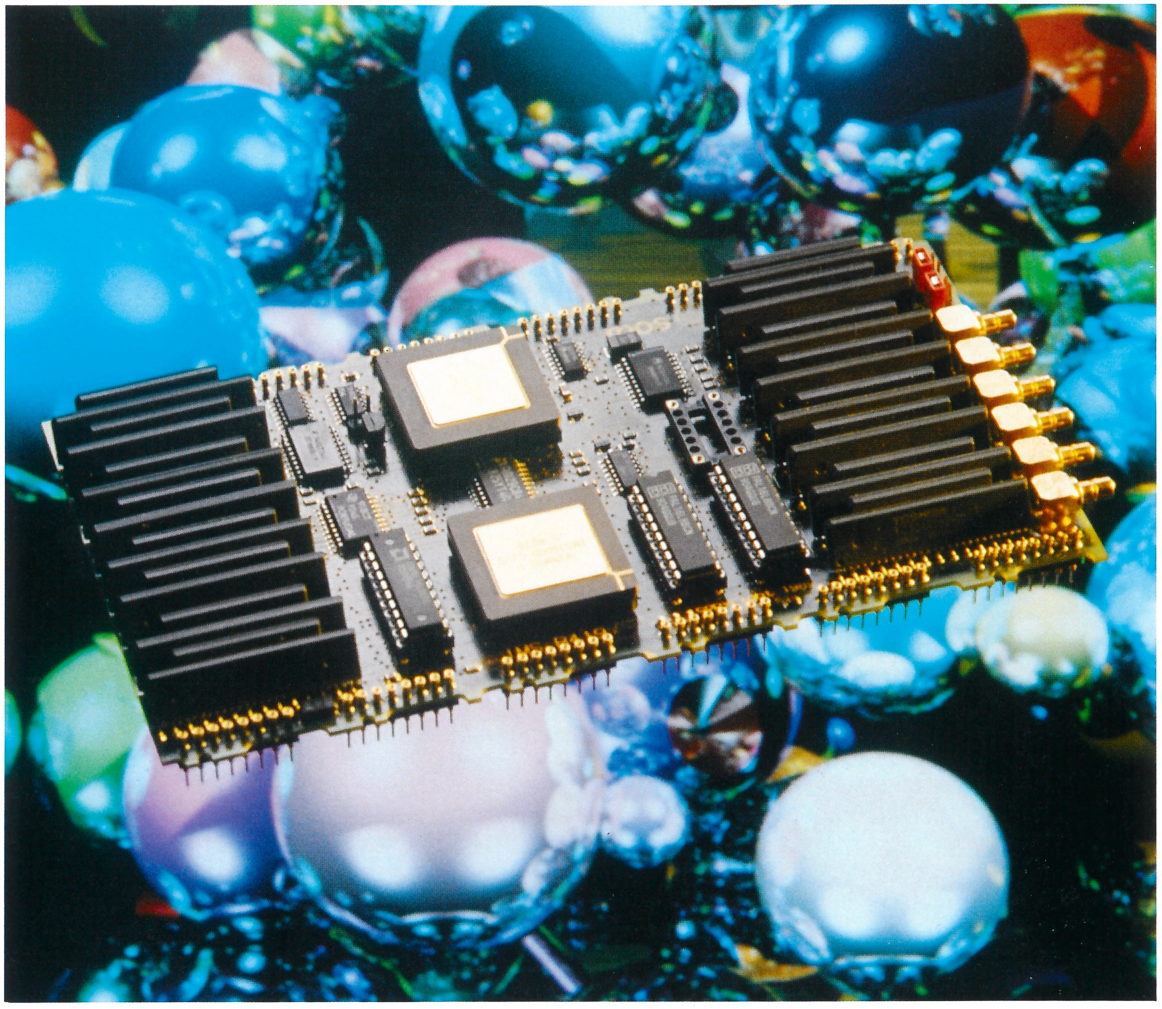


To support TV studio graphics the video timing generator on the CVCs can be programmed to produce EIA 343 or CCIR standard synchronising waveforms for interlaced systems. This makes it ideal for studio work both as an image grabber and for conversion between studio and computer standards.

The option of using a 24 bit color range is most useful in this environment.

The CVC will output either composite video (with or without flyback tesselations) or separate video and digital sync. It can be switched in software from being the master in a system to being a slave responding to a global synchronising scheme.

IMS G300 Graphics Module – IMS B419



Features

- IMS T800-20 transputer
- IMS G300 Color Video Controller
- 2 Mbytes of four cycle DRAM
- 2 Mbytes of four cycle VRAM
- Pixel rates 70 to 110 MHz at 8 bits/pixel
- Communicates via 4 INMOS serial links (selectable between 10 or 20 Mbits)
- Conforms to published transputer module (TRAM) specification and forms part of the INMOS *iq* systems range
- Size 6 TRAM

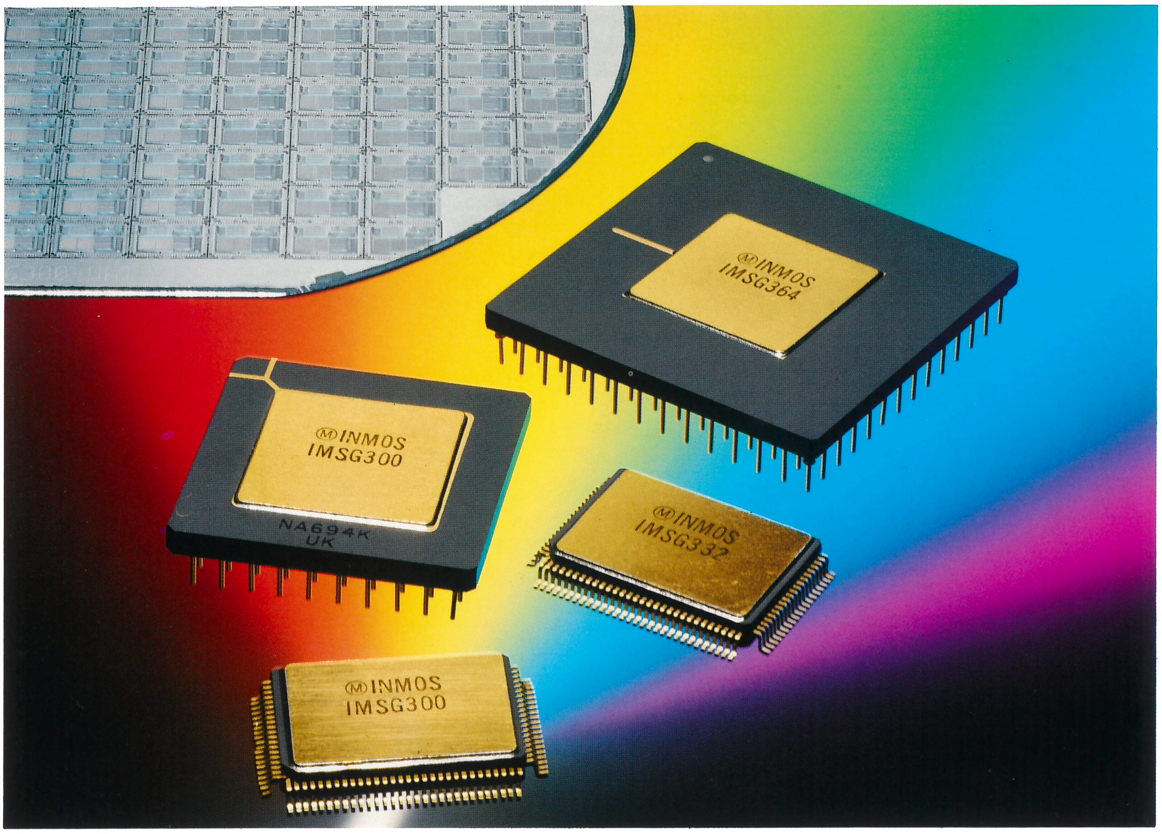
Whilst the Color Video Controller range is compatible with any microprocessor, INMOS has used its own transputer on a board to enable potential users to evaluate the IMS G300.

The IMS B419 incorporates the IMS G300 Color Video Controller with the IMS T800 32 bit floating point transputer to form a high performance graphics system. 2 Mbytes of four cycle DRAM provide a general purpose store sufficient to run applications such as an X window system, and allow INMOS development tools to be resident on board. 2 Mbytes of Video RAM provide arbitrary screen resolutions up to a maximum of 1280 x 1024 8 bits/pixel with unrestricted screen formats at resolutions below this.

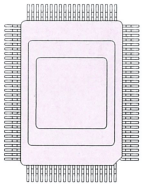
The board is supplied with software graphics libraries conforming to the CGI (Computer Graphics Interface) standard.

The B419 can plug into a variety of motherboards (PC, VME bus, Double Eurocard).

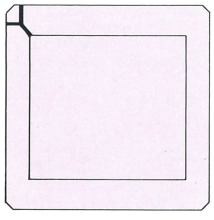
Ordering and Package Information



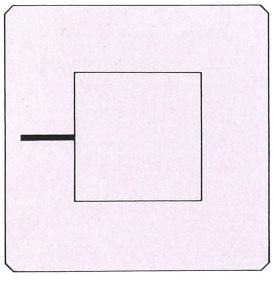
Actual size.



100 Pin CQFP



84 PGA



132 PGA

PART	PACKAGE	SPEED
IMSG300G-66S	84 Pin Grid Array	66 MHz
IMSG300G-85S	84 Pin Grid Array	85 MHz
IMSG300G-10S	84 Pin Grid Array	100 MHz
IMSG300G-11S	84 Pin Grid Array	110 MHz
IMSG300F-66S	100 Pin Ceramic Quad Flatpack	66 MHz
IMSG300F-85S	100 Pin Ceramic Quad Flatpack	85 MHz
IMSG300F-10S	100 Pin Ceramic Quad Flatpack	100 MHz
IMSG300F-11S	100 Pin Ceramic Quad Flatpack	110 MHz
IMSG332F-85S	100 Pin Ceramic Quad Flatpack	85 MHz
IMSG332F-10S	100 Pin Ceramic Quad Flatpack	100 MHz
IMSG332F-11S	100 Pin Ceramic Quad Flatpack	110 MHz
IMSG332F135S	100 Pin Ceramic Quad Flatpack	135 MHz*
IMSG364G-85S	132 Pin Grid Array	85 MHz
IMSG364G-10S	132 Pin Grid Array	100 MHz
IMSG364G-11S	132 Pin Grid Array	110 MHz
IMSG364G135S	132 Pin Grid Array	135 MHz*

** Higher speeds between 110 and 135 MHz will be introduced in 1991.*

N.B. PQFP packages for the G332 and G364 are under development.

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