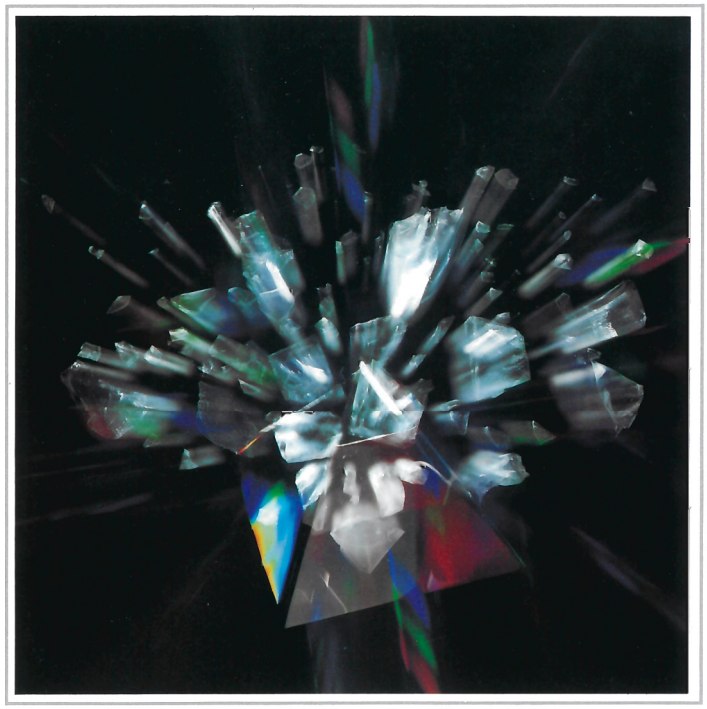
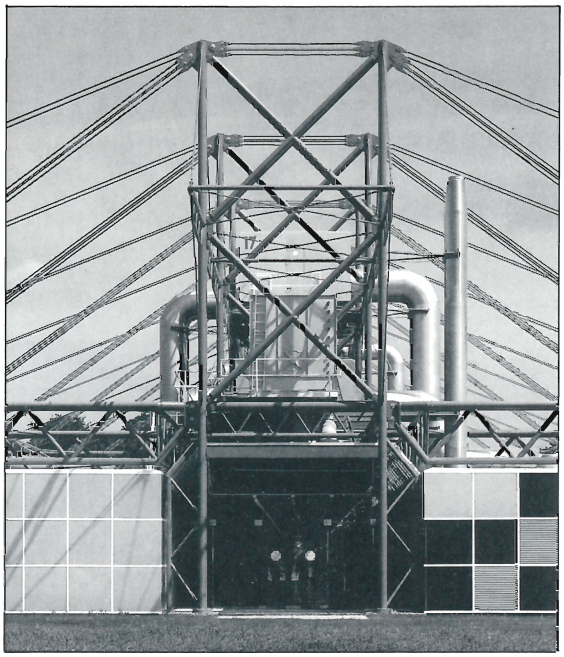
inmos®



SPECTRUM

Bristol



Newport

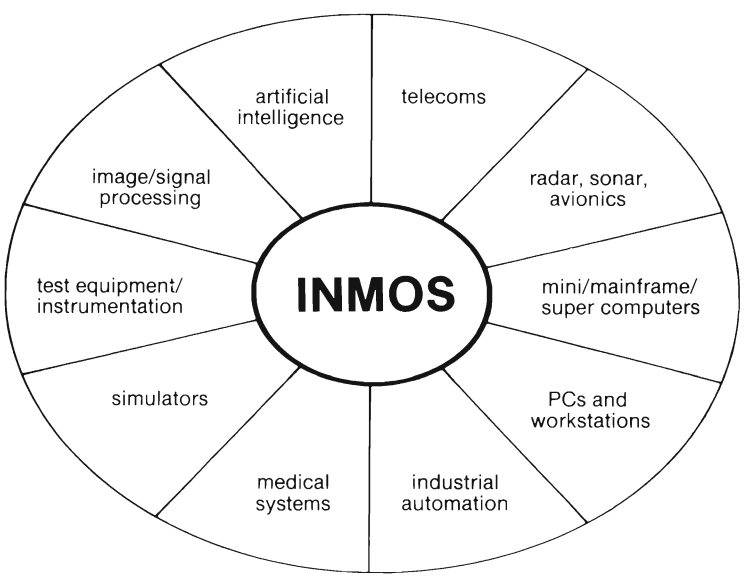
INMOS

INMOS designs, manufactures and sells high performance VLSI semi-conductors as a worldwide operation. Since inception in 1978, INMOS has brought to the market place a wide range of components and systems offering unique facilities not available in competitive products. The current product line includes revolutionary microprocessors called transputers, colour graphics devices, digital signal processors and very fast Static RAMs. These are all currently supplied to companies in North America, Japan, the Far East and Europe.

Corporate headquarters are based in Bristol, England, along with sales and marketing and the design centre. INMOS' wafer fabrication facility is in Newport, South Wales, UK, with final test facilities located both at Newport and Colorado Springs, Colorado, USA. The sales and marketing group has offices throughout the USA, in Bristol, Munich and Paris for Europe and in Tokyo for the Far East; each with an applications support team. This is further supported by a network of distributors covering all countries actively using VLSI semiconductors.

The INMOS Market Place

INMOS is successfully selling its products for use in a wide variety of equipment, from simple desk top microcomputers to sophisticated telecommunications systems, and into the world's supercomputers. INMOS products are applicable in all areas of computing, control and display as outlined in the table below.



The Product Range

The most important additions to this issue are the new TRAnsputer Modules (TRAMs) with their associated Motherboards and the extensions to the range of Development Tools. Both of these greatly extend the ease of application and the flexibility of use for the INMOS transputer products.

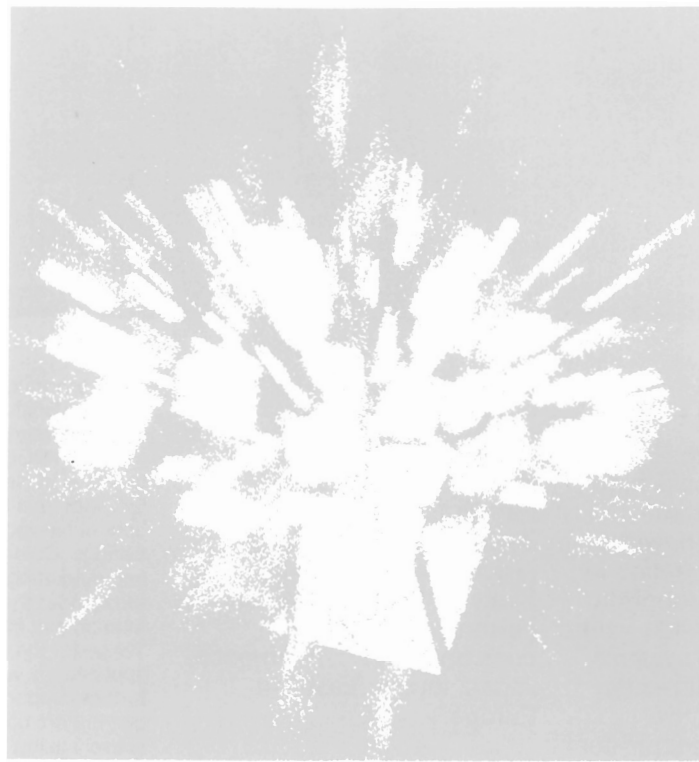
All products utilise the INMOS propriety CMOS technology, the latest designs using the 1.0 micron geometry version. This process technology coupled with the final test facilities have enabled INMOS to give a full commitment to MIL. STD. availability across it's range of silicon products.

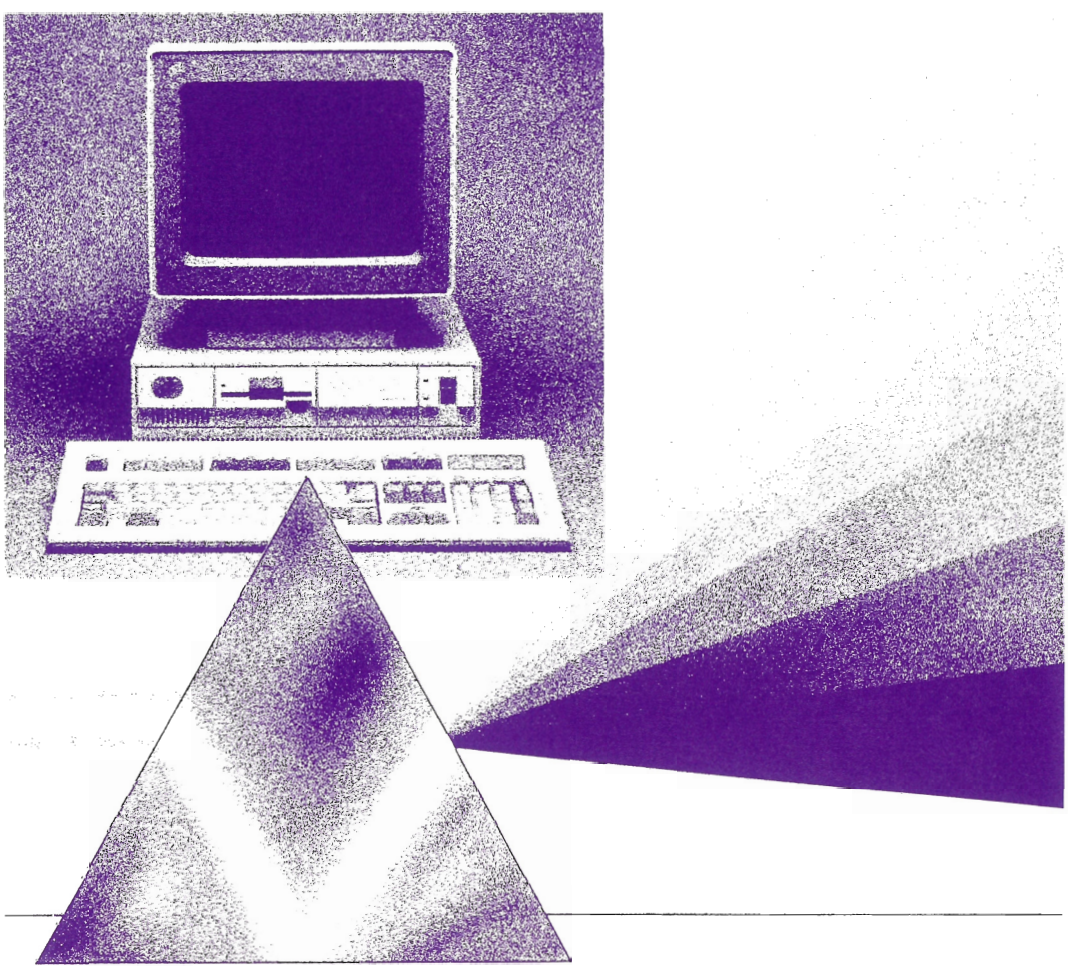
Colour Lookup Tables
The Industry Standard, 25 to 65MHz

Digital Signal Processor
Cascadable, 16Bit, 32 stage, up to 10MHz throughput, evaluation and user systems

Transputer Family
16 and 32 microprocessors, modules, boards and development systems

Fast Static RAMs
CMOS, 4K to 64K, X1/X4/X8, 20 to 70ns





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COLOUR CONTROL

inmos

COLOUR CONTROL

FEATURES

- Compatible with RS170 video standard
- 256 K possible colours
- RGB analogue output with composite blank and sync
- 6 Bit DACs
- Low DAC glitch energy
- Video signal output into 75 Ω
- Pixel word mask
- TTL compatible inputs
- Microprocessor compatible write interface
- Single monolithic high performance CMOS
- Single + 5V ± 10% power supply
- 28-pin, 600-mil DIP
- Low power dissipation

DESCRIPTION

The IMS G170 and the IMS G175 integrate the functions of colour look-up table (or colour palette), digital to analogue converters and microprocessor interface into a single 28 pin package.

Both devices are capable of displaying any 256 colours from a palette of 256 K possible colours. The IMS G170 and IMS G175 replace TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than modifying the look-up table.

The asynchronous operation of the microprocessor interface allows the controlling microprocessor to configure and update the contents of the look-up table without reference to the high speed timing of the video system, thus simplifying the design.

The analogue outputs can directly drive a 75 Ω load. Composite sync and blanking are supported.

IMS G170

High Performance 6 BIT DAC 8 BIT Pixel Colour Look-up Table

FEATURES

- 35, 50 MHz pixel rates
- Ceramic DIP

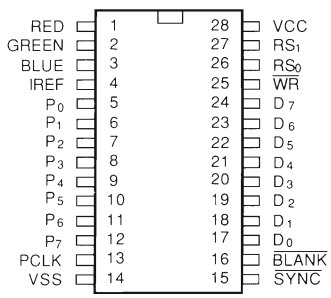
IMS G175

Low Cost 6 BIT DAC 8 BIT Pixel Colour Look-up Table

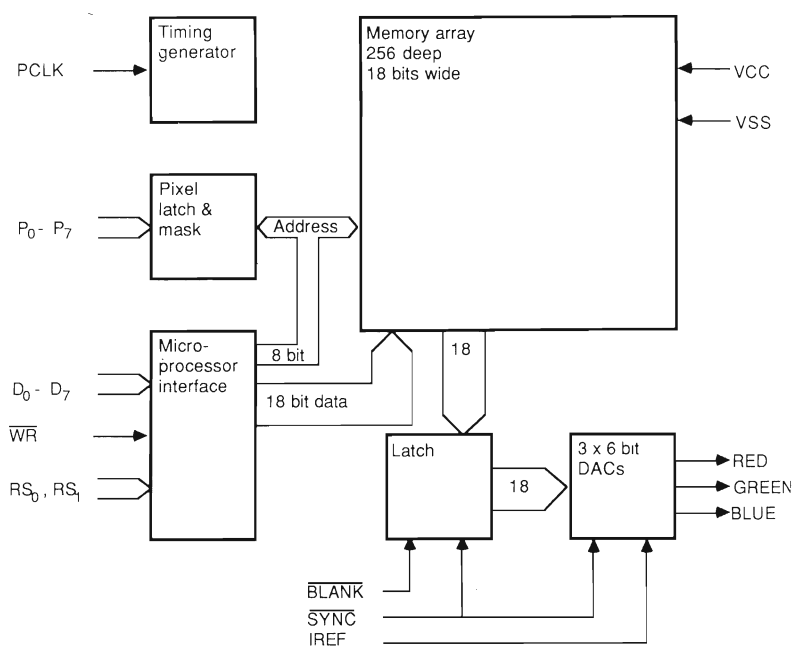
FEATURES

- 25 MHz pixel rates
- Low cost plastic DIP

PIN CONFIGURATION



PIN NAMES	
P_0 - P_7	Pixel address inputs
D_0 - D_7	Program data inputs
RS_0, RS_1	Register select
RED, GREEN, BLUE	Analogue video outputs
PCLK	Pixel clock
$\overline{WR}$	Write enable
$\overline{BLANK}$	Video blanking input
$\overline{SYNC}$	Video sync input
IREF	Reference current
VCC	+5 volt supply input
VSS	Ground



FEATURES

- Compatible with RS170 video standard
- 256 K possible colours
- Read back of look-up table and register contents
- RGB analogue output with composite blank
- 6 Bit DACs
- Low DAC glitch energy
- Output into doubly terminated 75 Ω load
- Pixel word mask
- TTL compatible inputs
- Microprocessor compatible interface
- Single monolithic high performance CMOS
- Single + 5V ± 10% power supply
- Low power dissipation
- 28-pin, 600-mil DIP

DESCRIPTION

The IMS G171 and the IMS G176 integrate the functions of colour look-up table (or colour palette), digital analogue converters and microprocessor interface into a single package.

The IMS G171/6 can display 256 different colours from a palette of 256 K. They replace TTL/ECL systems, giving reduced component cost, board area and power consumption.

The pixel word mask allows displayed colours to be changed in a single write cycle rather than modifying the look-up table.

The asynchronous operation of the microprocessor interface allows the controlling microprocessor to configure, update and examine the contents of the look-up table and the various control registers without reference to the high speed timing of the video system, thus simplifying the design.

The analogue outputs can directly drive a 75 Ω load. Composite blanking is supported.

IMS G171

High Performance 6 BIT DAC 8 BIT Pixel Colour Look-up Table

FEATURES

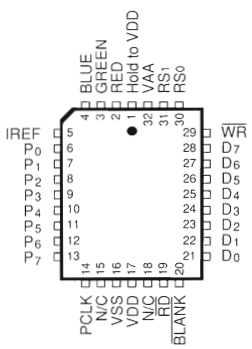
- 35, 50 MHz pixel rates
- Ceramic or plastic DIP
- Used in all IBM PS/2 models

IMS G176

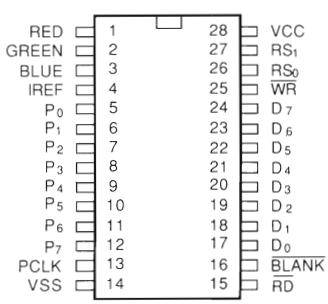
High Performance 6 BIT DAC 8 BIT Pixel Colour Look-up Table

FEATURES

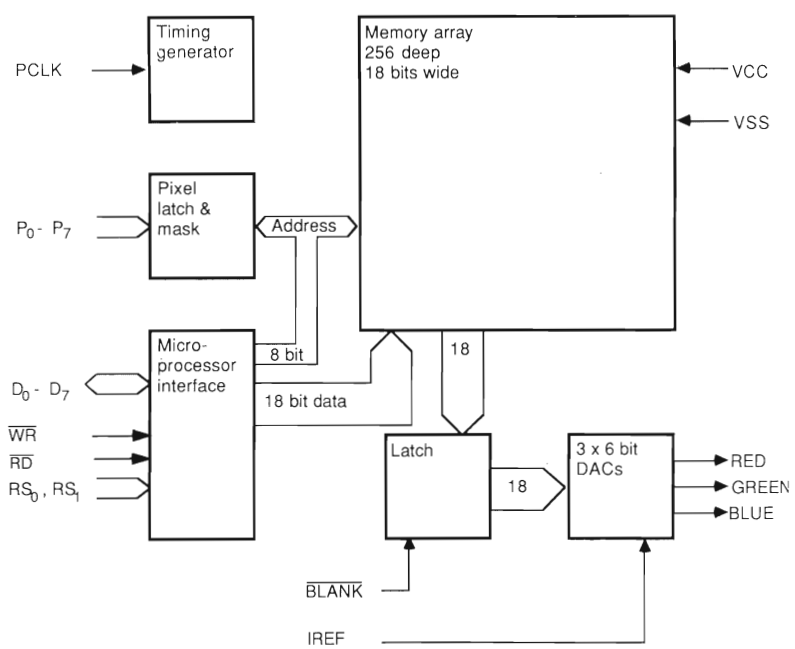
- 40, 50, 65 MHz pixel rates
- Asynchronous access to pixel mask register
- Hardware and software compatible with IMS G171
- Available in 28-pin ceramic or plastic DIP and 32-pin PLCC



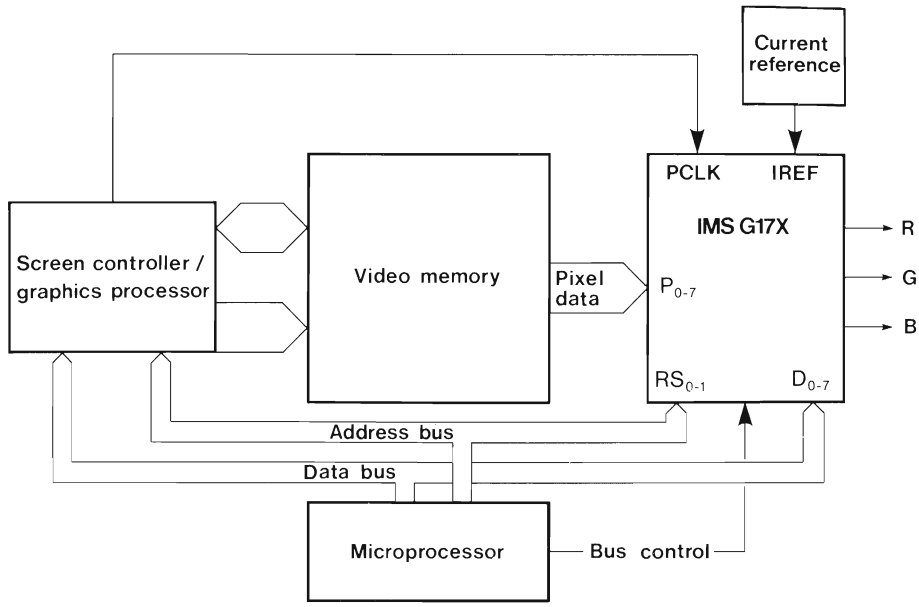
PIN CONFIGURATION



PIN NAMES	
P_0–P_7	Pixel address inputs
D_0–D_7	Program data
RS_0, RS_1	Register select
RED, GREEN, BLUE	Analogue video outputs
PCLK	Pixel clock
$\overline{WR}$	Write enable
$\overline{RD}$	Read enable
$\overline{BLANK}$	Video blanking input
IREF	Reference current
VCC	+5 volt supply input
VAA	Analogue supply
VDD	Digital supply
VSS	Ground



COLOUR CONTROL

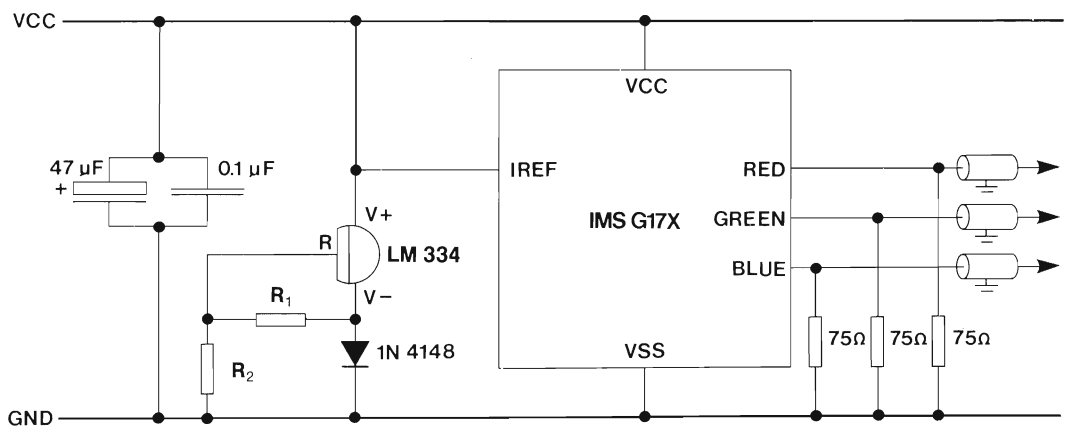


The IMS G17X family of colour look-up tables provide the analogue output stage for colour graphic systems. They contain a high speed random access store or look-up table, three DACs, a pixel word mask and a microprocessor interface.

A pixel word, up to 8 bits wide, is read in on the Pixel Address inputs. The pixel word is used as a read address into the look-up table memory. The resultant data word is applied to the inputs of the three DACs. The IMS G17X family thus map an 8 bit digital value to an analogue signal that will produce one of a wide range of possible colours on a monitor. All members of the IMS G17X family give a palette of 256 colours from a total range of 256K colours.

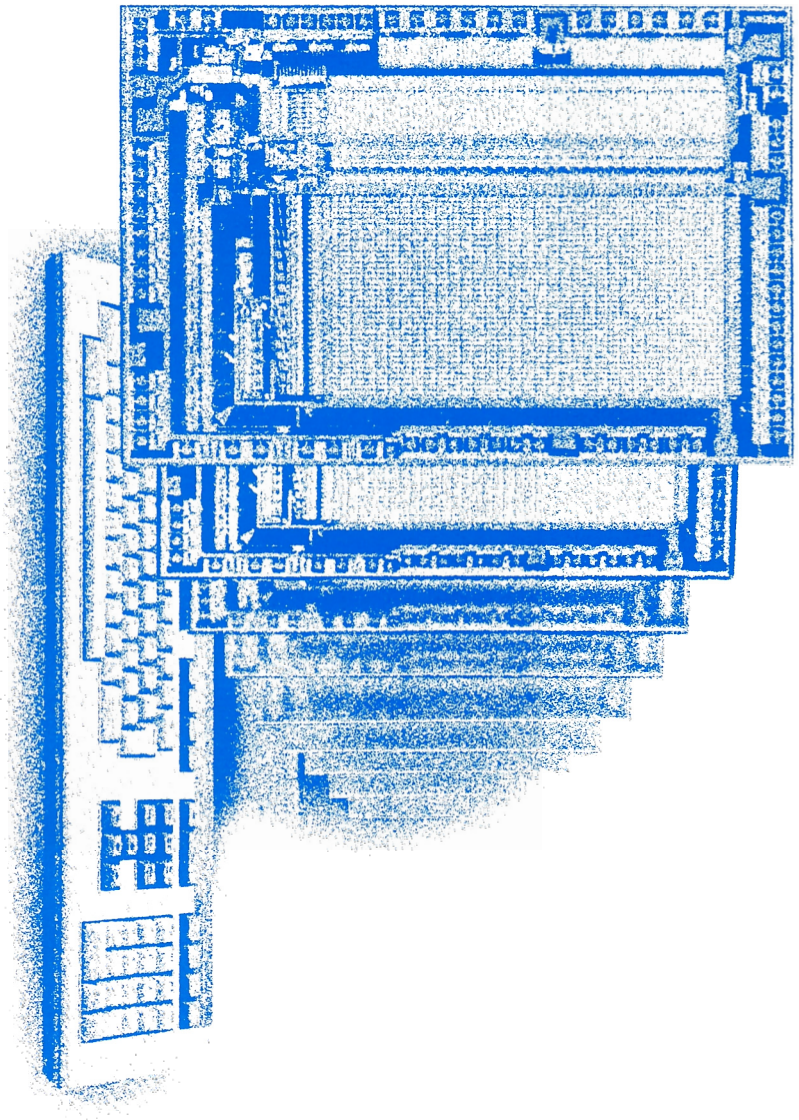
The look-up table and the Pixel Mask register can be accessed through an 8 bit wide microprocessor interface. The use of an internal synchronising circuit allows operations on the interface to be totally asynchronous to the video path. This asynchronous interface greatly simplifies graphic system design.

A pixel word mask is included to allow the incoming pixel address to be masked. This permits rapid changes of the effective contents of the look-up table to facilitate such operations as animation, overlays and flashing objects.



	R_1	R_2
IMS G170/5	30	300
IMS G171/6	15	150

The DACs are comprised of a number of summed current sources. The number of active current sources being determined by the digital value applied to the DAC. The current drawn from the IREF pin is a reference current setting the output current of each of the current sources. A voltage is produced by placing a load resistor between the DAC outputs and ground. This load resistor also provides the terminating impedance for the connection between the DAC outputs and the monitor.



SIGNAL PROCESSOR

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SIGNAL PROCESSOR

IMS A100

Cascadable Signal Processor

FEATURES

- Full 16 bit, 32 stage, transversal filter
- 320 Million Operations Per Second (MOPS) capability
- Fully cascadable with no speed degradation or reduction in dynamic range
- Data throughout to 10 MHz
- Coefficients selectable as 4, 8, 12 or 16 bits wide
- High speed microprocessor compatible interface
- Data input and output through dedicated ports or via the microprocessor interface
- Fully static high speed CMOS implementation
- TTL compatible
- Single +5V±10% power supply
- Power dissipation <1.5 Watts
- Standard 84-pin ceramic PGA
- MIL.STD. processing available

The IMS A100 is a high speed, high accuracy 32 stage digital transversal filter. Its flexible architecture allows it to be used as a "building block" in a wide range of Digital Signal Processing applications. The part is capable of performing high speed DFTs, convolution and correlation, as well as many filtering functions.

The input data word length is 16 bits, and coefficients are programmable to 4, 8, 12 or 16 bits wide. No truncation or rounding occurs within the multiply accumulation array. Two's complement numerical formats are used for both data and coefficients.

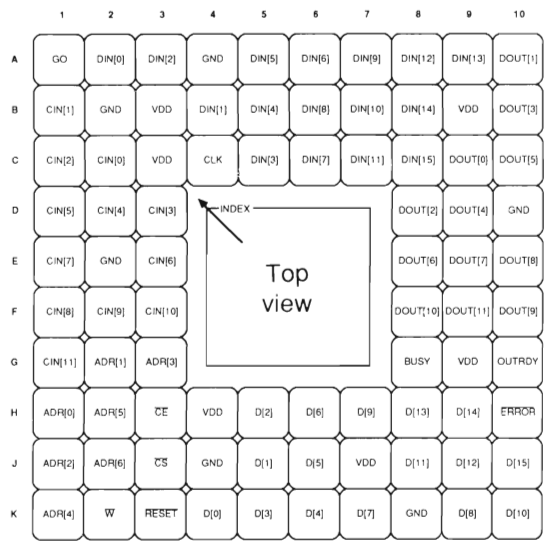
The coefficients can be updated asynchronously to the system clock during normal operation, allowing the chip to be used in a variety of adaptive systems.

The IMS A100 can be cascaded to construct longer transversal filters with no additional logic or degradation in speed, whilst preserving a high degree of accuracy.

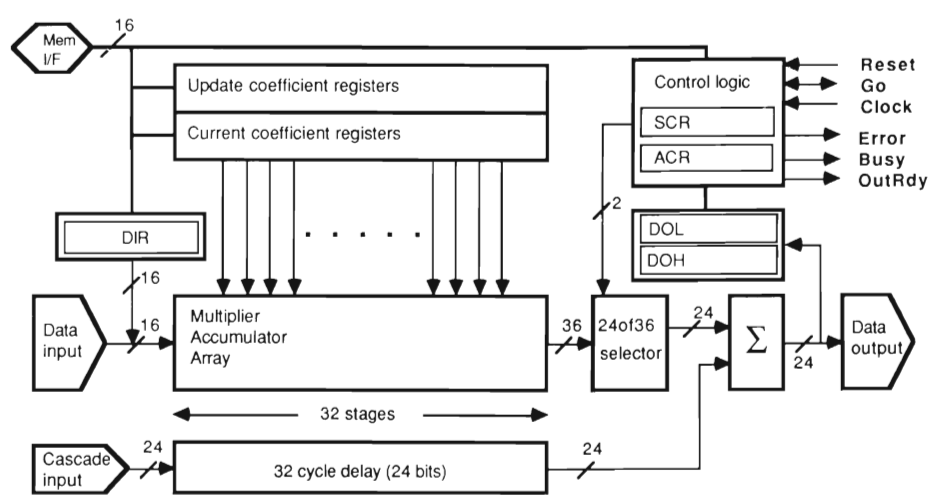
Multiple IMS A100s can also be used where greater dynamic range is required for data or coefficients, or where higher data rates are required.

APPLICATIONS

- Digital FIR filtering
- High speed adaptive filtering
- Correlation and Convolution
- Discrete Fourier Transform
- Speech processing using Linear Predictive Coding
- Image processing
- Waveform synthesis
- Adaptive and fixed equalizers and echo cancellers
- Spread spectrum communication
- Beamforming and beamscanning in sonar and radar
- Pulse compression
- High speed fixed point matrix multiplication



PIN	NAMES
$\overline{CS}$	Memory interface select
$\overline{CE}$	Memory interface enable
$\overline{W}$	Memory interface write enable
ADR[0-6]	Memory interface address
D[0-15]	Memory interface data
$\overline{RESET}$	Reset
$\overline{ERROR}$	Numerical overflow
BUSY	Bank swap in progress
CLK	Clock
GO	Initiate cycle
DIN[0-15]	Data input
DOUT[0-12]	Data output (multiplexed)
OUTRDY	Output data ready
CIN[0-11]	Cascade data input



DESCRIPTION

The IMS A100 is a 32 stage, cascadable, digital transversal filter. The general canonical transversal filter is shown in Figure 1. An alternative, and functionally equivalent filter is shown in Figure 2. In this realisation, used in the IMS A100, the input signal is supplied in parallel to all 32 multipliers, and the delay and summation are performed in a distributed manner.

Each data sample loaded into the IMS A100 is fed in parallel to all 32 stages. At each stage the current input sample is multiplied by a coefficient stored in memory, and added to the output of the previous stage delayed by one clock cycle. The filter output at time $t = kT$ is given by:

$$y(kT) = C(0)x(kT) + C(1)x((k-1)T) + \ldots$$
$$\ldots + C(N-1)x((k-N+1)T)$$

where $x(kT)$ represents the kth input data sample, and $C(0)$ to $C(N-1)$ are the coefficients for the N stages. While the IMS A100 architecture is designed as a transversal filter it contains many features which allow it to be used in a wide range of signal processing applications eg. adaptive filtering, matrix multiplication, discrete Fourier transforms, correlation and convolution.

Figure 1 - Canonical transversal filter architecture

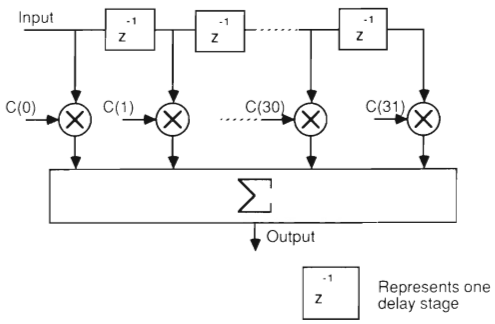
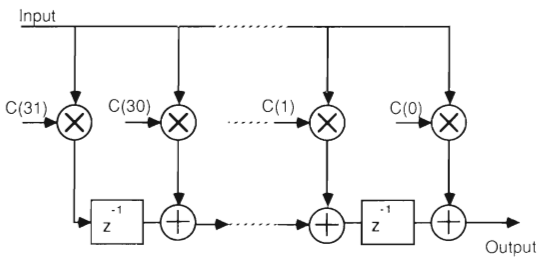


Figure 2 - Modified transversal filter architecture

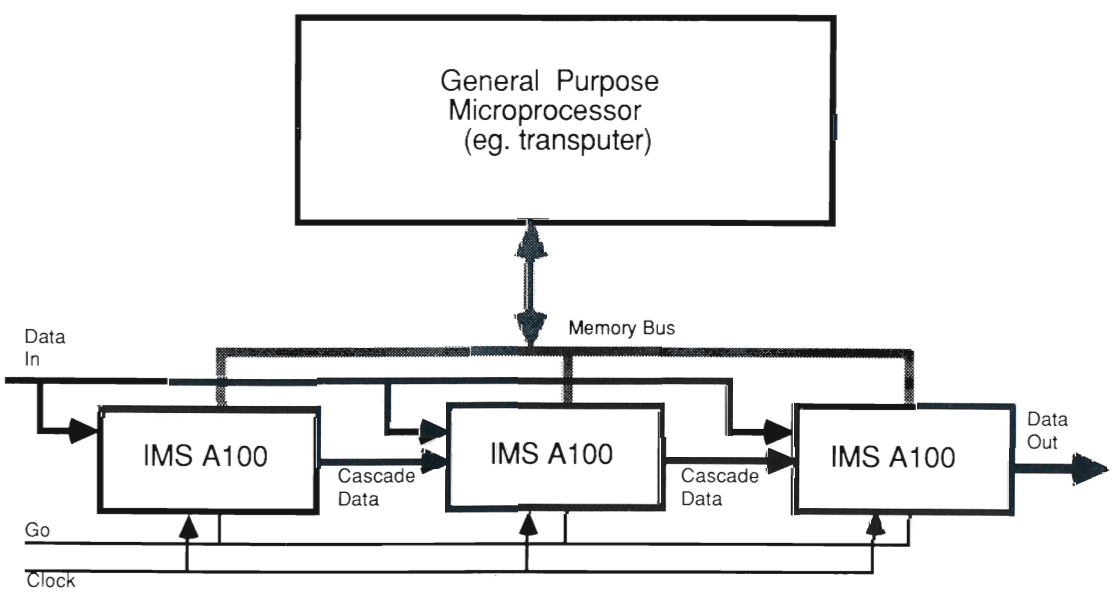


The IMS A100 has four interfaces through which data can be transferred. The memory interface port allows access to the coefficient registers, the configuration and status registers and the data input and output registers for the multiply accumulator array. Three dedicated ports are also provided, allowing high speed data input and output to the IMS A100 and the cascading of several devices. Typically a microprocessor will configure the IMS A100 via the memory interface, then in a simple system data input and output can be performed through the data input (DIR) and data output (DOL, DOH) registers. Alternatively in a higher performance system data transfer may be performed via the dedicated input and output ports. A typical IMS A100 based system is shown in Figure 3.

Two banks of coefficients are provided. At any instant one set of coefficients is in use within the multiply-accumulation array, the other set being accessible via the memory interface. Once a new set of coefficients has been loaded, the two coefficient banks can be interchanged by performing a write operation to the "Bank Swap" bit of a control register.

So that devices can be cascaded (eg. to construct long transversal filters), a 32 stage, 24 bit wide, shift register and 24 bit adder is included on chip. The output of one chip is connected directly to the cascade input of the next. The output of the shift register is added internally to the output of the programmable barrel shifter to give the final 24 bit output from the chip. To minimise pin count and external buses, the data output and the cascade input ports transfer 24 bit words as a pair of 12 bit words across a 12 bit wide multiplexed interface.

Figure 3 - A simple IMS A100 based system



DSP DEVELOPMENT SYSTEM

FEATURES

- Numerically accurate software simulation of IMS A100 cascadable signal processor and IMS B009 evaluation board facilities
- Comprehensive IMS A100 controller software (for the IMS T212 processor on the IMS B009 evaluation board)
- Interactive access to IMS A100s (simulation or hardware)
- User friendly software harness for rapid software development
- Wide range of examples to speed development of optimised solutions including FIR, DFT, Convolution, Correlation and Partitioning
- User friendly multi-window graphics interface
- Runs on IBM PC XT, AT (or compatible) with CGA/EGA and occam 2 Transputer Development System
- All software supplied in fully documented source and binary code
- Executes on IMS B004 or IMS B009-2 evaluation boards

DESCRIPTION

The IMS D703 DSP Development System is a complete software design environment for the development, execution, and debugging of IMS A100 based applications. The system executes on any IBM PC based transputer system, using an IMS T414 with at least 1 MByte of RAM.

By providing the user with a structured method for adapting the source code to model specific configurations, almost any IMS A100 based DSP system can be prototyped and its numerical performance evaluated. A number of example application tasks are supplied with the system, demonstrating most common algorithms and programming techniques. The full occam 2 high level concurrent programming language is used to provide an extremely powerful method of describing real systems, particularly those using dataflow techniques.

The system as supplied also provides an interactive simulator of a "raw" cascade of IMS A100s, ie. a cascade with a simple linear addressing scheme. The user can read and write locations interactively, or pass externally generated data files through the simulator, and capture results. This provides users with a "knife and fork" facility for manipulating the IMS A100 model cascade. The interactive simulator can be used in conjunction with application tasks, so that users can stop an application during execution, examine the contents of the IMS A100s, modify them if required, then restart the application.

As the IMS D703 was designed in conjunction with the IMS B009 IMS A100 Evaluation Board, a complete IMS B009 driver is included, together with a software emulation of the IMS B009 evaluation board itself.

The hardware driver is also supplied in source form, showing users how to exploit the advanced features of the IMS B009. Support libraries enable users to produce code that will execute unmodified on either the software or hardware version of the IMS B009, so that applications can be developed on a transputer-only system, and executed on an IMS B009 without modification.

The IMS D704 combines the IMS D703 with the IMS B009 to provide a complete package for enhancing any IBM PC or compatible into a high performance DSP workstation. It is also the ideal tool for developing IMS A100 based applications, and evaluating the potential of the IMS A100 in a wide range of environments.

Using the IMS B009 evaluation board, users can develop high performance real time systems, or use the board as a "number cruncher" coprocessor to the IBM PC.

External data can be supplied to, and read from the IMS B009, so that the board can be used in real systems, controlled by the IMS D703 environment.

The IMS B009 comes either with (IMS B009-2) or without (IMS B009-1) a host processing module, which comprises a 32-bit IMS T414 transputer with 1 MByte of DRAM. This optional module enables first time users to execute the full occam development system on the IMS B009 itself. Users already possessing the IMS D701 Transputer Development System need only obtain the IMS B009-1 and the IMS D703 to achieve the same functionality, though this solution does consume two IBM PC slots rather than one using the full IMS B009-2. Users should also note that the IMS D703 software can only be modified on an IBM PC based occam 2 transputer development system.

IMS D703

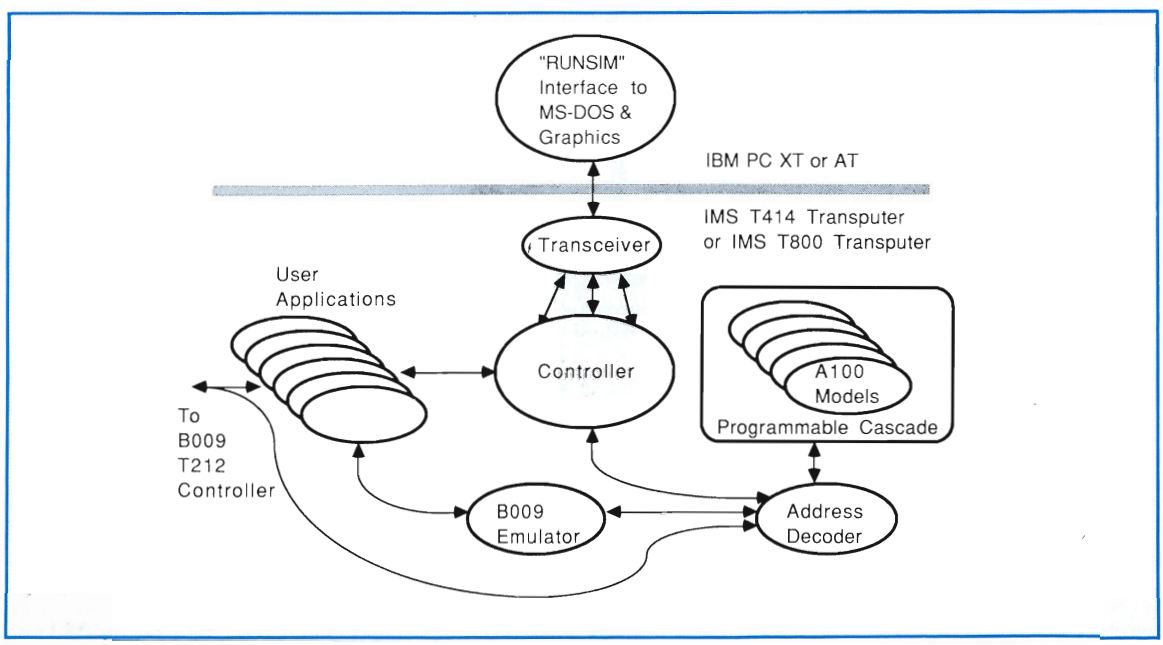
FEATURES

- DSP Development System software for use with Transputer Development System

IMS D704

FEATURES

- Complete DSP Development System
- Hardware/Software bundle for IBM PC XT, AT or compatible
- IMS D703, DSP software
- Transputer Development System software
- IMS B009-2, the IMS A100 Evaluation Board with 1 MByte Transputer module



IMS B009

IMS A100 Evaluation Board — IBM PC add-in board

FEATURES

- Cascade of four IMS A100 signal processors
- 1280 Million Operations Per Second (MOPS) capability
- Continuous data rates upto 10 MSamples/sec
- Fully programmable control of IMS A100 by IMS T212 16 bit transputer
- Option to install module with IMS T414 32 bit transputer and 1 Mbyte DRAM
- Arrayable for high performance pipelined systems
- General purpose address mapper (look Up Table) for data sequencing
- Data supplied from internal or external sources
- Controllable from IBM PC applications under MS-DOS or from other transputer systems
- IMS A100 cascade accessible directly from IBM PC bus

IMS B009-1

- Standard IBM PC add-in board format
- Four IMS A100s
- IMS T212 with 64 kByte SRAM
- IBM PC bus interface

IMS B009-2

IMS B009-1 plus

- Module with IMS T414 and 1 MByte DRAM

DESCRIPTION

The IMS B009 evaluation board enables the power of the IMS A100 Cascadable Signal Processor to be fully evaluated. Users of the IMS B009 are provided with a powerful combination of four IMS A100s and one or two transputers for implementation of a wide range of high performance DSP algorithms. By exploiting a range of I/O and hardware optimisation facilities, users can utilise the IMS B009 directly in real time applications such as video, audio, or communications.

A single IMS B009 is capable of performing 128 tap Finite Impulse Response filters (FIRs) at up to 2.5 MSamples/sec with 16 bit coefficients, or up to 10 MSamples/sec with 4 bit coefficients. Correlations and convolutions can be performed at similar rates. High speed DFTs can also be performed using Prime Number Transform techniques.

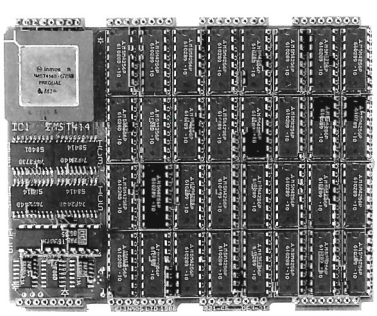
A variety of specialised features have been provided for optimised execution of DSP algorithms. These include special block move address modification decorders enabling the IMS T212 block move engine to pass data through the IMS A100's at maximum speed. Also included is a general purpose address mapper, which enables memory locations to be arbitrarily mapped for complex data sequencing tasks.

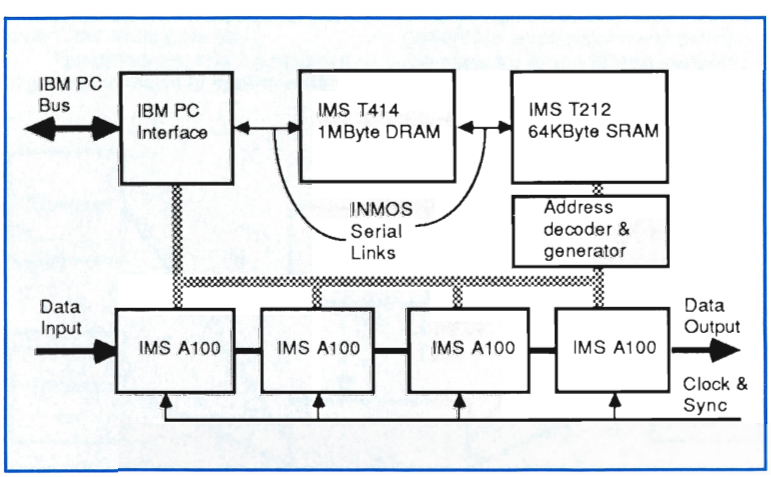
Multiple IMS B009 boards can be arrayed using the INMOS high speed serial links, for developing partitioned algorithms and/or pipelined applications. The use of standard INMOS links also enables users to connect to any transputer based system.

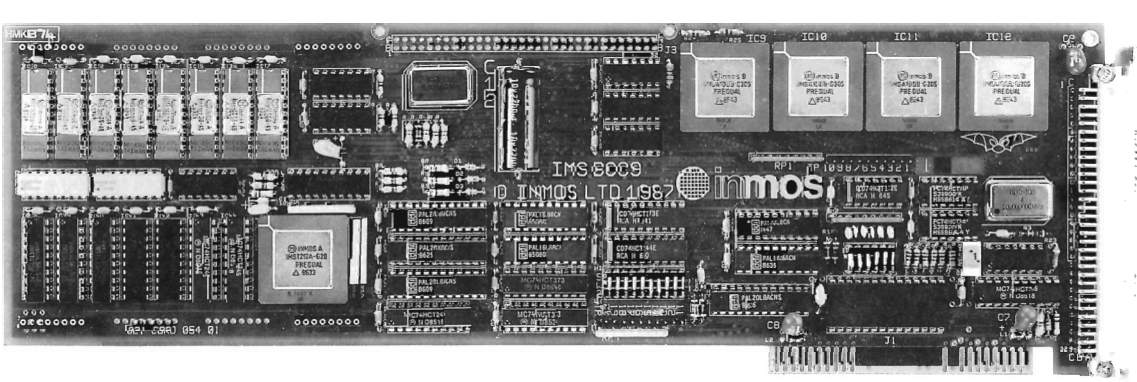
The IMS B009 contains an IMS T414 32 bit transputer with 1MByte DRAM, an IMS T212 16 bit transputer with 64kByte SRAM, and a cascade of four IMS A100s. The IMS T414 provides a general purpose host processor, capable of support ng the full INMOS occam/transputer development environment. The IMS T212 provides a high performance controller for the IMS A100 cascade.

The IMS T212 can be connected to the IMS T414 with one or more standard INMOS serial links, each link being capable of around 0.9MBytes/sec full data rate in either direction. The transputer links can also be used to connect to other transputer evaluation boards, or for arraying IMS B009s to form a high bandwidth signal processing pipeline. The IMS T414 can be upgraded to use the IMS T800 floating point transputer, which considerably improves processing performance.

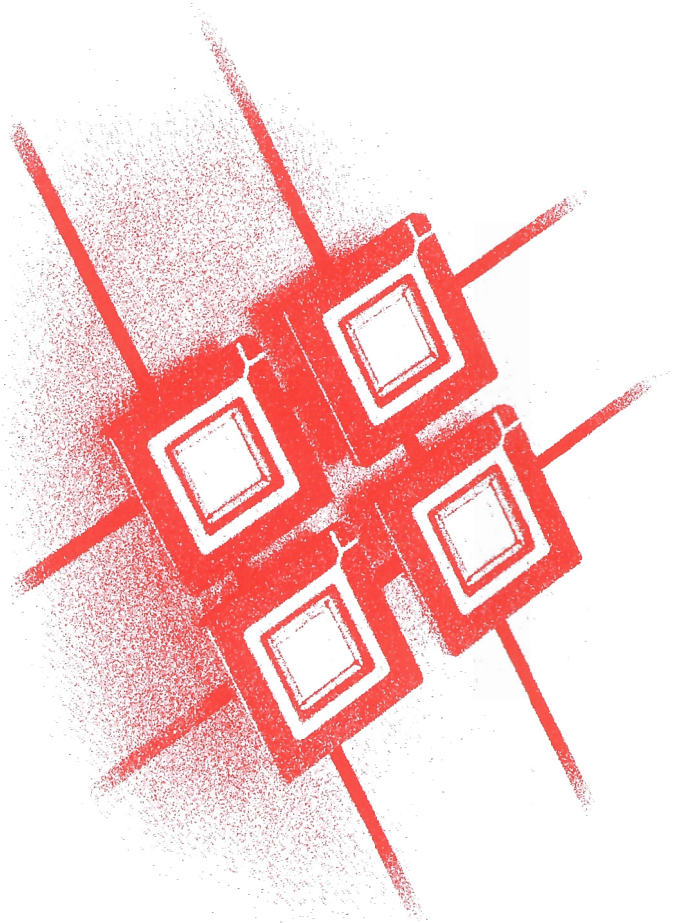
In order to maximise the range of applications of the IMS B009, most of the key control and data signals are brought to either the 96 way DIN 41612 connector, or to an internal connection area. This enables users to construct DMA interfaces to all devices on the IMS T212 memory interface bus. Thus, a wide range of real time interfaces can be realised, making the IMS B009 ideal for general laboratory use or prototyping of final systems.







EVALUATION BOARD



The transputer concept

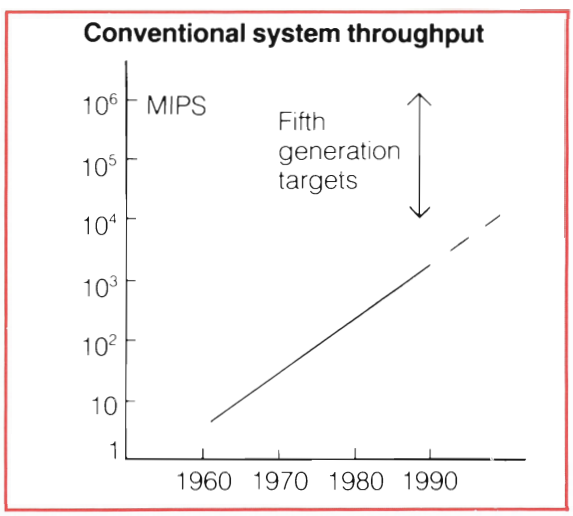
In the past, system performance has increased regularly by a factor of ten each decade. This improvement has been achieved largely by advances in circuit technology. For the future, VLSI offers the potential of much higher levels of integration, but only modest increases in circuit performance.

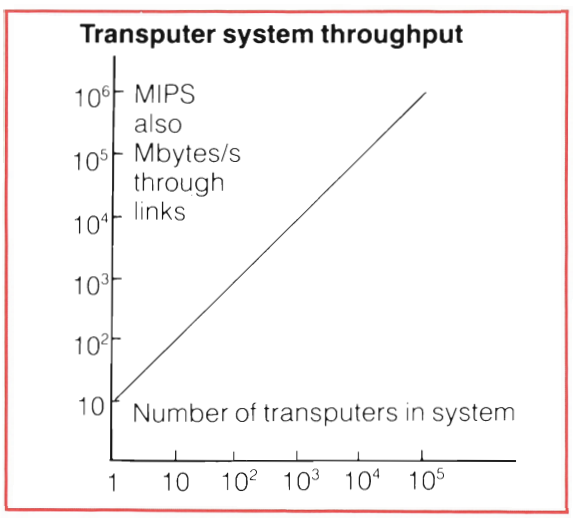
The economics of current systems are based on the historical perspective that processing is expensive in comparison with memory. This has led to the von Neumann bottleneck where a single processor is connected to vast amounts of memory. The economics of VLSI are different. Today, a single wafer of silicon can contain 16 Mbytes of static memory or 256 conventional microprocessors.

To exploit this potential it will be necessary to build systems with a much higher degree of concurrency than is currently possible. The transputer is designed as a programmable component to implement such systems. The term 'transputer' reflects this new device's ability to be used as a system building block. The word is derived from 'transistor' and 'computer', since the transputer is both a computer on a chip and a silicon component like a transistor.

The power of the transputer is that it creates a new level of abstraction. Just as the use of logic gates and Boolean algebra provides the design methodology for present electronic systems, so the transputer, together with the formal rules of occam, provides the design methodology for future concurrent systems.

In their proposals to achieve intelligent interaction between people and computers, the Japanese have projected the need for fifth generation computers with one thousand times the performance of present day systems. This will only be possible using concurrency, and the transputer has been designed to make such computers a reality.





The programmable component

The transputer is a programmable component.

It is designed to exploit the opportunity of VLSI, providing performance and convenience through simplicity. Its revolutionary architecture enables the potential of concurrency to be realized for the first time, making today's applications easier to implement and creating a new dimension for tomorrow's systems.

The transputer uses silicon capability to make programming simpler and to make engineering easier than for any previous microprocessor.

The architecture has been optimized to obtain the maximum of functionality for the minimum of silicon. It allows different trade offs between performance and cost, always giving an intrinsic advantage over older architectures.

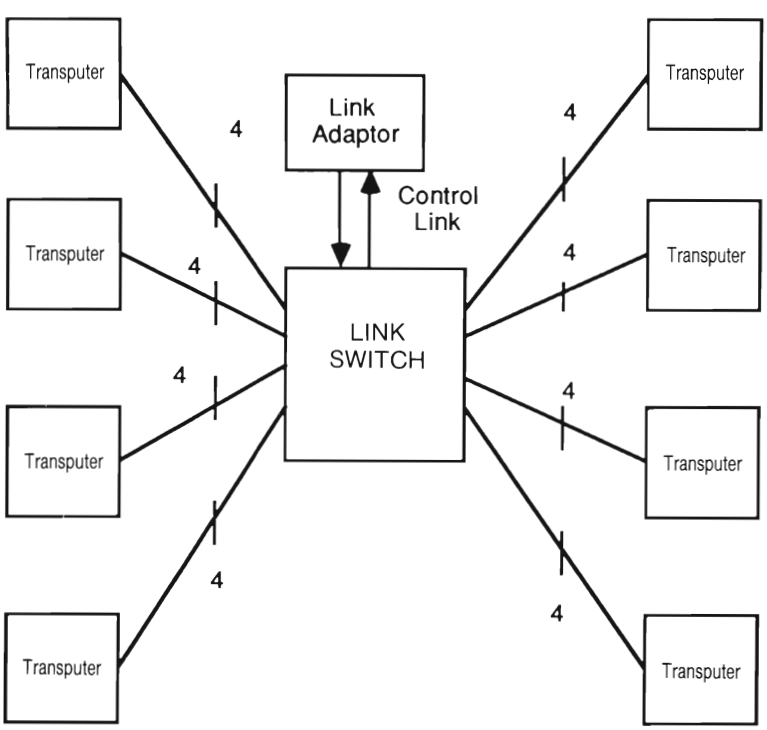
The architecture is future-proof. It spans the range of applications supercomputers. Transputers will exploit future levels of integration by increasing the amount of processing, memory, communications and concurrency within the same architecture.

Occam enables more powerful systems to be designed using interconnected transputers. Such concurrent systems unlock the processing potential of VLSI for fifth generation applications and provide the basis for future silicon systems.

THE PRODUCT RANGE

The range has now expanded beyond classical components and evaluation boards. INMOS now offers an integrated series of products which are:-

- TRANSPUTERS, as processors and peripheral controllers
- LINK SWITCH and ADAPTORS, particularly important as they allow the transputers high speed serial communications ports, up to four per device, to be switched in multi-transputer networks or interfaced to standard parallel bus structures.
- TRANSPUTER MODULES (TRAMs), the new range of supercomponents where a densely packaged transputer based subsystem is mounted into a unique module format, which in turn is plugged into a Motherboard. Each Motherboard holds up to 16 modules allowing reconfigurable transputer systems.
- BOARDS and DEVELOPMENT TOOLS, to run in industry standard development workstations.



inmos

TRANSPUTER FAMILY

IMS T800

FEATURES

- Integral hardware 64 bit floating point unit
- ANSI-IEEE 754-1985 Floating Point Representation
- 1.5 Sustained MegaFlops/sec
- Full 32 bit transputer architecture
- Pin compatible with the IMS T414-20 transputer
- 4 Kbytes RAM on chip for 80 Mbytes/sec data rate
- 32 bit configurable memory interface
- External memory bandwidth 26.6 Mbytes/sec
- High performance Graphics support
- Single 5 MHz clock input
- Typical power dissipation less than 1 Watt
- DRAM refresh control
- Four 10/20 Mbits/sec INMOS serial links
- External event interrupt
- Internal timers
- Support for run-time error diagnostics
- Boot from ROM or link
- 4 Mega Whetstone benchmark performance
- 84-Pin Ceramic PGA

DESCRIPTION

The IMS T800 is a 64-bit floating point member of the transputer family.

The IMS T800 integrates a 32-bit microprocessor, a 64-bit floating point unit, four standard transputer communications links, 4Kbytes of on-chip RAM, a memory interface and peripheral interfacing on a single chip, using a 1.5 micron CMOS process.

The 64-bit floating point unit provides single length and double length operation according to the ANSI-IEEE 754-1985 standard for floating point arithmetic and is able to perform floating point arithmetic operations concurrently with the processor, sustaining in excess of 1.25 MegaFlops.

The IMS T800 uses a DMA block transfer mechanism to transfer messages between memory and another transputer product via an INMOS link. The link interfaces and the processor all operate concurrently, allowing processing to continue while data is being transferred.

The 4 Kbytes of on chip static RAM provide a maximum data rate of 80 Mbytes/sec with access from both the processor and links. The IMS T800 can directly access a linear address space up to 4 Gbytes. The 32 bit wide external memory interface uses multiplexed data and address lines and provides a data rate of up to 26.6 Mbytes/sec.

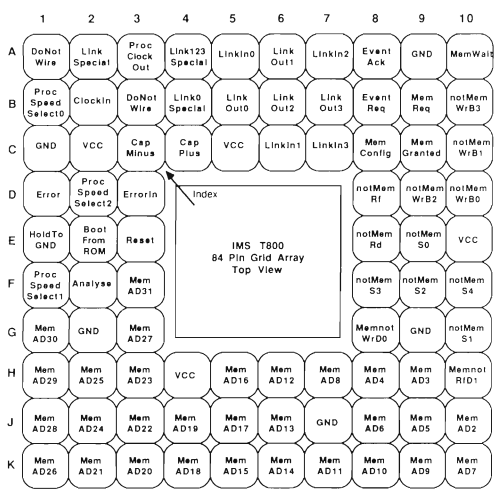
Processor	Whetstone/second single length
Intel 80286/80287 8 MHz	300K
IMS T414-20 20 MHz	663K
NS 32332-32081 15 MHz	728K
MC 68020/68881 16/12.5 MHz	755K
ATT 32000/32100	1000K
Intel 80386/80387 20 MHz	1800K
IMS T800-20 20 MHz	4000K

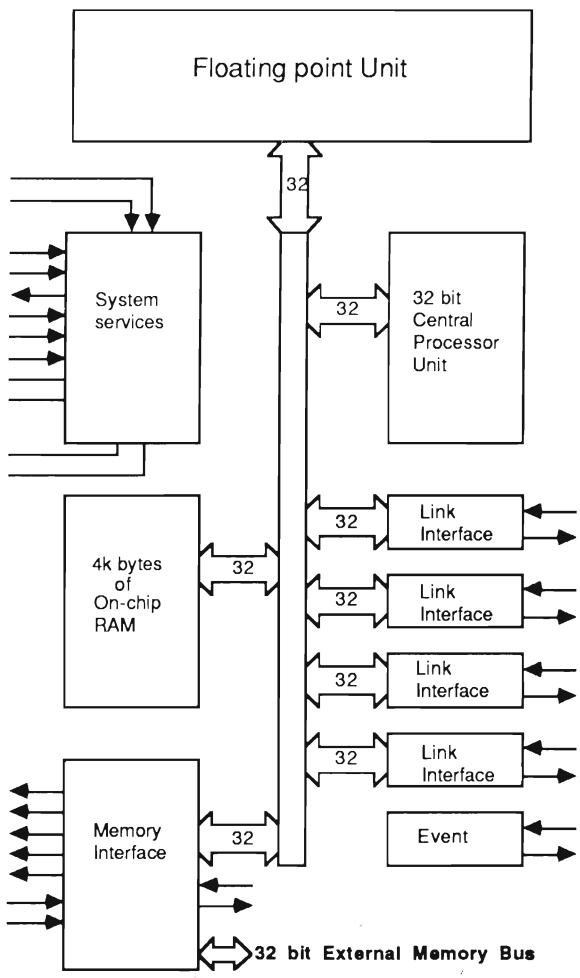
The IMS T800 has a microcoded graphics capability; three instructions increase the speed of operation when block transferring two dimensional arrays of bytes. Block moves operate at the speed of memory.

Instructions have been included in the IMS T800 to provide the ability to perform Cyclic Redundancy Checks (CRC) on serial data streams of arbitrary length. Cyclic redundancy checks are used to provide error detection in situations where data integrity is critical.

Designation	Processor clock speed	Processor cycle time	Input clock frequency
IMS T800-17	17.0 MHz	58.8 ns	5 MHz
IMS T800-20	20.0 MHz	50.0 ns	5 MHz

Faster processor clock versions due during 1988





IMS T414

FEATURES

- 32 bit architecture with 10 MIPS performance
- 2 Kbytes 50 ns RAM on chip
- Four 5/10/20 Mbits/sec INMOS serial links
- 32 bit configurable memory interface
- Directly addresses 4 Gbytes at 26.6 Mbytes/sec
- Hardware scheduler for concurrent programs
- Sub-microsecond context switch
- Internal timers for real time processing
- External event interrupt
- Sub-microsecond typical interrupt latency
- Boots from communication link or ROM
- On-chip DRAM controller
- Single 5 MHz clock input
- 84-Pin Ceramic PGA and 84-Pin Plastic J-Lead

DESCRIPTION

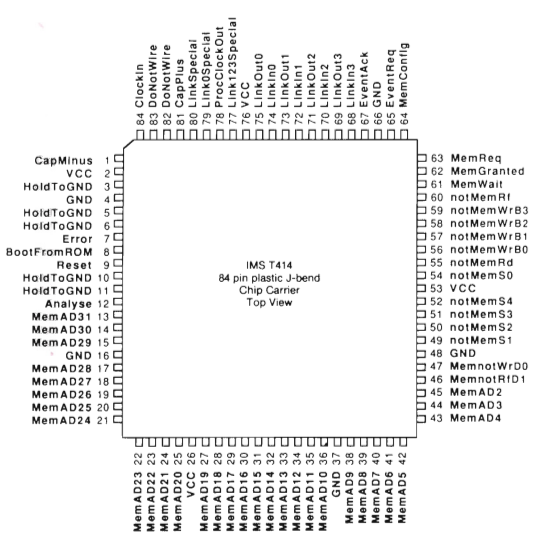
The IMS T414 transputer is a 32 bit microcomputer with 2 Kbytes on-chip RAM for high speed processing, a configurable memory interface and four standard INMOS communication links. The instruction set achieves efficient implementation of high level languages and provides direct support for the occam model of concurrency when using either a single transputer or a network. Procedure calls, process switching and typical interrupt latency are sub-microsecond. The IMS T414 provides high performance arithmetic and microcode support for floating point operations. A device running at 20 MHz achieves an instruction throughput of 10 MIPS.

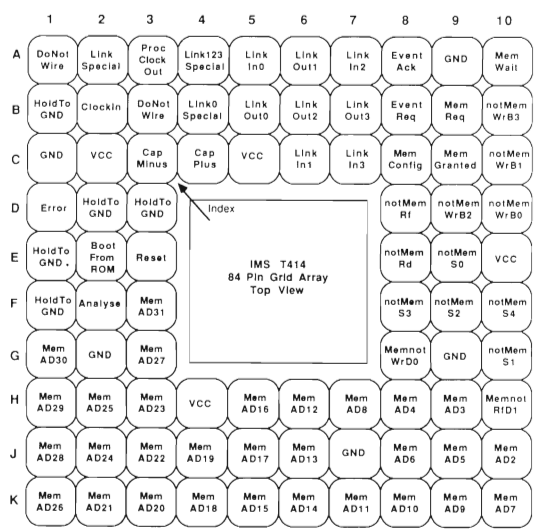
The IMS T414 can directly access a linear address space of 4 Gbytes. The 32 bit wide memory interface uses multiplexed data and address lines and provides a data rate of up to 4 bytes every 150 nanoseconds (26.6 Mbytes/sec) for a 20 MHz device. A configurable memory controller provides all timing, control and DRAM refresh signals for a wide variety of mixed memory systems.

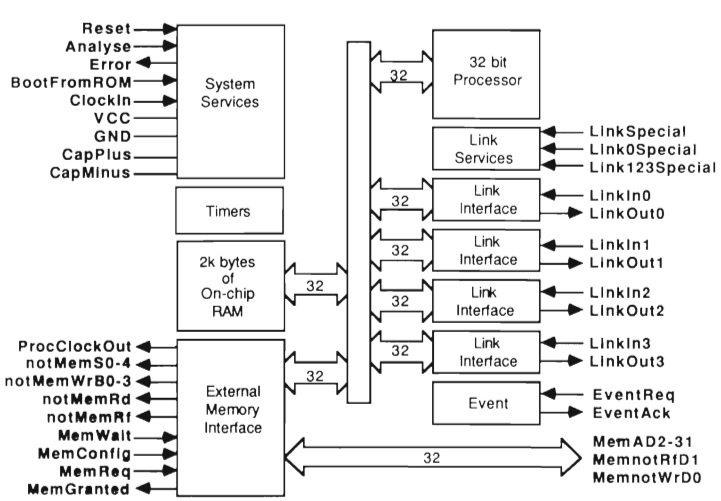
System Services include processor reset and boot control, together with facilities for error analysis.

The INMOS communication links allow networks of transputers to be constructed by direct point to point connections with no external logic. The links support the standard operating speed of 10 Mbits per second, but also operate at 5 and 20 Mbits per second.

The IMS T414 is designed to implement the occam language, but also efficiently supports other languages such as C, Pascal and Fortran.







32 BIT TRANSPUTER

IMS T212

FEATURES

- 16 bit 10 MIPS processor
- 64Kbytes linear address space
- 16 bit wide 20 Mbyte/sec memory interface
- Configurable on-chip memory controller
- 2 Kbytes high speed on chip RAM
- 4 inter-transputer links, each with full duplex DMA transfer capability up to 20 Mbits/sec
- Advanced 1.5 micron CMOS technology
- 68-Pin Ceramic PGA and 68-Pin Plastic J-Lead

DESCRIPTION

The IMS T212 integrates a 16-bit microprocessor, four standard transputer communications links, 2 Kbytes of on-chip RAM, a memory interface and peripheral interfacing on a single chip, using a 1.5 micron CMOS process.

The design achieves compact programs, efficient high level language implementation and provides direct support for the occam model of concurrency. Procedure calls, process switching and interrupt latency are all sub-microsecond.

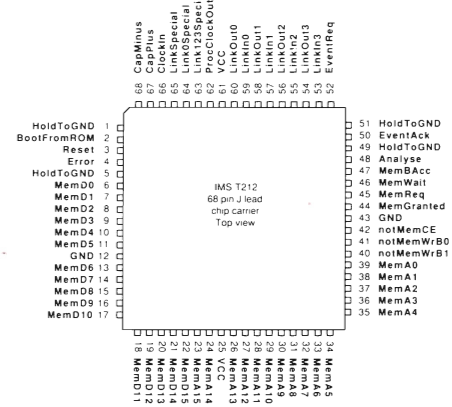
The processor shares its time between any number of concurrent processes. A process waiting for communication or a timer does not consume any processor time. Two levels of process priority enable fast interrupt response to be achieved.

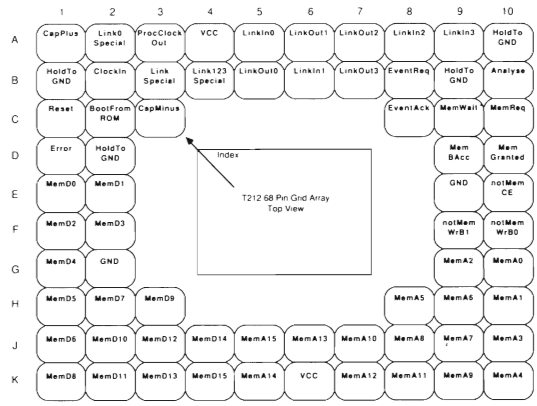
The T212 uses a DMA block transfer mechanism to transfer messages between memory and another transputer product via the INMOS links. The link interfaces and the processor all operate concurrently, allowing processing to continue while data is being transferred on all of the links.

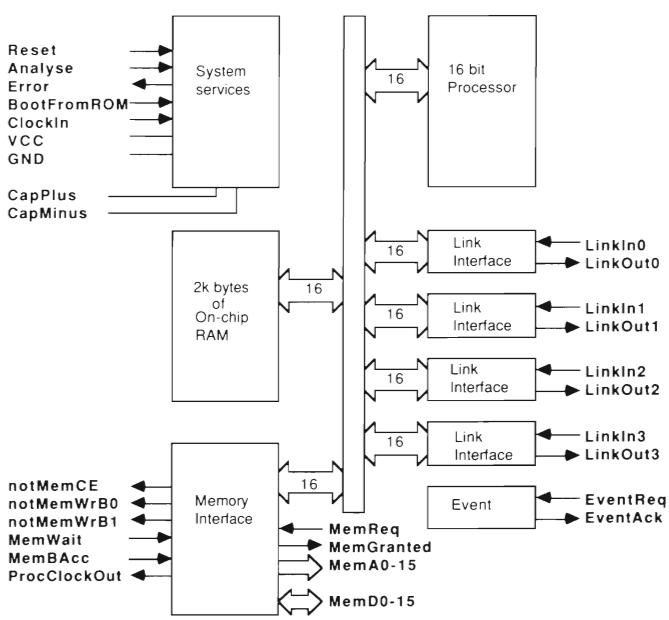
The 2 Kbytes of static RAM provide a maximum data rate of 40 Mbytes/sec with access for both the processor and links.

The T212 can directly access a linear address space up to 64 Kbytes, and has a 16-bit wide data bus and a 16-bit wide address bus, non-multiplexed, providing a data rate of up to 20 Mbytes/sec, and supporting word or byte organisation. The data bus can be dynamically configured to be 16-bits or 8-bits wide.

The memory controller supports memory mapped peripherals, which may use DMA. Links may be interfaced to peripherals via an INMOS link adaptor. A peripheral can request attention via the event pin.







IMS M212

FEATURES

- Soft-sectored winchester or floppy disk controller
- ST506/ST412 compatible disk interface
- On-chip data separation and precompensation
- 16 bit 10 MIPS processor
- 2 Kbyte high speed on-chip RAM
- User programmable
- 2 inter-transputer links, each with full duplex DMA transfer capability up to 20 Mbits/sec
- Advanced 1.5 micron CMOS technology
- 68-Pin Ceramic PGA and 68-Pin Plastic J-Lead

DESCRIPTION

The IMS M212 disk processor contains a 16-bit processor capable of 10 MIPS with on chip memory, 2 byte-wide programmable, bi-directional ports and disk interface hardware providing a standard floppy or winchester disk interface.

Software, resident in an on-chip ROM, enables the M212 to interface, via two INMOS links, directly to winchester or floppy disk drives with no additional software development and the minimum of external hardware. The links can connect to any transputer based system or, via a link adaptor, to a conventional microprocessor system. Additional software may be provided by the designer to enhance the functionality of the M212.

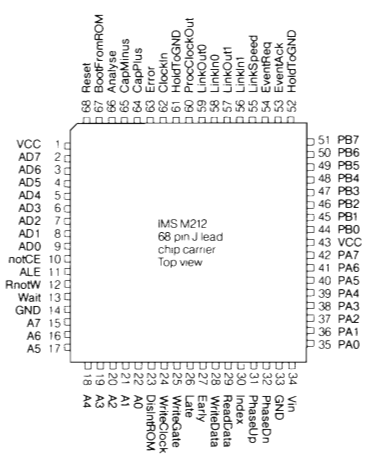
The bi-directional parallel ports are used to control disk functions such as head position and selection, disk status reads etc.

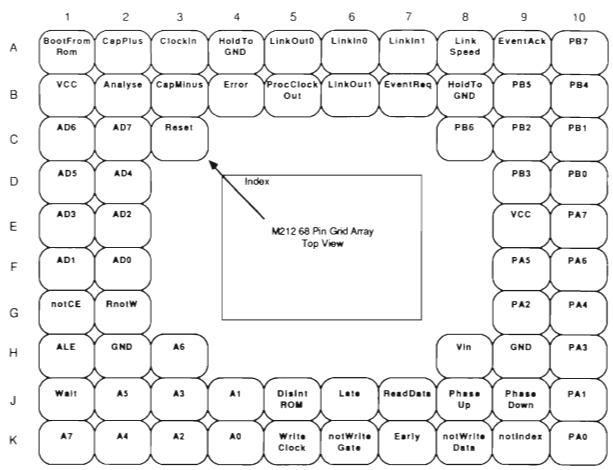
The disk hardware is controlled via on-chip hard channels using a simple command protocol.

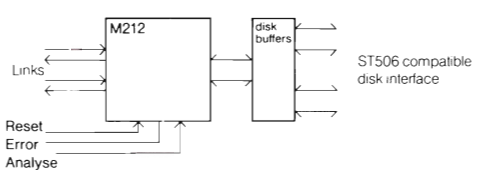
The on-chip RAM can be used for program or data storage, as a sector buffer or to store parameters and format information.

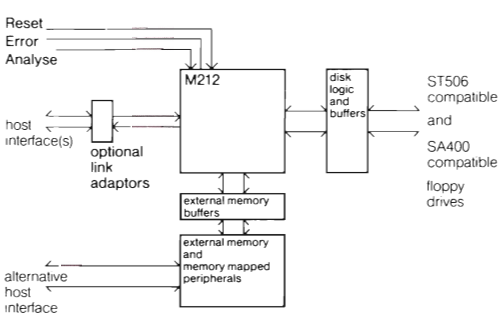
The memory can be extended off chip using the external memory interface.

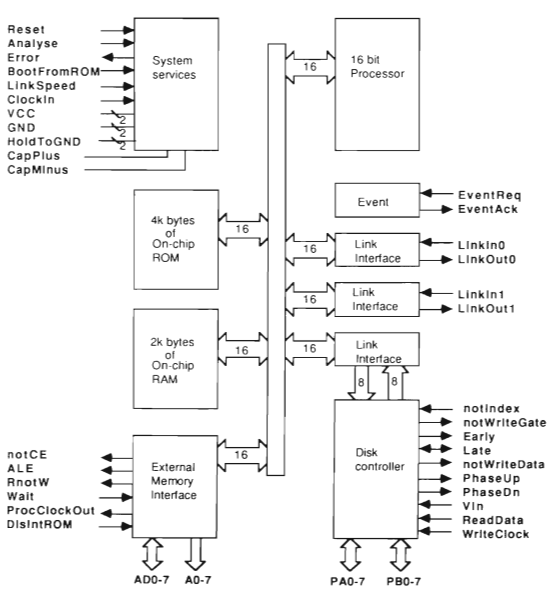
The M212 has been designed to interface with minimal support logic to small (5.25 in. or 3.5 in.) soft sectored winchester or floppy disk drives.











DISK PROCESSOR

IMS C004

FEATURES

- Programmable 32 way crossbar switch
- Standard INMOS links
- Regenerates input signal
- Cascadable to any depth
- No loss of signal integrity
- 10 or 20 Mbits/sec operating speed
- Separate INMOS configuration link
- TTL and CMOS compatible
- Single +5V ± 10% power supply
- 84-Pin Ceramic PGA

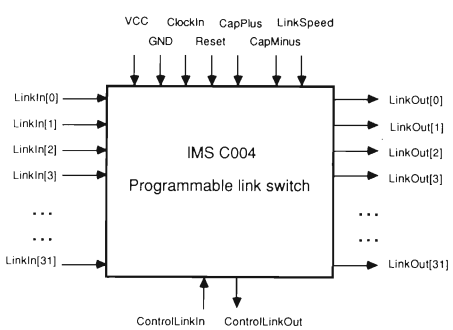
DESCRIPTION

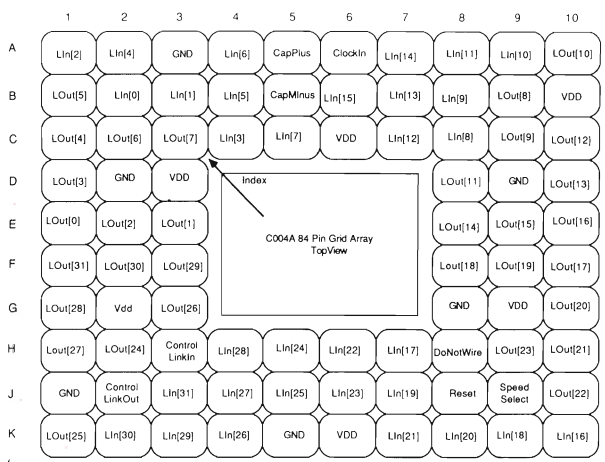
The IMS C004 programmable link switch provides a full crossbar switch between 32 link inputs and 32 link outputs. It will switch links running at standard transputer speeds (10 and 20 Mbaud). And only introduces a 1.6 to 2 bit time-delay on the signal.

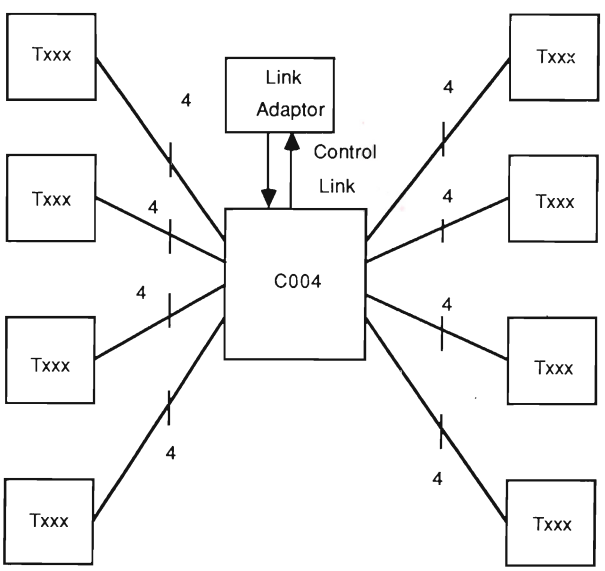
It can be cascaded to any depth without loss of signal integrity and it can be used to construct reconfigurable networks of arbitrary size.

The C004 is programmed via a separate serial link called the configuration link.

One C004 can set up all possible networks of 8 transputers. Four C004 chips can set up all possible networks of 32 transputers. It can also be used as a component of a larger switching system. The C004 switch allows dynamic reconfiguration of transputer networks providing there is no link activity on the links to be switched at reconfiguration time.







FEATURES

- High performance system interconnect
- Bi-directional handshaken byte-wide interface
- INMOS serial link
- 10 or 20 Mbits/sec data rate
- Interrupt control for microprocessor buses
- Two configuration options
- Advanced 1.5 micron CMOS technology

IMS C011
- 28-Pin, 600-mil DIP

IMS C012
- 24-Pin, 300-mil DIP

APPLICATIONS

- Programmable I/O pins for a transputer
- Link between transputers running at different clock frequencies
- Interface between transputers and industry standard peripherals
- High performance handshaken link between standard microprocessor buses

DESCRIPTION

The IMS C011/12 link adaptors offer a universal high speed system interconnect, providing full duplex communication according to the INMOS serial link protocol. The link protocol provides synchronised message transmission using handshaken byte streams. Data reception is asynchronous, allowing communication to be independent of clock phase.

The IMS C011 converts the bidirectional serial link data into parallel data streams. It can be used to freely inter-connect transputers, INMOS peripheral controllers, I/O subsystems, and microprocessors of different families.

The serial links can be operated at differing speeds: two C011 link adaptors can connect high and low speed links whilst maintaining the synchronised message transmission provided by the link protocol.

IMS C011

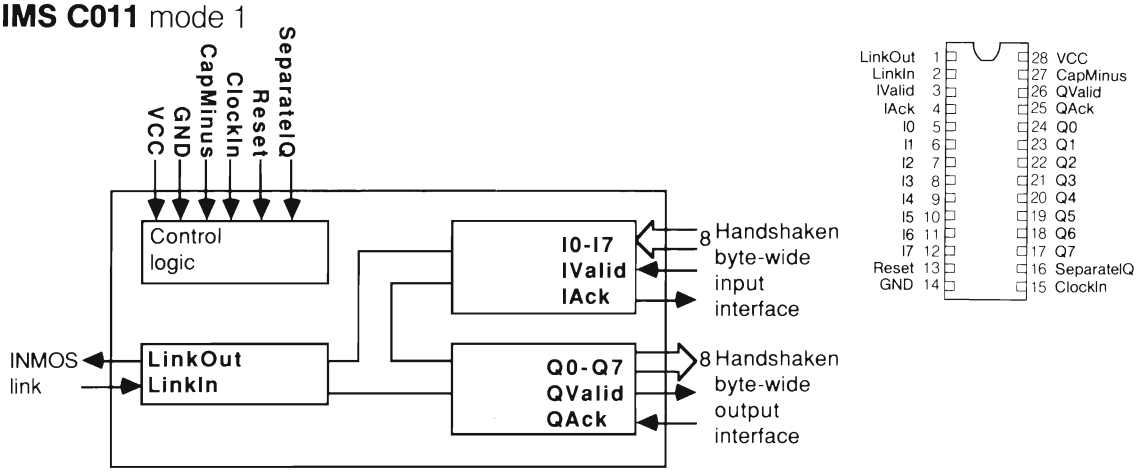
In mode 1 the link adaptor converts between an INMOS serial link and two independent fully handshaken byte-wide interfaces. One interface is for data coming from the serial link and one for data going to the serial link.

IMS C011/12

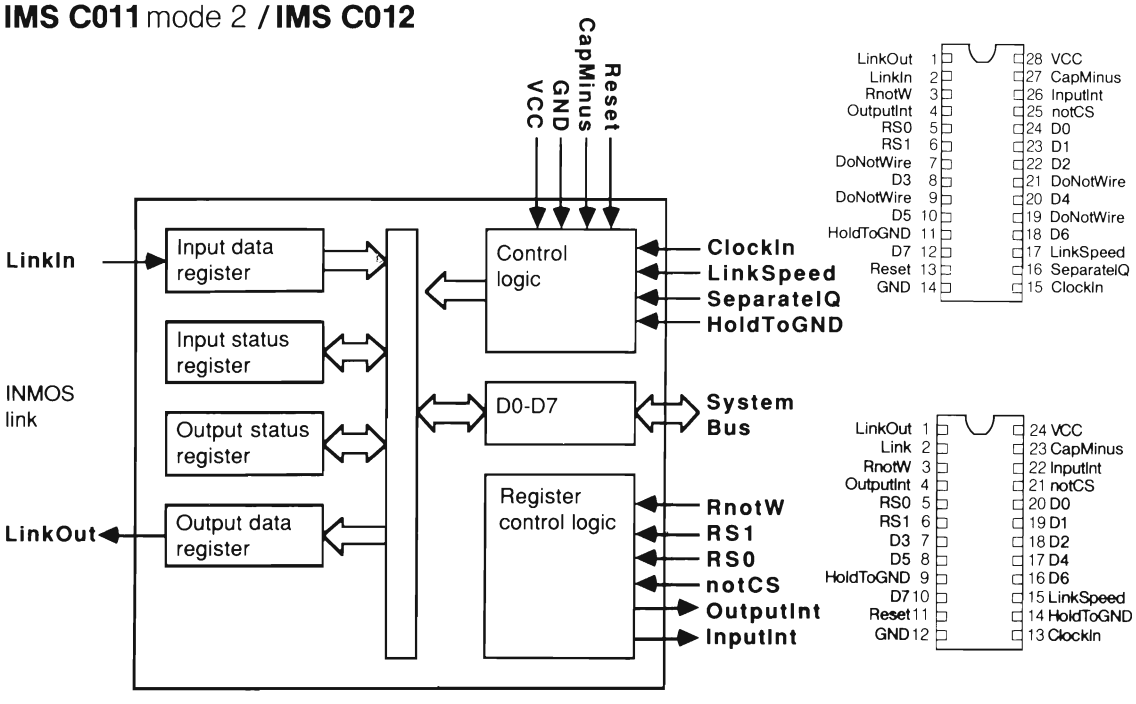
The IMS C011 mode 2 and IMS C012 link adaptors provide an interface between an INMOS serial link and a microprocessor system bus, via an 8-bit bi-directional interface.

This mode has status/control and data registers for both input and output. Any of these can be accessed by the byte wide interface at any time. Two interrupt lines are provided, each gated by an interrupt enable flag. One presents an interrupt on output ready, and the other on data present.

IMS C011 mode 1



IMS C011 mode 2 / **IMS C012**



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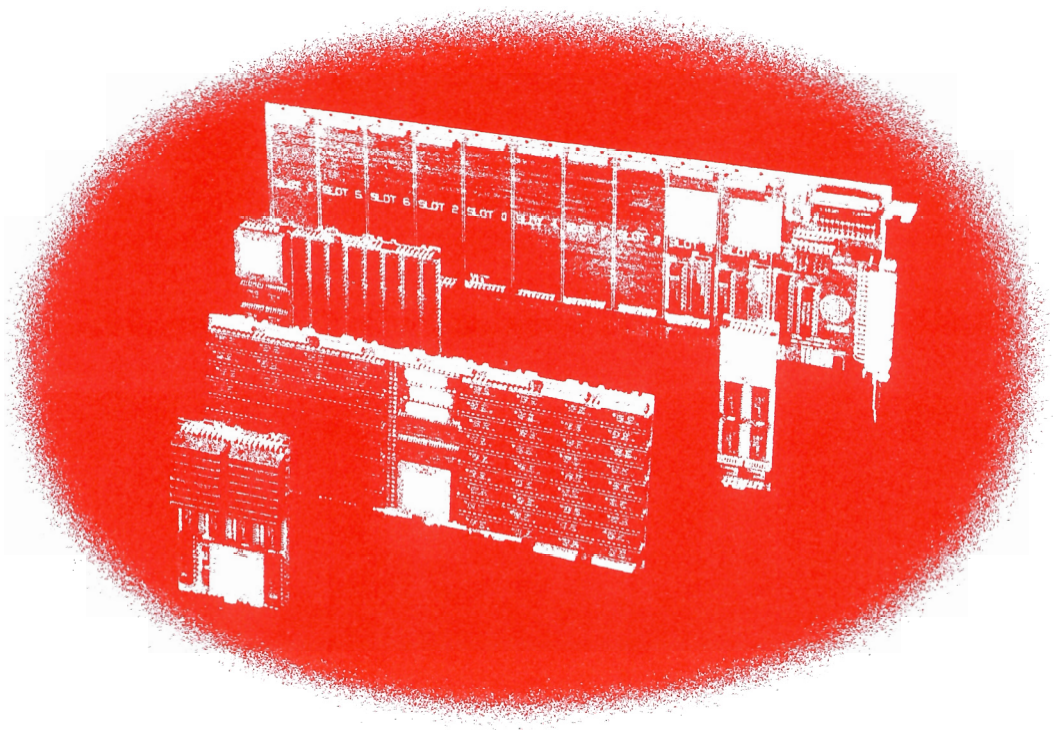
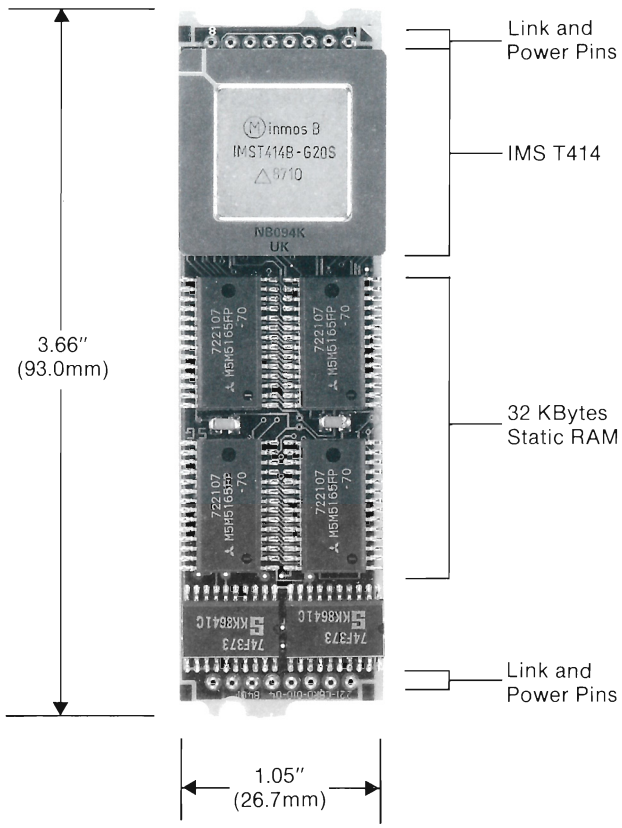
TRANSPUTER BOARDS



INMOS Transputer Boards

The INMOS range of transputer evaluation boards has now been complemented with a new range of modular components and motherboards. This evolution was driven by the need to allow highly flexible transputer systems to be constructed for finished equipment and evaluation use. The new concept now allows the communications capability of transputers to be exploited using a small number of component parts to satisfy the wide need for power and flexibility. All part of the transputer revolution.

The TRAnsputer Module (TRAM) concept is simple, based on a series of small PCBs (size 1 is 3.66" x 1.05" with sizes 2, 3, 4 etc. simple multiples of size 1). Each module fits into an array of standardized sockets on any of the range of motherboards. TRAMs are stackable allowing the user to create highly flexible multi-processor systems. A typical subsystem on a TRAM would be a 32Bit transputer with an array of Static RAM connected to the memory interface ie. the IMS B401. Standard buffered INMOS link connections are provided on all TRAMs; this allows the simple interconnection of multi-transputer networks on each motherboard.



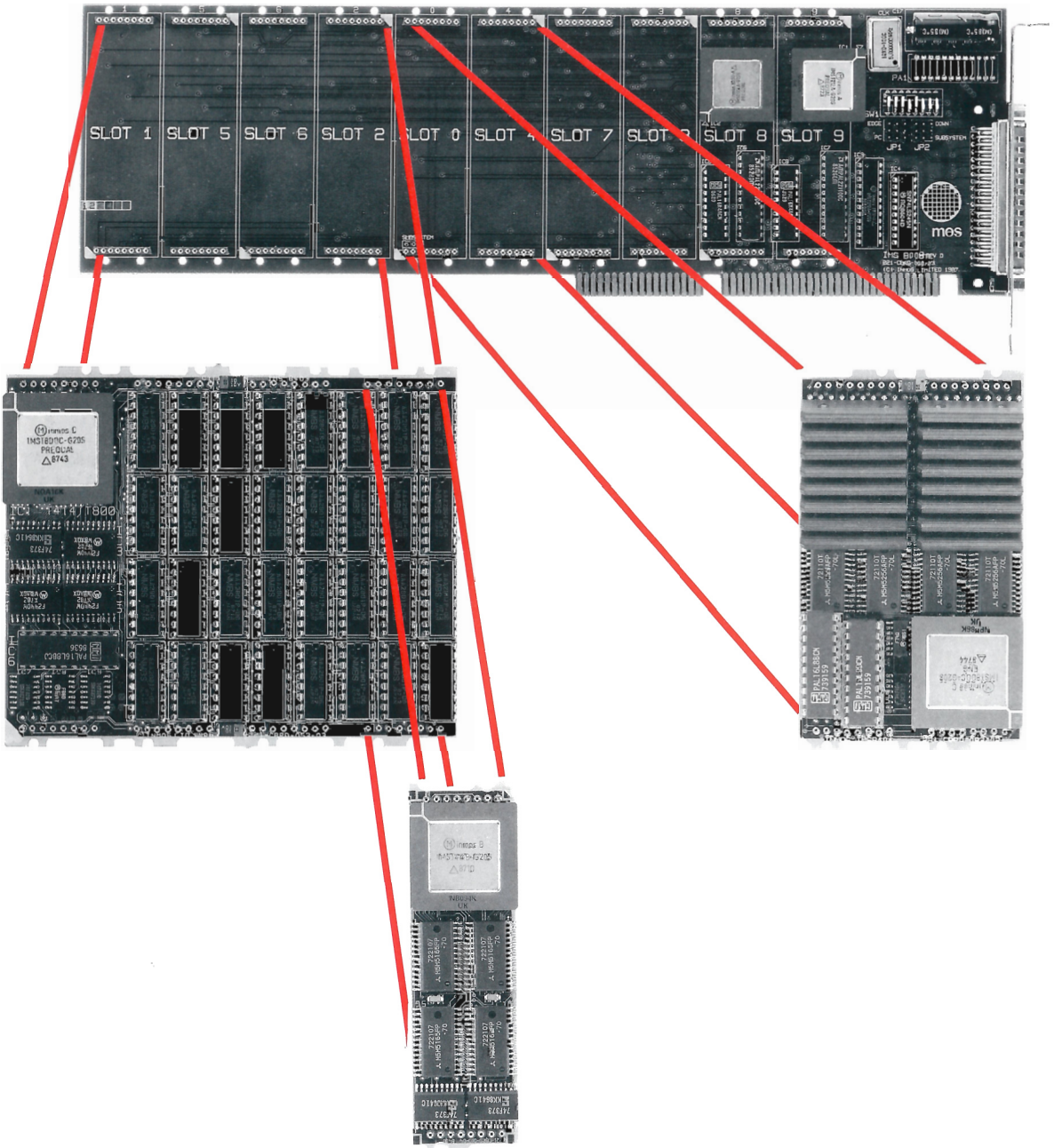
IMS B401 TRAM

Larger arrays or widely distributed systems are now feasible using the INMOS link connections available on all the motherboards and configured boards. The controlling software, either OCCAM or one of the supported scientific languages as outlined in the Development Tools section, is compiled and configured for the network of boards using the Transputer Development System; the resulting code is then down loaded and distributed into the system to be executed.

INMOS' board and TRAM system supports the complete transputer range, with more TRAMs and Motherboards to follow from both INMOS and Third-Party vendors. The TRAM standards are published and freely available allowing independent development and support. This has set a new standard in the simplicity and cost effectiveness with which multi-processor systems can now be built.

Application Areas

- Industrial OEM
- PC add-in/turbo boards
- Super components
- Prototype and development



The INMOS TRAM and MOTHERBOARD family

The INMOS Transputer Modules (TRAMs)

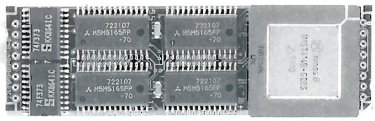
- Standard technology
- Expandable
- Stackable
- Upgradeability
- Flexibility
- Cost effective
- Fast design cycles
- INMOS commitment to latest silicon products on TRAMs
- Third-Party vendors

IMS B401 TRAM

FEATURES

- IMS T414 or IMS T800 transputer
- 32 KBytes no-wait-state static RAM
- Stackable
- Size 1

The IMS B401 (TRAM) is a low cost, high performance, high density, 16 pin transputer ideal for applications where 2 KBytes or 4 KBytes of on-chip RAM is not quite enough. The 32 KBytes of off-chip RAM is more than was sold on many PDP8's, and is ideal for systolic processing, signal processing, feature extraction etc. The IMS B008, fitted with ten IMS B401-3 TRAMSs, offers 40 MWhetstones/s in a single slot of an IBM PC (*). In the INMOS ITEM, 160 IMS B401-2s would offer the user 1.6 GIPS (1600 MIPS) and 5 MBytes.



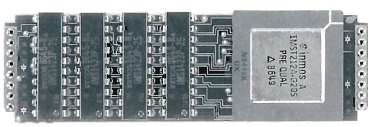
(*) For IBM PC read: Original PC, XT, AT, PS2 Model 30 and most clones.

IMS B402 TRAM

FEATURES

- IMS T212 transputer
- 8 KBytes no-wait-state static RAM
- Stackable
- Size 1

The IMS B402 (TRAM) is useful for similar applications as the IMS B401 (TRAM), as well as communications. The faster multiplication of the 16 bit transputer and the faster external memory interface give the IMS B402 higher performance than the IMS B401 for fixed point signal processing and feature extraction. Even with programmed floating point, the IMS B402 delivers 127 KWhetstones/s. Occam makes it easy to program 16 bit integers on this 16 bit processor, for high precision arithmetic and operations on sets. The IMS B402 is also ideal for message switching, for intelligent control of IMS C004 link switches, and for protocol conversion.



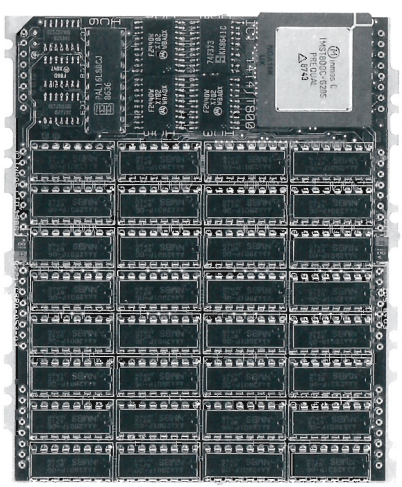
IMS B403 TRAM

FEATURES

- IMS T414 or IMS T800 transputer
- 1 MByte no-wait-state dynamic RAM
- Stackable
- Size 4

The IMS B403 (TRAM) provides the ultimate performance for a full 1 MByte of RAM, offering 4 MWhetstones/s with the IMS T800-20 transputer option. Rather than use expensive 256K SRAM's, which would take up much more board area, the IMS B403 uses 60 ns access time DRAM's, designed by INMOS.

Using IMS B403's, the INMOS ITEM (IMS B211) will hold 40 transputers, offering a total of 40 MBytes, 3 cycle memory and fully flexible network configurations.



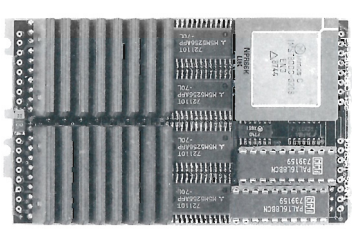
IMS B404 TRAM

FEATURES

- IMS T800 transputer
- 2 MBytes single wait-state dynamic RAM
- 128 KBytes zero wait-state static RAM
- Stackable
- Size 2

The IMS B404 (TRAM), of all INMOS board level products, has the highest packing density of silicon; 11 cm^2 on a board the size of a credit card. Its speed has been enhanced by extending the principle of fast on-chip RAM to include 128 KBytes of SRAM.

Four IMS B404s fit on to the IMS B008 in a single slot of the IBM PC (*). Eighty IMS B404's fit into an INMOS ITEM (IMS B211), to give 160 MBytes, 800 MIPS, 320 MWhetstones, with space to spare for other modules.



(*) For IBM PC read: Original PC, XT, AT, PS2 Model 30 and most clones.

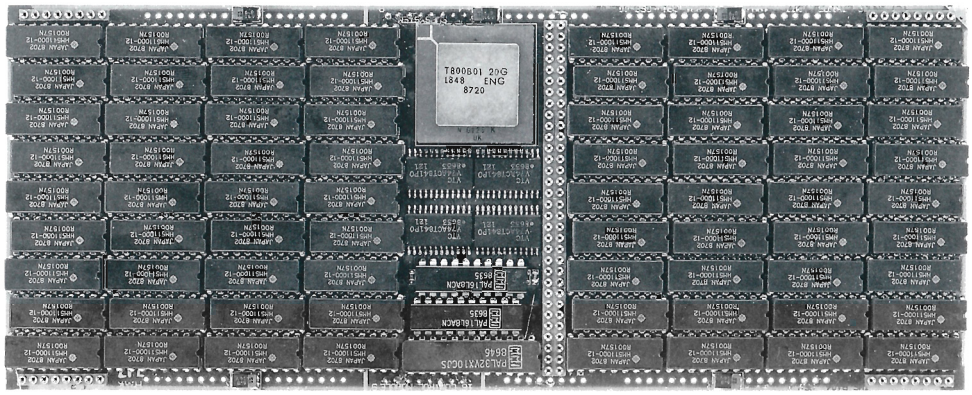
IMS B405 TRAM

FEATURES

- IMS T800 transputer
- 8 MBytes DRAM
- Stackable
- Size 8

The IMS B405 (TRAM) puts 8 MBytes, with parity, on to a module that fits comfortably on a IMS B008 in the IBM PC (*). This is considerably more volume efficient that a 20 MByte Winchester disk and makes the board ideal for running existing large programs, such as CAD, AI or simulation.

(*) For IBM PC read: Original PC, XT, AT, PS2 Model 30 and most clones.



MOTHERBOARDS (FOR TRAMs)

IMS B008

IBM PC Motherboard

FEATURES

- 10 transputer module (TRAM) slots
- IMS T212 transputer
- IMS C004 programmable 32 way switch
- IBM PC(*) format

DESCRIPTION

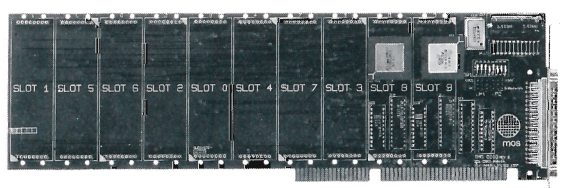
The IMS B008 takes up one slot in the IBM PC (*) and provides ten slots for the INMOS TRAMs. With one IMS B404 TRAM it offers an IBM PC board with 2 MBytes and a turbocharging performance of ten times that of the IBM PC AT. The IMS B008 with a IMS B404 and two IMS B401's gives 60 times the PC AT performance i.e. a program that takes one hour on the AT takes one minute on the IMS B008, a program that takes one minute on the AT takes one second on the IMS B008.

Many different module combinations can be based on the IMS B008 board and if more than one PC slot is available the modules are designed to be stacked. A system might be built from a IMS B405, two IMS B403's, four IMS B404's and two IMS B401's. This gives nine transputers, 18 MBytes and around 20 MWhetstones (double precision) using IMS T800 transputers. Such a combination would take up the space of two PC slots and less than 10 amps.

For developing appropriate network topologies the IMS B008 is ideal. The IMS C004 link switch allows the user to connect the transputers on the board as needed, direct from the keyboard without doing any wiring. The transputers can be arranged as a lattice, a cube, a Petersen net and a variety of trees. A total of twelve links are routed to a 37 way D style connector to give a robust and screened connections to other boards or boxes.

The IMS B008 is the ideal building base. With a low starting cost and low incremental cost for each module, the user can slowly build up a personal "Incremental Supercomputer".

(*) For IBM PC read: Original PC, XT, AT, PS2 Model 30 and most clones.



IMS B012

Double Eurocard Motherboard

FEATURES

- 16 transputer module (TRAM) slots
- IMS T212 - 16 bit transputer
- Two IMS C004 programmable 32 way switches
- Double Extended Eurocard

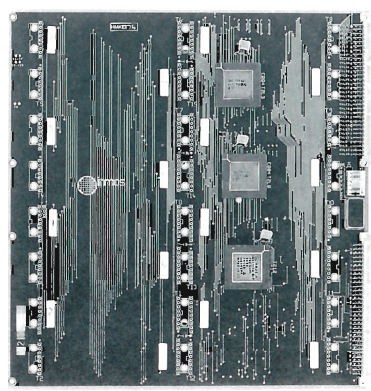
DESCRIPTION

The IMS B012 provides 16 slots for TRAMs, with IMS C004's to provide a wide variety of configurations. The IMS B012 can be populated with two IMS B405 modules to give 2 transputers and 16 MBytes per IMS B012, or with 16 IMS B401's to give 160 MIPS per IMS B012, or any other mix of TRAMs. A possible application might be an image or speech recognition system using eight IMS B401's for feature extraction and a IMS B405 running LISP or another AI language for recognition.

Ten IMS B012's in an INMOS ITEM offer a huge range of machine performance, from above 50 MWhetstones and 160 MBytes (using IMS B405's) to 160 MWhetstones and 5 MBytes (using IMS B401's).

Networks that can be built on the IMS B012 or on multiple IMS B012's include pipes, rings, lattices, (hyper)cubes, toroids and trees.

The IMS B012 can also be used as a "telephone exchange" for links from other boards. For example a system could be built in an ITEM from eight IMS B003's and two IMS B012's. One would be used to make all the North/South link connections between the IMS B003's, the other would be used to make all the East/West link connections between the IMS B003's.



IMS B006

Double Eurocard Motherboard

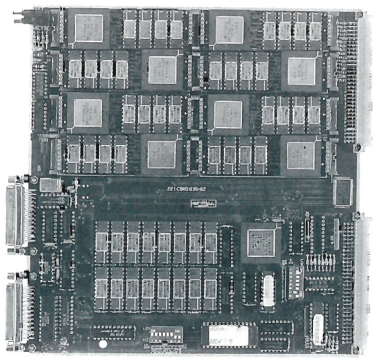
FEATURES

- 8 transputer module (TRAMs) slots
- IMS T212 - 16 bit transputer
- Two RS232 ports
- INMOS serial links
- Double Extended Eurocard

DESCRIPTION

The IMS B006 board enables users to evaluate and demonstrate the IMS T212 transputer.

The IMS B006 is supplied with one T212 transputer, which provides access to the EPROM, UART and switches. It can accommodate up to 8 additional transputer modules.



IMS B010

NEC PC Motherboard

FEATURES

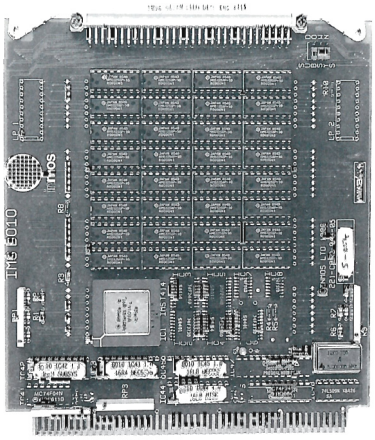
- 4 transputer module (TRAMs) slots
- IMS T414 and 1 Mbyte of dynamic RAM
- The PC-9801 subsystem logic, which allows a program running on the PC 9801 to Reset and Analyse systems
- The IMS C012 link adaptor
- NEC PC-9801 compatible

DESCRIPTION

The IMS B010 add-in board for the NEC PC-9801 Personal Computer enables users to evaluate and demonstrate the use of transputers.

The board provides standard INMOS link connections and external control of the transputer's reset and analyse functions. This allows it to control a subsystem consisting of other compatible boards, or to be a component of such a subsystem.

These three distinct parts of the board are joined together, if required, by the two jumpers provided. The 'Reset' jumper allows the PC subsystem to respond to addresses from the PC-9801, and connects the transputer's reset analyse and error signals to those controlled by the PC-9801. The 'Link' jumper connects the link adaptor to one of the transputer's links, and allows the link adaptor to respond to addresses from the PC-9801.



IMS B011

VME board

FEATURES

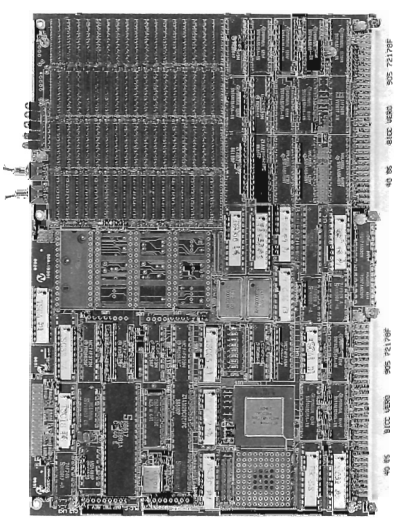
- 2 transputer module (TRAMs) slots
- Double VME card
- IMS T414 or IMS T800, 32 bit transputer
- 2 Mbytes of DRAM
- Acts as bus master/slave to VME bus
- Two RS232 ports
- INMOS board interface

DESCRIPTION

The IMS B011 board is suitable for applications in the system level market, which can perform all communications between a system bus and an array of transputers.

The user has the option of one or more transputers on-board and connections to more external evaluation boards. The expansion connectors on the IMS B011 are compatible with those on other INMOS boards, and with the INMOS module Links Interface format.

The IMS B011 is suited as a main system processor, a specialised accelerator within existing systems, and as a transputer development tool running under UNIX.



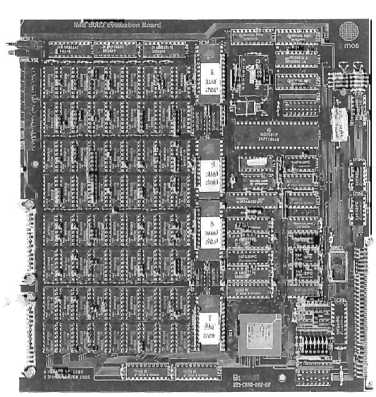
BOARDS

IMS B002

FEATURES

- 32 bit transputer
- 2 Mbyte dynamic RAM with parity
- 128 Kbytes of ROM
- Bootstrap Loader
- Buffered INMOS serial links
- Compatible board family
- Two RS232 ports
- Double Extended Eurocard

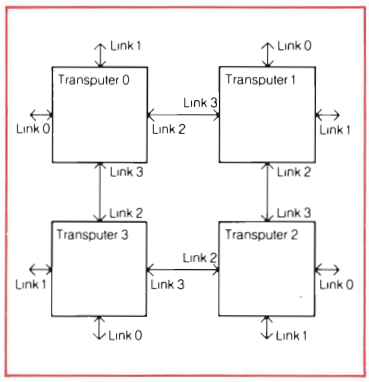
The INMOS B002 enables users to demonstrate larger applications by making available 2 Mbytes of DRAM to the processor. The two RS232 ports allow users to download programs from a remote development station such as the VAX.



IMS B003

FEATURES

- 4 IMS T414, 32 bit transputers
- 256 Kbytes of DRAM per transputer
- INMOS serial links
- Up to 40 MIPS processing capability
- Double Extended Eurocard

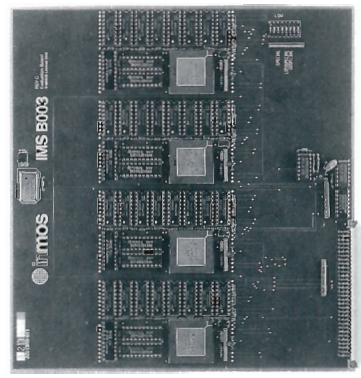


The INMOS B003 board enables users to evaluate and demonstrate the use of multiple transputers.

The four 32 bit transputers on this evaluation board make it a very powerful processing tool capable of up to 40 MIPS. Each transputer has its own 256 Kbytes dynamic RAM.

The links provided with the evaluation board enable the user to extend the array of transputers easily by connecting other boards, using the cables provided.

The configuration of the four transputers on the board is shown in the diagram.



IMS B004

IBM PC add-in board

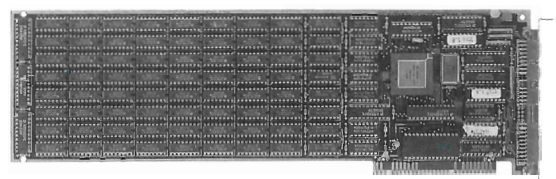
FEATURES

- 32 bit transputer
- 2 Mbyte dynamic RAM with parity
- INMOS link adaptor
- IBM PC I/O channel interface
- Buffered INMOS serial links
- Compatible board family
- Board ready for installation in an IBM PC XT or AT system unit expansion slot

The INMOS B004 IBM PC add-in board enables users to demonstrate the use of transputers. Containing a 32 bit transputer, the board provides a powerful upgrade to the IBM PC XT or AT. The board is one of a family of compatible evaluation boards.

The INMOS transputer development system actually runs on the transputer in the 2 Mbytes of RAM, offering an extremely fast and efficient compilation.

The IBM PC I/O channel is interfaced to an INMOS link by the on-board IMS C002 link adaptor, and logic is provided for the transputer's external reset control and monitoring. Simple external connections complete the communication and control route between the IBM PC and the transputer system.



IMS B005

FEATURES

- IMS M212 transputer, with two standard links and 64 Kbyte of static RAM
- SA400/ST506 standard disc drive interface with buffering
- 20 Mbyte 3.5 inch Winchester disc drive
- 1 Mbyte 3.5 inch floppy disc drive
- Double Extended Eurocard

DESCRIPTION

The IMS B005 board allows the user to evaluate and demonstrate the use of the M212 disc controller transputer.

The IMS M212 is able to control up to four disc drives via the industry standard SA400/ST506 interfaces. Two drives are present on the IMS B005 and provision has been made for connecting other drives if the user so desires, or to change either of the drives on the board (for instance use two Winchester drives).

The external memory interface can address 64K of memory space; as supplied this memory is static RAM (two 32K x 8 devices), but it is possible to replace one or both with EPROM if required. The external memory interface may be switch programmed for different speeds.

IMS B007

transputer graphics board

FEATURES

- IMS T414 – 32 bit transputer
- IMS G170 colour palette
- 512 Kbytes RAM
- 512 Kbytes dual ported video RAM
- 262,144 colours
- Buffered INMOS serial links
- Double Extended Eurocard
- Graphics software primitives
- RGB output

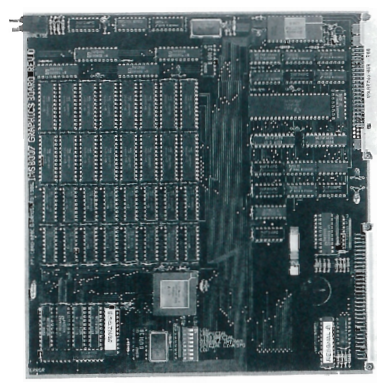
DESCRIPTION

The IMS B007 graphics board enables users to evaluate and demonstrate the use of transputers for graphics.

The dual ported video RAM allows display refresh to occur whilst still allowing the processor full read and write access to the display memory.

The display consists of 512 by 512 byte wide pixels, and is controlled by a memory mapped CRT controller. It is suitable for any colour monitor with line scan frequencies of 20 to 50 kHz.

Occam support for the B007 is provided by low level primitives for line and polygon drawing and alphanumeric text generation with scaling.



IMS B211

transputer board rack

FEATURES

- Slots for 10 double extended Eurocards
- Configurable backplane with removable card assembly.
- Built in power supply unit
- Built in forced air cooling
- Meets U.S. FCC standards
- 19 inch rack mountable
- Overall dimensions 425mm x 330mm x 450mm

DESCRIPTION

The IMS B211 is a small modular cabinet that has been designed to accommodate up to 10 INMOS Eurocard format transputer boards. Ample power supply and air cooling is provided. The backwiring is suitable for connecting directly to standard evaluation board connectors. The back panel is hinged to allow easy access and has two male and two female RS232 connectors for connection to a terminal or a development system. The front panel is also hinged.

The requirements for current and future boards from INMOS have been accommodated in the IMS B211. The power supply unit can deliver 12 volts or 5 volts and there are four BNC plugs at the rear.

The IMS B211 provides a simple rack system for a number of transputers on boards. For portability there are carrying handles recessed into the sides.

When populated with 10 x IMS B003 boards, the IMS B211 provides a low cost 400 MIPS supercomputer with 10 Mbytes of store.

IMS B213

INMOS transputer system (ITEM series)

FEATURES

- IMS B211, 10 slot card cage
- 10 x IMS B003 totalling 40 transputers
- 256K DRAM per transputer (10 Mbytes)
- Transputer development system included
- Built in power supply
- Built in forced air cooling
- Meets U.S. FCC standards

ITEM 300

- 40 x IMS T414B-G15
- 300 MIPs

ITEM 400

- 40 x IMS T414B-G20
- 400 MIPs

ITEM 4000

- 40 x IMS T800-G20
- Sustains 60 MFLOPS

DESCRIPTION

The initial ITEM configuration contains 10 INMOS evaluation cards (IMS B003) each containing 4 transputers with 256 K bytes DRAM each. The total system memory is 10 Mbytes.

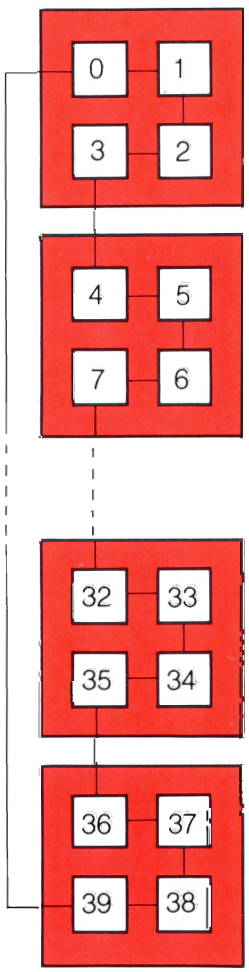
The system comes complete with the Transputer Development System for the IBM PC, which itself contains an IMST414 and 2 Mbytes of DRAM.

The user can thus write and debug his occam program on a transputer, using the IBM PC as his terminal. The compiled code can then be downloaded over the INMOS links at 10 Mbit/sec into the array of 40 transputers. This allows the performance of concurrent systems to be evaluated in real-time.

The configuration of transputers on a single board is a simple square with 8 free links brought to the edge connector. Arbitrary configurations of the system can be achieved by using the supplied link cables to connect between the boards. The configuration can be further extended by connecting into additional ITEMs for even larger systems.

In addition to the IBM PC XT/AT as system host, the VAX 11/7xx (including Microvax) range of computers may also be used. This requires the IMS D600 or IMS D605 VAX/VMS Transputer Development Software and a transputer board with an RS232 interface capability (e.g. IMS B002-2). These are available as additional products from INMOS.

The design allows other boards from the INMOS range to replace the supplied boards.



40 node ring – one of many configurations for the ITEM 400

DEVELOPMENT TOOLS

The following products have been designed to provide the necessary tools to make evaluation and development of transputer systems inexpensive and straightforward.

All products come with documentation to load and run the relevant software. For each item INMOS customers receive their own personal registration number, which they subsequently quote if requiring support from their local INMOS representative office. This ensures that a personal service can be provided by the INMOS field support teams.

Products available for transputer development fall into 3 major categories.

The Transputer Development System (T.D.S.)

FEATURES

- Fully integrated editor and development tools
- Transputer add in board
- Compiles and loads occam II for:
  - evaluation boards
  - other transputer networks
- All application development at occam source level
- Hierarchical program structure with separate compilation
- Source level network debugger
- Allows the inclusion of in-line transputer assembly code

Stand alone tool sets

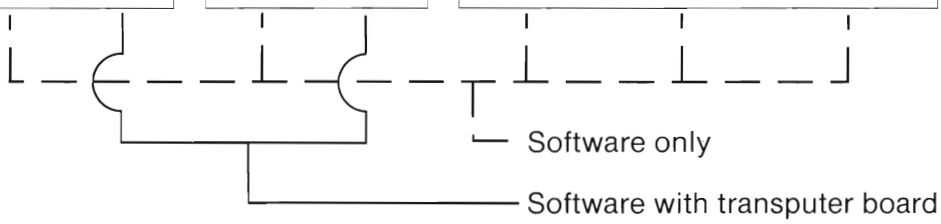
- Commands invoked from host operating system level prompt
- Supports mixed occam and scientific language compilations
- Permits multi-user access
- Simplifies version control management
- Allows the inclusion of in-line transputer assembly code

Scientific Languages

- C, PASCAL and FORTRAN compilers meeting industry standards are available for transputers.

Inmos Development Tools — Nomenclature

	T.D.S.		Toolsets		Scientific languages		
					C	PASCAL	FORTRAN
SUN	—	—	D505*	D525*	D511*	D512*	D513*
VAX	D600	—	D605*	—	D611*	D612*	D613*
IBM PC	D700	D701	D705	D725	D711	D712	D713
NEC PC	D700	D801	D705	D825	D711	D712	D713



* *Advanced information.*

Please contact Inmos representative for availability.

DEVELOPMENT TOOLS

TDS (TRANSPUTER DEVELOPMENT SYSTEM)

The transputer development system provides a complete programming environment for the generation of reliable, well structured and efficient programs. The structured editing facilities provided by the fully integrated user interface mirror the hierarchical structure of the transputer application under development. The integrated system provides a secure mechanism for separate compilation and the use of separate files, allowing fast editing and recompilation for minor program changes.

Major system utilities are menu selectable. The individual tools are invoked by function keys, and the integrated editing system allows the application of any utilities to any part of the program under design.

The benefits of the transputer development system combine to provide excellent design productivity. They greatly increase confidence in the timely and accurate implementation of highly concurrent and real time systems.

The hierarchical structure of the application under design can be captured in occam, allowing an interconnected set of processes to be regarded from the outside as a single process. In order to assist the designer in the creation of a program, INMOS has based the programming environment on the same notion of *hierarchical structure.*

The software component of the TDS is available separately.

User Interface

The user interface is based on a full screen structured editor, exploiting the concept of folding. Folding provides a very effective method of navigating around and viewing selected parts of a large design, and yet operates within the constraints of an ordinary text VDU. The programmer's dependence on hard copy listings is much reduced, and the system is able to exploit the structure to provide facilities such as compilation control (exactly those parts of a program which have been changed are recompiled), navigation to *the part of the program where an* error (compile time or runtime) was detected, as well as the editing convenience of being able to reorganise the major structure of a program simply and easily.

IMS D701

DESCRIPTION

The IMS D701 transputer development system runs on a transputer board using a file server which executes on the NEC/IBM PC and provides access to the PC's resources.

The PC communicates with the transputer add-in board via the link adaptor on the board.

The IMS D701 is available in two hardware configurations. The first with an IMS B004* single transputer board incorporating 2 Mbyte DRAM. The second is with an IMS B008*, IMS B401-3 and an IMS B404-3. The latter is a multi-transputer development environment which may be expanded with further modules, and can also be used as a target for application software.

A symbolic transputer network debugger is incorporated in the IMS D701. This allows a post-mortem examination of a single transputer or a network of transputers connected via links to the host transputer. Also provided is a mechanism to interrogate internal register status and memory contents of any transputer on a network by reference to source code lines and variables. Users may also backtrack through code calls by a single function key depression.

*NEC PC-9801 uses IMS B010

CONTENTS

- Occam compiler
- Linker
- Network configurer
- DOS file server
- Integrated editor
- Floating point I/O library
- File conversion utilities
- Source level symbolic debugger
- Tutorial and sample programs
- Memory configuration program
- EPROM support

DOCUMENTATION

- System installation manual
- TDS manual
- Tutorial introduction to occam
- Occam reference manual

IMS D701-4 : IMS B004
IMS D701-5 : IMS B008, IMS B401-3, IMS B404-3

Software on 5¼" floppy discs

IMS D600
VAX/VMS

DESCRIPTION

The transputer development system runs on any VAX computer (including MicroVAX) under versions 3 and 4 of VMS. It provides all the facilities of the occam programming system, and is entered by a simple VMS command.

CONTENTS

- Licence terms and conditions permits internal use for any purpose
- Integrated occam editor/compiler
- Occam kernel (in VAX/VMS object format)
- Floating point and I/O library
- Utilities for file conversion and copying
- Tutorial file
- VMS installation commands
- Software supplied on 1600 bpi magnetic tape

Terminal capability

- VT220, VT100, TVI-920 and Y-50
- Table driven terminal driver
- Terminal driver source

DOCUMENTATION

- System installation manual
- Transputer development system manual
- Occam programming manual
- VAX implementation manual
- Transputer implementation manual.

OCCAM
Stand Alone Tool Set

DESCRIPTION

The occam toolset is designed to enable users to compile and run programs on transputers and other hosts. These programs may be written purely in occam, or written in other languages, called from within an occam program. The tools all work on standard host format files. Thus users are able to use their own favourite editors and version control mechanisms.

Programs may be written with any editor which produces ASCII text files. The compiler supports a mechanism which allows parts of a program to be compiled separately from other parts of the same program (the parts are combined by the linker prior to running). Occam progams may use libraries. In addition non-occam programs may be called (run) from within an occam harness.

All components of a program must be linked together to produce configurable (or bootable) code. Bootable code is compiled source which contains additional binary information. This additional information enables it to self load onto a transputer or transputer network, and commence running. This code is added by the linker in the case of a single processor, or by the configurer in the case of a multiprocessor network.

The software component of the Stand Alone Toolset is available separately.

LOADING ONTO TRANSPUTER

Code is loaded on to a transputer board connected to the host for single processor applications, or via a transputer board for multiprocessor networks. This is achieved by the file server supplied.

SIMULATOR

An IMS T414 transputer simulator is supplied with all occam toolsets that run on non-transputer hosts. This allows the user to fully debug his occam software without the need for target hardware.

N.B. Software to run on one or more IMS T414 or IMS T800 processors may be tested in this way.

IMS D505/D525
SUN 3 Toolset

DESCRIPTION

The IMS D525 is a transputer development tool that runs on a SUN 3 workstation. Tools are provided to download code to transputer networks.

IMS D605
VAX Toolset

DESCRIPTION

The IMS D605 is a software product allowing VAX customers to develop occam and scientific languages for the transputer in a multi-user environment.

CONTENTS

- Transputer simulator
- Network configurer
- Floating point and I/O library
- VMS file server
- Compiler and linker library
- File dependancy utility
- Software supplied on 1600 bpi
- VAX format magnetic tape

DOCUMENTATION

- System installation manual
- Tutorial introduction to occam
- Occam reference manual
- User manual

IMS D705/D725
NEC/IBM PC Toolset

DESCRIPTION

The IMS D725 transputer development system runs on a transputer board using a file server which runs on the NEC/IBM PC, and provides access to the PC's resources.

The PC communicates with the transputer add-in board via the link adaptor on the board.

The hardware configuration of the IMS D725 consists of an IMS B008*, an IMS B401-3 and IMS B404-3. This provides a multi-transputer development environment which may be extended with further modules and can also be used as a target for application software.

*NEC PC-9801 uses IMS B010

CONTENTS

- Occam compiler
- Linker
- Network configurer
- DOS file server
- Floating point I/O library
- File dependency utility
- Tutorial and sample programs

DOCUMENTATION

- System installation manual
- Tutorial introduction to occam
- Occam reference manual
- User manual

IMS D725: IMS B008, IMS B401-3, IMS B404-3

Software on 5¼" floppy discs

SCIENTIFIC LANGUAGES

In addition to occam, transputers can be programmed in C, PASCAL and FORTRAN.

These compilers can be used to build programs running on a single IMS T414 or IMS T800 transputer, or used in conjunction with the occam 2 toolset (e.g. IMS D705) to program networks of transputers.

A separately compiled program written in one of these languages executes as a single process with occam channel inputs and outputs. The channels may be accessed indirectly by calls to the standard language input/output system which use a protocol to communicate with the server on the host. Direct access to channels is provided by language extensions or libraries (as appropriate) giving an occam-like input/output system.

Using the occam 2 toolset several processes may be executed on a single transputer or on a network of transputers by linking them into an occam harness. The processes may be written in different languages. The harness describes the channel connections between each process and how the processes are mapped onto processors. The configurer is used to collate the code and appropriate load modules into a form which the server can load onto the transputer network. The linking and configuration mechanisms are independent of the source language.

Each scientific language product includes a compiler, linker and host server; the linker is used to combine separately compiled units and libraries into an executable program, or into a form equivalent to an occam process with input and output channels. The linker will also allow separately compiled program units to be prelinked into user libraries. The host server is used to load programs onto the transputer and to support access to the host operating system.

IMS D711

The C compiler

The general purpose high level language C was invented by Kernighan and Ritchie at Bell Telephone Laboratories in 1978, since when it has found applications in many areas, especially operating system development and systems programming. The C compiler supplied by INMOS supports the full set of C operators and standard programming constructs, as well as all data structures. It also supports structure assignment, functions taking structure arguments and returning structure results, and enumerated types. A portable I/O package is provided. Identifiers can have up to 31 significant characters, and can contain the "$" character. Macros and conditional compilation are also supported.

The compiler also provides explicit error and warning messages.

No internationally accepted standard as yet exists for C. However, the C compiler is aligned to the provisions of the anticipated ANSI X3J11 standard.

IMS D712

The Pascal compiler

Originally designed by N. Wirth for teaching purposes, Pascal has now found application in many areas including systems programming. Over the years since it was devised a great variety of Pascal dialects have evolved, many of which are mutually incompatible, and this has led in recent years to the development of international standards for the language. The Pascal compiler supplied by INMOS is one of the first to be written to these standards, namely ISO 7185 (BSI 6129:1982 Level 1).

Because the standard defines a language with limited application, the Pascal compiler provided by INMOS includes optional extensions which when invoked extend its scope in key areas. For example, modules are introduced to permit the development of large applications in a structured and partitioned manner.

Extensions included are:

- Modules for separate compilation
- Import and export of procedures, functions and variables
- Source file inclusion
- The use of "$" and "_" characters in identifiers
- Constants specified to any base between 2 and 36
- Bit vector operators (and, or, shift, etc)
- The use of "OTHERWISE" in CASE statements
- Non-printable characters in strings
- Universal parameter type
- An address function

IMS D713

The FORTRAN compiler

FORTRAN has been widely used for many years for scientific programming. The FORTRAN compiler supplied by INMOS implements the version designated as FORTRAN-77, defined in the ANSI standard X3.9-1978 (ISO 1539-1980). In addition, a number of extensions are provided to assist the transfer of programs developed using other compilation systems.

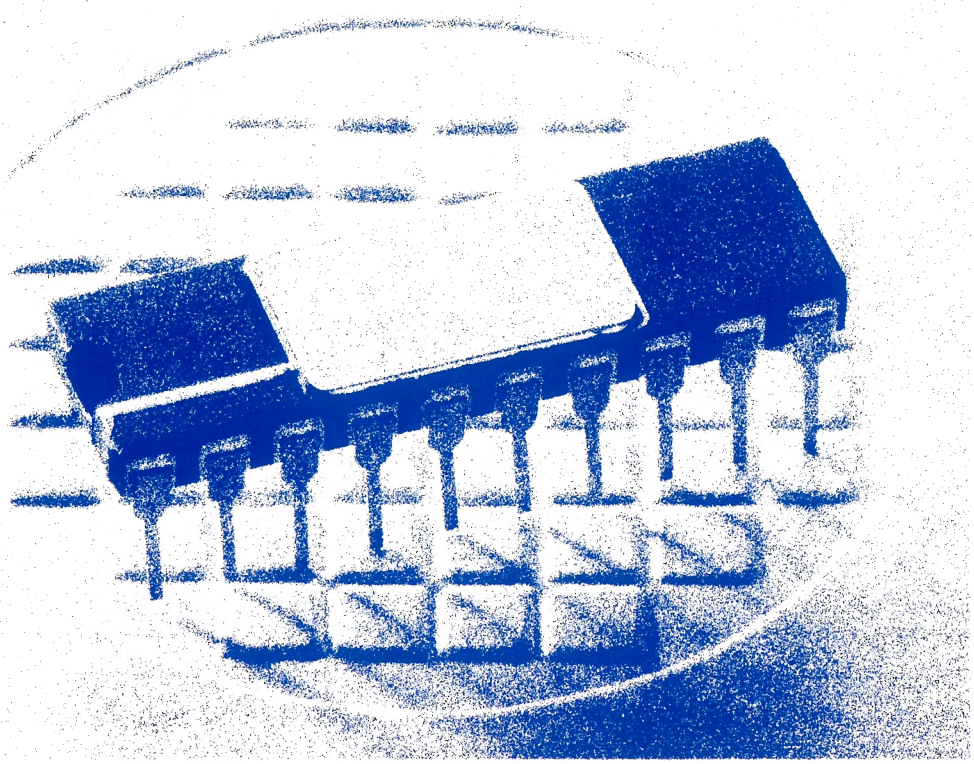
Extensions included are:

- Lower case in program text
- Up to 32 characters in identifiers
- DOUBLE COMPLEX
- IMPLICIT NONE
- DO WHILE construct
- Bit handling intrinsic functions
- Data initialisation in type statements
- Extended range of DO loops

Compile time options for warnings and error reports are supported. A number of run-time checks can optionally be invoked including checks for:

- Use of assignment variables
- Array bounds
- Invalid character substring specifiers

For information on Scientific Compilers to run on SUN 3 and VAX systems please contact your INMOS representative.



FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 1.6 Micron Design Rules
- 4K x 1 Bit Organization
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 18-Pin, 300-mil DIP
- Single +5V±10% Operation
- Power Down Function

DESCRIPTION

The INMOS IMS1203 is a high performance 4K x 1 CMOS static RAM. The IMS1203 allows speed enhancements to existing 4K x 1 applications with the additional benefit of reduced power consumption.

The IMS1203 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1203 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

IMS1203

CMOS High Performance 4K x 1 Static RAM

FEATURES

- 20, 25, 35 and 45 nsec Address Access Times
- 20, 25, 35 and 45 nsec Chip Enable Access Times

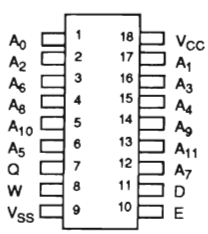
MIL-STD-883C IMS1203M

CMOS High Performance 4K x 1 Static RAM

FEATURES

- Specifications guaranteed over full military temperature range
- 25, 35 and 45 nsec Address Access Times
- 25, 35 and 45 nsec Chip Enable Access Times

PIN CONFIGURATION

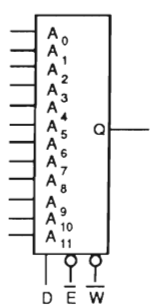


DIP

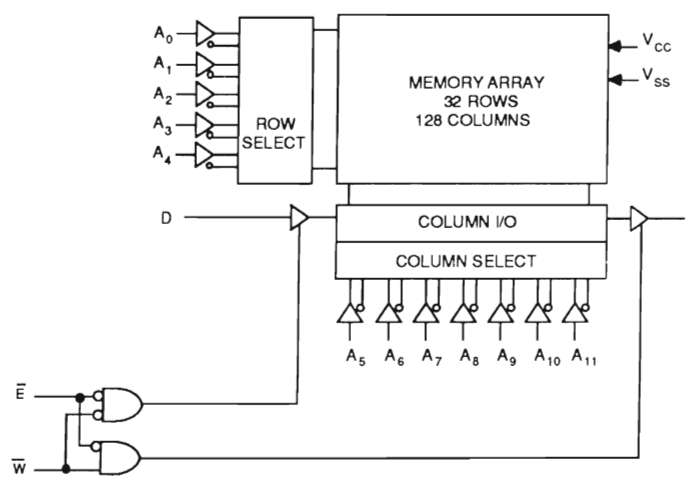
PIN NAMES

$A_0 - A_{11}$	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{ss}	GROUND
D	DATA IN		
$\overline{E}$	CHIP ENABLE		
Q	DATA OUTPUT		

LOGIC SYMBOL



BLOCK DIAGRAM



FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 1.6 Micron Design Rules
- 1K x 4 Bit Organization
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Three-state Output
- 18-Pin, 300-mil DIP
- Single +5V±10% Operation
- Power Down Function

DESCRIPTION

The INMOS IMS1223 is a high performance 1K x 4 CMOS static RAM. The IMS1223 allows speed enhancements to existing 1K x 4 applications with the additional benefit of reduced power consumption.

The IMS1223 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1223 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

IMS1223

CMOS High Performance 1K x 4 Static RAM

FEATURES

- 20, 25, 35 and 45 nsec Address Access Times
- 20, 25, 35 and 45 nsec Chip Enable Access Times

MIL-STD-883C

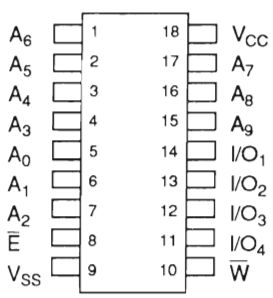
IMS1223M

CMOS High Performance 1K x 4 Static RAM

FEATURES

- Specifications guaranteed over full military temperature range
- 25, 35 and 45 nsec Address Access Times
- 25, 35 and 45 nsec Chip Enable Access Times

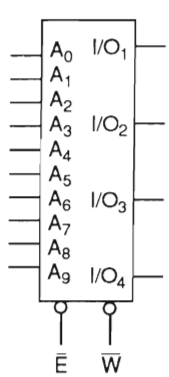
PIN CONFIGURATION



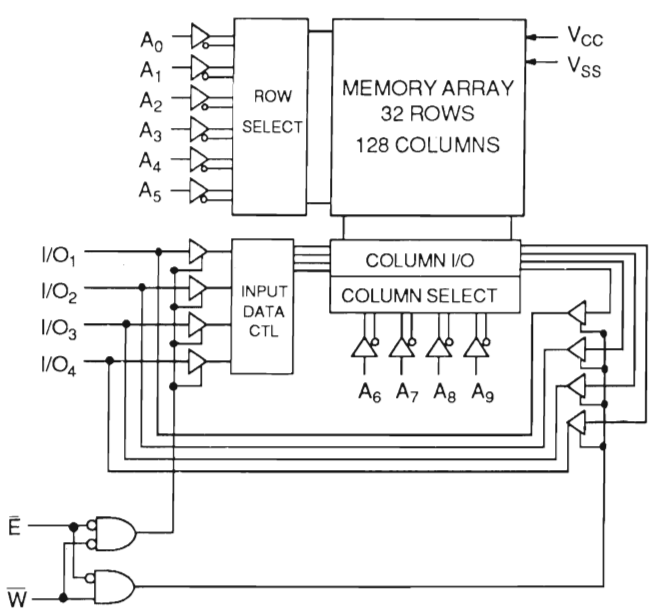
PIN NAMES

A_0 - A_9	ADDRESS INPUTS	V_{CC}	POWER
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O_1-I/O_4	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		

LOGIC SYMBOL



BLOCK DIAGRAM



FEATURES

- 16K x 1 Bit Organization
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 20-Pin, 300-mil DIP and 20-Pin LCC
- Single +5V±10% Operation
- Power Down Function
- Pin Compatible with IMS1400

DESCRIPTION

The INMOS IMS1403 is a high performance 16K x 1 CMOS static RAM. The IMS1403 allows speed enhancements to existing 16K x 1 applications with the additional benefit of reduced power consumption. The IMS1403 is a low cost alternative to 4K x 4 and 16K x 4 designs, allowing even higher system bandwidth due to the separate I/O lines.

The IMS1403 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1403 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

IMS1403

CMOS High Performance 16K x 1 Static RAM

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 1.6 Micron Design Rules
- 25, 35, 45 and 55 nsec Address Access Times
- 25, 35, 45 and 55 nsec Chip Enable Access Times

MIL-STD-883C

IMS1403M/LM

CMOS High Performance 16K x 1 Static RAM

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (-55°C to +125°C)
- 35, 45 and 55 nsec Address Access Times
- 35, 45 and 55 nsec Chip Enable Access Times
- Battery Backup Operation — 2V Data retention (L version only)

MIL-STD-883C

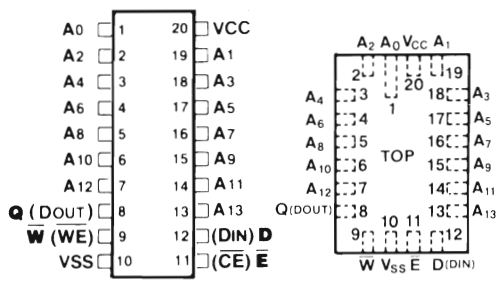
IMS1400M

NMOS High Performance 16K x 1 Static RAM

FEATURES

- INMOS High Speed NMOS
- Specifications guaranteed over full military temperature range (-55°C to +125°C)
- MIL-STD-883C Processing
- 45, 55 and 70 nsec Chip Enable Access Times
- Maximum Active Power 660mW
- Maximum Standby Power 165mW
- 20-pin, 300 mil DIP and 20-pin chip carrier

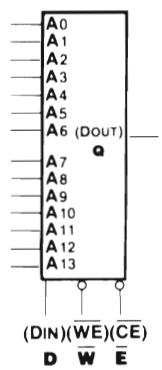
PIN CONFIGURATION



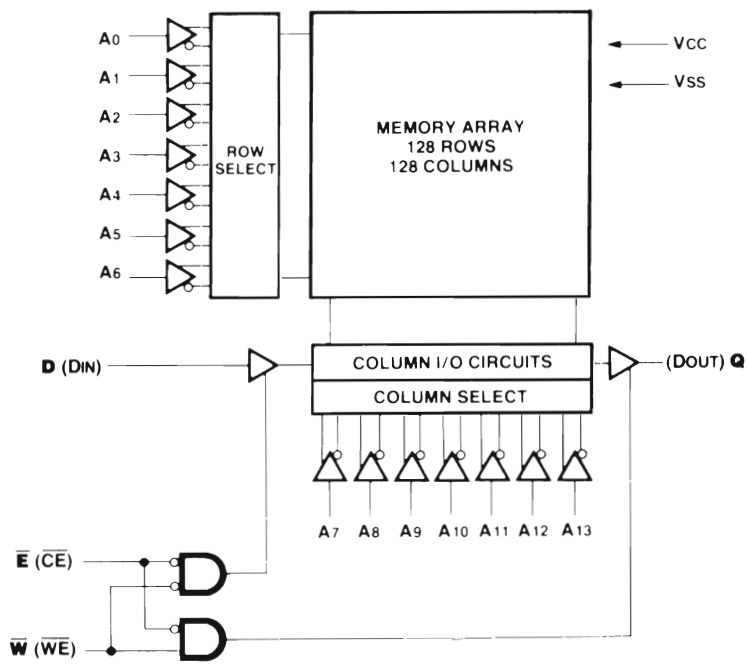
PIN NAMES

A0 - A13	ADDRESS INPUTS	VCC POWER(+5V)
W (WE)	WRITE ENABLE	VSS GROUND
E (CE)	CHIP ENABLE	
D (DIN)	DATA INPUT	
Q (DOUT)	DATA OUTPUT	

LOGIC SYMBOL



BLOCK DIAGRAM



FEATURES

- 4K x 4 Bit Organization
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V±10% Operation
- Power Down Function
- 20-Pin, 300-mil DIP and 20-Pin LCC
- Pin Compatible with IMS1420

DESCRIPTION

The IMS1423 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1423 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power to 100mW. By using CMOS levels, the standby power may be reduced to an even lower 33mW.

IMS1423

CMOS High Performance 4K x 4 Static RAM

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 2 Micron Design Rules
- 25, 35, 45 and 55 nsec Address Access Times
- 25, 35, 45 and 55 nsec Chip Enable Access Times
- 580mW Maximum Power Dissipation
- 100mW Maximum Standby Power
- 33mW Maximum Standby Power (Stable CMOS levels)

MIL-STD-883C

IMS1423M

CMOS High Performance 4K x 4 Static RAM

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 2 Micron Design Rules
- Specifications guaranteed over full military temperature range (–55°C to +125°C)
- MIL-STD-883C Processing
- 35, 45 and 55 nsec Address Access Times
- 35, 45 and 55 nsec Chip Enable Access Times
- Intended for Military temperature applications that demand superior performance and reliability

MIL-STD-883C

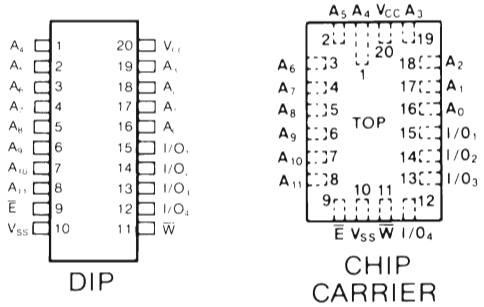
IMS1420M

NMOS High Performance 4K x 4 Static RAM

FEATURES

- INMOS High Speed NMOS
- Specifications guaranteed over full military temperature range (–55°C to +125°C)
- MIL-STD-883C Processing
- 55 and 70 ns Address Access
- 55 and 70nsec Chip Enable Access
- 660mW Maximum Power Dissipation
- Power Down Function
- 165mW Maximum Standby Power
- 20-pin, 300-mil DIP and 20-pin chip carrier.

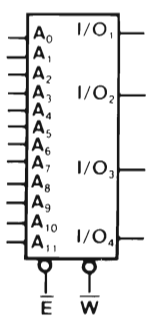
PIN CONFIGURATION



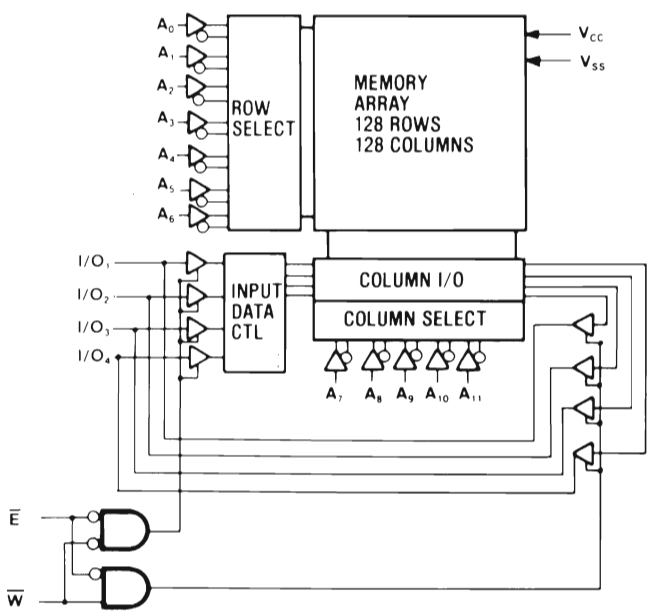
PIN NAMES

A_0-A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
$\overline{E}$	CHIP ENABLE		
I/O	DATA IN/OUT		

LOGIC SYMBOL



BLOCK DIAGRAM



FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 1.6 Micron Design Rules
- 2K x 8 Bit Organization
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V±10% Operation
- 24-Pin, 300-mil DIP
- Fast Write Cycle when Outputs Disabled

DESCRIPTION

The IMS1433 is a high speed CMOS 2K x 8 Static RAM having access times of 35 and 45 ns.

The IMS1433 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1433 provides a Chip Enable function ($\overline{E}$) to place the circuit into a reduced power standby mode.

IMS1433

CMOS High Performance 2K x 8 Static RAM

FEATURES

- 35 and 45 nsec Address Access Times
- 35 and 45 nsec Chip Enable Access Times

MIL-STD-883C

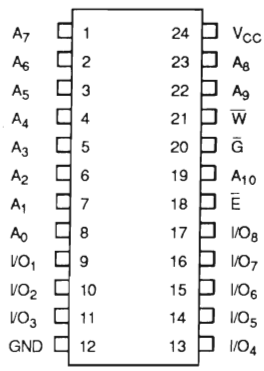
IMS1433M

CMOS High Performance 2K x 8 Static RAM

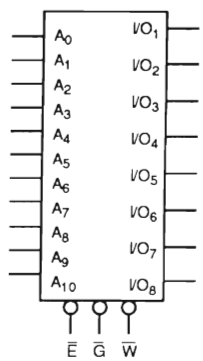
FEATURES

- Specifications guaranteed over full military temperature range
- 45 and 55 nsec Address Access Times
- 45 and 55 nsec Chip Enable Access Times

PIN CONFIGURATION



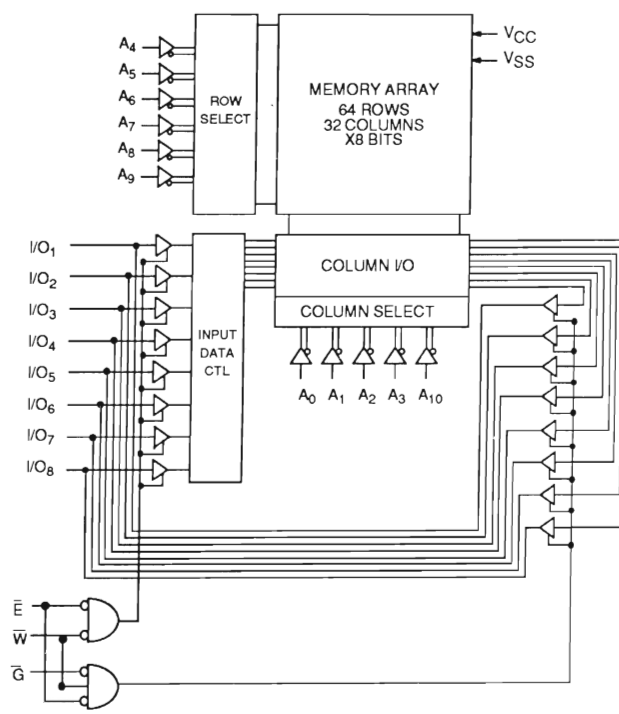
LOGIC SYMBOL



PIN NAMES

A_0-A_{10}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O_1-I/O_8	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

BLOCK DIAGRAM



FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 2 Micron Design Rules
- 64K x 1 Bit Organization
- Fully TTL Compatible
- Separate Data Input & Output
- Three-state Output
- 22-Pin, 300-mil DIP and 22-Pin LCC
- Single +5V±10% Operation
- Power Down Function

DESCRIPTION

The IMS1600 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. Additionally, the IMS1600 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode, thus reducing power. By using stable CMOS levels, the standby power may be reduced to an even lower level.

IMS1600

CMOS High Performance 64K x 1 Static RAM

FEATURES

- 35, 45 and 55 nsec Address Access Times
- 35, 45 and 55 nsec Chip Enable Access Times

IMS1601L

CMOS Battery Backed 64K x 1 Static RAM

FEATURES

- 45 and 55 nsec Address Access Times
- 45 and 55 nsec Chip Enable Access Times
- Data Retention to 2 volts

MIL-STD-883C

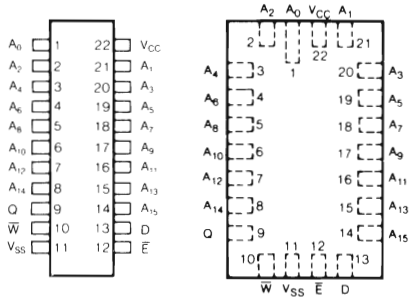
IMS1600M/01LM

CMOS 64K x 1 Static RAM

FEATURES

- 45, 55 and 70 nsec Address Access Times
- 45, 55 and 70 nsec Chip Enable Access Times
- Data Retention to 2 volts (1601LM version only)
- Processed to the requirements of MIL-STD-883 Rev. C
- Specifications guaranteed to operate over the full temperature range, -55°C to +125°C

PIN CONFIGURATION

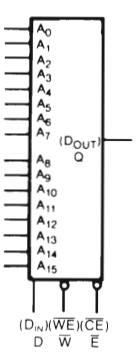


DIP CHIP CARRIER

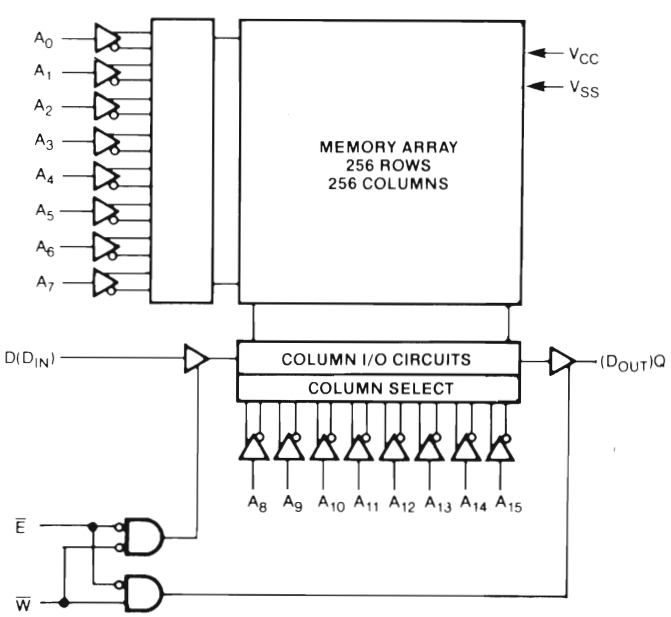
PIN NAMES

A_0 - A_{15} ADDRESS INPUTS	V_{CC} POWER (+5V)
$\overline{W}$ WRITE ENABLE	
$\overline{E}$ CHIP ENABLE	
D DATA INPUT	
Q DATA OUTPUT	

LOGIC SYMBOL



BLOCK DIAGRAM



FEATURES

- INMOS Very High Speed CMOS
- 16K x 4 Bit Organization
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V±10% Operation
- Power Down Function
- 22-Pin, 300-mil DIP and 22-Pin LCC

DESCRIPTION

The IMS1620 is a high speed CMOS 16K x 4 Static RAM having access times of 35, 45 and 55ns. These characteristics are made possible by the combination of innovative circuit design and INMOS' proprietary CMOS technology.

The IMS1620 features fully static operation requiring no external clocks or timing strobes. The IMS1620 is optimized for high speed system operation as well as providing increased reliability due to the CMOS process.

The low power version (IMS1620L) offers a battery backup data retention capability operating from a 2 volt battery.

IMS1620

CMOS High Performance 16K x 4 Static RAM

FEATURES

- Advanced Process – 1.6 Micron Design Rules
- 35, 45 and 55 nsec Address Access Times
- 35, 45 and 55 nsec Chip Enable Access Times

IMS1620A

CMOS High Performance 16K x 4 Static RAM

FEATURES

- Advanced Process – 1.2 Micron Design Rules
- 25 and 35 nsec Address Access Times
- 25 and 35 nsec Chip Enable Access Times

MIL-STD-883C

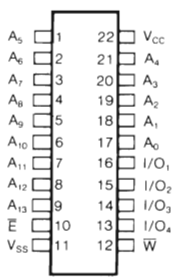
IMS1620M/LM

CMOS High Performance 16K x 4 Static RAM

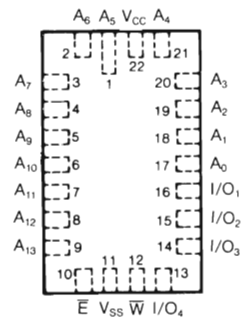
FEATURES

- Advanced Process – 1.6 Micron Design Rules
- Specifications guaranteed over full military temperature range (–55°C to + 125°C)
- MIL-STD-883C Processing
- 45, 55 and 70 nsec Address Access Times
- 45, 55 and 70 nsec Chip Enable Access Times
- Battery Backup Operation — 2V data retention (L version only)

PIN CONFIGURATION



DIP

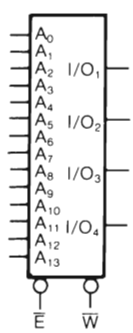


CHIP CARRIER

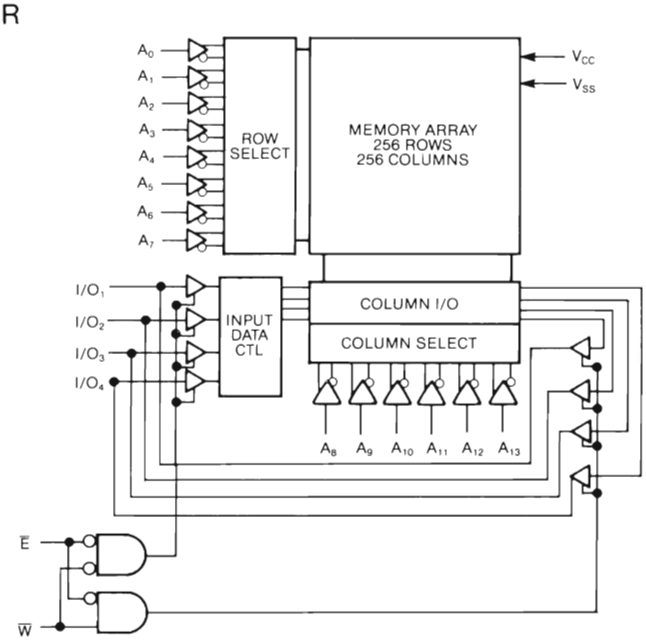
PIN NAMES

A_0-A_{13}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		

LOGIC SYMBOL



BLOCK DIAGRAM



FEATURES

- INMOS Very High Speed CMOS
- 16K x 4 Bit Organization (with Output Enable)
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V±10% Operation
- Power Down Function
- 24-Pin, 300-mil DIP (JEDEC Standard)
- 28-Pin LCC (JEDEC Standard)
- Output Enable to Control Bus Contention

DESCRIPTION

The IMS1624 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1624 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode. The IMS1624 also includes an Output Enable ($\overline{G}$) to eliminate bus contention. The IMS1624 is functionally equivalent to the IMS1620, with the addition of the $\overline{G}$ control function.

The low power version (IMS1624L) offers a battery backup data retention capability operating from a 2 volt battery.

IMS1624

CMOS High Performance 16K x 4 Static RAM

FEATURES

- Advanced Process – 1.6 Micron Design Rules
- 35, 45 and 55 nsec Address Access Times
- 35, 45 and 55 nsec Chip Enable Access Times
- Battery Backup Operation – 2V data retention (L version only)

IMS1624A

CMOS High Performance 16K x 4 Static RAM

FEATURES

- Advanced Process – 1.2 Micron Design Rules
- 25 and 35 nsec Address Access Times
- 25 and 35 nsec Chip Enable Access Times

MIL-STD-883C

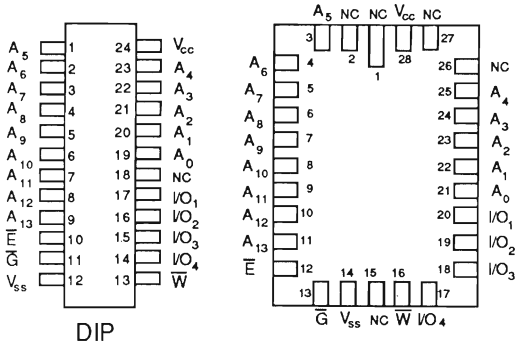
IMS1624M/LM

CMOS High Performance 16K x 4 Static RAM

FEATURES

- Advanced Process – 1.6 Micron Design Rules
- 45, 55 and 70 nsec Address Access Times
- 45, 55 and 70 nsec Chip Enable Access Times
- Battery Backup Operation — 2V data retention (L version only)
- Specifications guaranteed over full military temperature range

PIN CONFIGURATION



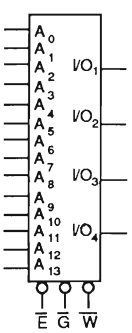
DIP

CHIP CARRIER

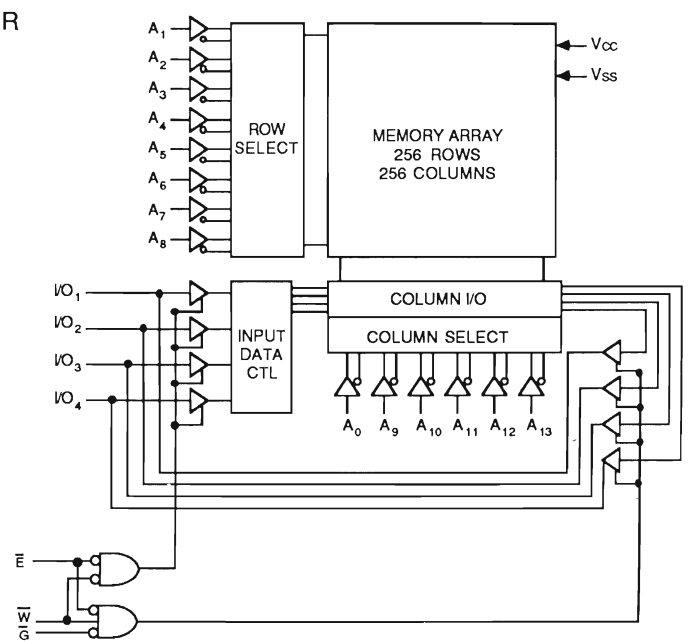
PIN NAMES

A_0–A_{13}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O	DATA IN/OUT		
$\overline{E}$	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

LOGIC SYMBOL



BLOCK DIAGRAM



16K x 4 – SRAM

FEATURES

- INMOS Very High Speed CMOS
- Advanced Process – 1.6 Micron Design Rules
- 8K x 8 Bit Organization
- Fully TTL Compatible
- Common Data Inputs & Outputs
- Single +5V±10% Operation
- 28-Pin, 600-mil DIP and 32-Pin LCC
- Fast write cycle when outputs disabled

DESCRIPTION

The IMS1630 features fully static operation requiring no external clocks or timing strobes, and equal address access and cycle times. The IMS1630 provides a Chip Enable ($\overline{E}$) function that can be used to place the device into a low-power standby mode.

IMS1630

CMOS
High Performance
8K x 8 Static RAM

FEATURES

- 45 and 55 nsec Address Access Times
- 45 and 55 nsec Chip Enable Access Times

MIL-STD-883C

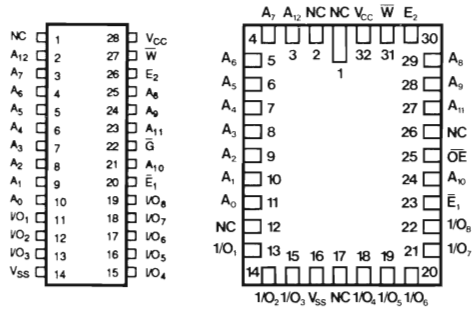
IMS1630M/LM

CMOS
High Performance
8K x 8 Static RAM

FEATURES

- Specifications guaranteed over full military temperature range (−55°C to +125°C)
- 55 and 70 nsec Address Access Times
- 55 and 70 nsec Chip Enable Access Times
- Battery Backup Operation — 2V Data retention (L version only)

PIN CONFIGURATION

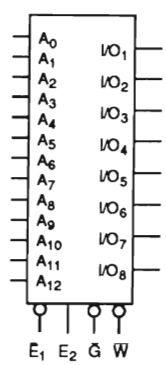


DIP CHIP CARRIER

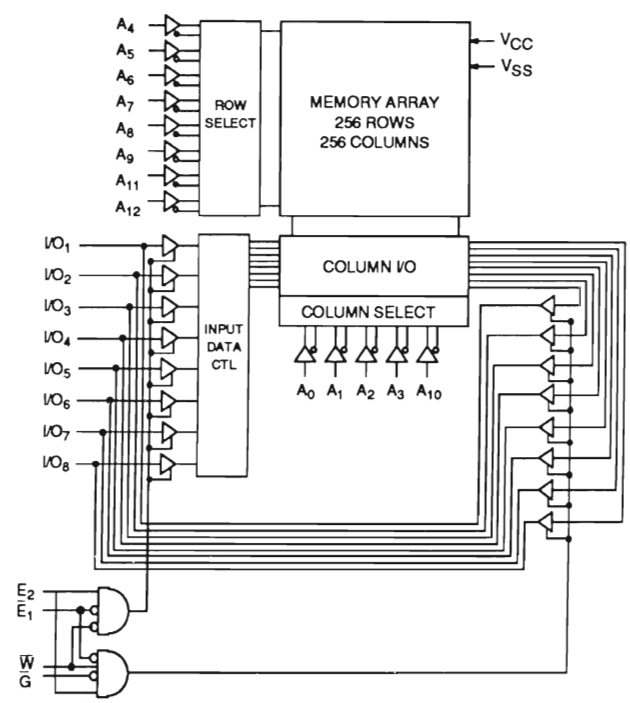
PIN NAMES

A_0-A_{12}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{W}$	WRITE ENABLE	V_{SS}	GROUND
I/O_1-I/O_8	DATA IN/OUT		
$\overline{E}_1$, E_2	CHIP ENABLE		
$\overline{G}$	OUTPUT ENABLE		

LOGIC SYMBOL



BLOCK DIAGRAM



Colour Look Up Table

Organisation	Part Number	Package	Bandwidth (MHz)	Page No.
6 Bit DAC 8 Bit Pixel+Sync	IMS G170	S	35, 50	4
	IMS G175	P	25	
6 Bit DAC 8 Bit Pixel+Readback	IMS G171	S, P	35, 50	5
	IMS G176	S, J, P	40, 50, 65	

Cascadable Signal Processor

Description	Part Number	Package	Clock Rate (MHz)	Page No.
16 Bit, 32 Stage Filter/Correlator	IMS A100	G	21	8
	IMS A100M	G	21	

Transputer Family

Description	Part Number	Package	Processor Clock (MHz)	Page No.
32 bit Transputer + 64 Bit FPU	IMS T800	G	17, 20	14
32 bit Transputer	IMS T414	G, J	15, 20	15
16 bit Transputer	IMS T212	G, J	17, 20	16
16 bit Disk Processor	IMS M212	G, J	15, 20	17
32 Way Link Switch	IMS C004	G		18
Link Adaptor	IMS C011	S,P		19
	IMS C012	P		

Transputer Modules (TRAMs)

Description	Part Number	Format	Page No.
IMS T414/IMS T800 + 32 Kbytes SRAM	IMS B401	TRAM Size 1	23
IMS T212 + 8 Kbytes SRAM	IMS B402	TRAM Size 1	23
IMS T414/IMS T800 + 1 Mbyte DRAM	IMS B403	TRAM Size 4	23
IMS T800 + 2Mbytes DRAM +128 Kbytes SRAM	IMS B404	TRAM Size 2	23
IMS T800 + 8 Mbytes DRAM	IMS B405	TRAM Size 8	24

Mother-Boards (for TRAMs)

Description	Part Number	Format	Page No.
IMS T212+IMS C004 + 10 TRAM Slots	IMS B008	IBM PC XT/AT	24
IMS T212 + 2 x IMS C004 + 16 TRAM Slots	IMS B012	Double Extended Eurocard	24
IMS T212 + 9 TRAM Slots	IMS B006	Double Extended Eurocard	25
IMS T414 + 1 Mbyte DRAM + 4 TRAM Slots	IMS B010	NEC PC 9801	25
IMS T414/IMS T800 + 2 Mbytes DRAM + 2 TRAM Slots	IMS B011	Double VME Card	25

Boards

Description	Part Number	Format	Page No.
IMS T414 + 2 Mbytes DRAM	IMS B002	Double Extended Eurocard	25
4 x (IMS T414 + 256 Kbytes DRAM)	IMS B003	Double Extended Eurocard	26
IMS T414 + 2 Mbytes DRAM	IMS B004	IBM PC XT/AT	26
IMS M212 +20 Mbytes Winchester Drive +1 Mbyte 3.5 inch Floppy Disk	IMS B005	Double Extended Eurocard	26
IMS T414+IMS G170 +Dual Port RAM	IMS B007	Double Extended Eurocard	26
4 x IMS A100+IMS T212 +(IMS T414 +1 Mbyte DRAM Upgrade)	IMS B009	IBM PC XT/AT	11

Systems

Description	Part Number	Format	Page No.
Board Rack (10 slots) +Power Supply	IMS B211	Double Extended Eurocard	27
IMS B211+10 x IMS B003 +Transputer Development System	IMS B213	Double Extended Eurocard	27

Development Tools

Description	Part Number A	Part Number B	Format	Page No.
Transputer Development System (TDS)	IMS D600	—	VAX/VMS	30
	IMS D700	IMS D701	IBM PC XT/AT	
	IMS D700	IMS D801	NEC PC 9801	
Stand Alone Toolsets (Mixed Languages + Multi-User)	IMS D505	IMS D525	SUN 3	31
	IMS D605	—	VAX/VMS	
	IMS D705	IMS D725	IBM PC XT/AT	
	IMS D705	IMS D825	NEC PC 9801	
Scientific Languages (C, Pascal, Fortran)	IMS D511/2/3	—	SUN 3	32
	IMS D611/2/3	—	VAX/VMS	
	IMS D711/2/3	—	NEC/IBM PC	
Cascadable Signal Processor Development System	IMS D703		IBM PC XT/AT + IMS B004	10
IMS D703+Evaluation Hardware (IMS B009)	IMS D704		IBM PC XT/AT	10

KEY

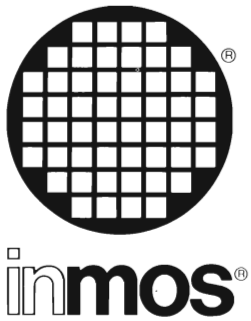
A Software only
B Integrated Software and Hardware

Static RAM

Organisation	Part Number	Package	Access Time (ns)	Page No.
4K x 1	IMS 1203	S,P	20, 25, 35, 45	34
	IMS 1203M	S	25, 35, 45	
1K x 4	IMS 1223	S,P	20, 25, 35, 45	35
	IMS 1223M	S	25, 35, 45	
16K x 1	IMS 1403	S,P,W	25, 35, 45, 55	36
	IMS 1403M	S,N	35, 45, 55	
	IMS 1403LM	S,N	35, 45, 55	
	IMS 1400M	S,N	45, 55, 70	
4K x 4	IMS 1423	S,P,W	25, 35, 45, 55	37
	IMS 1423M	S,N	35, 45, 55	
	IMS 1420M	S,N	55, 70	
2K x 8	IMS 1433	S,P	35, 45	38
	IMS 1433M	S	45, 55	
64K x 1	IMS 1600	S,P,W	35, 45, 55	39
	IMS 1601L	S,P,W	45, 55	
	IMS 1600M	S,N	45, 55, 70	
	IMS 1601LM	S,N	45, 55, 70	
16K x 4	IMS 1620	S,P,W	35, 45, 55	40
	IMS 1620A	S,P,W	25, 35	
	IMS 1620M	S,N	45, 55, 70	
	IMS 1620LM	S,N	45, 55, 70	
	IMS 1624	S,W	35, 45, 55	41
	IMS 1624A	S,W	25, 35	
	IMS 1624M	S,N	45, 55, 70	
	IMS 1624LM	S,N	45, 55, 70	
8K x 8	IMS 1630	S,W	45, 55	42
	IMS 1630M	S,N	55, 70	
	IMS 1630LM	S,N	55, 70	

Package Cross Reference

S Ceramic Dual In Line
P Plastic Dual In Line
N Leadless Chip Carrier (solder dip)
W Leadless Chip Carrier (gold finish)
G Ceramic Pin Grid Array
J Plastic J-Lead Chip Carrier



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